

PCB Design Techniques for the SI and EMC of Gb/s Differential Transmission Lines

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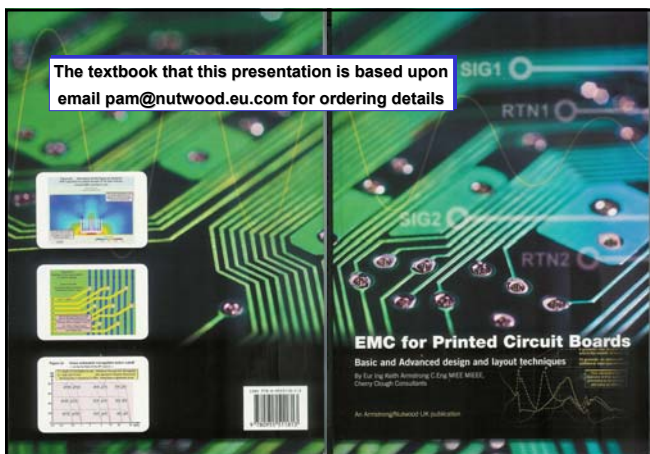
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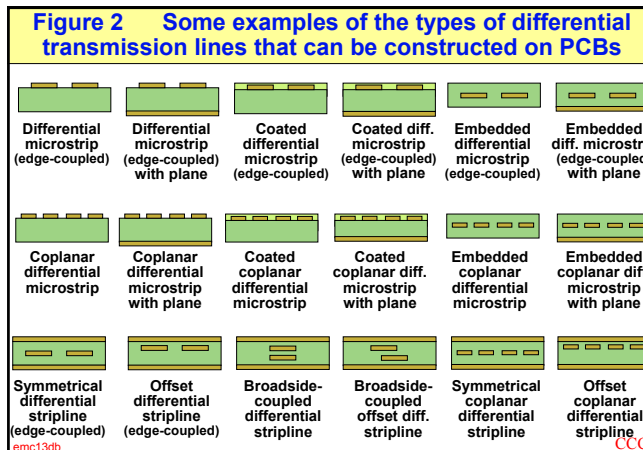
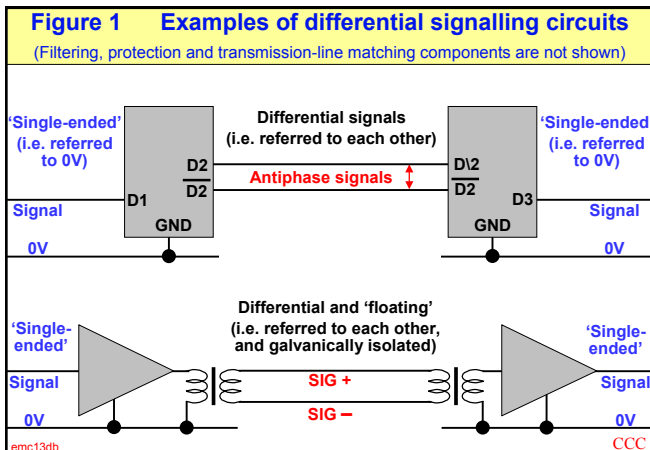
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Introduction

- Differential signalling is being increasingly used in PCBs for high-speed clocks and data
 - because of their benefits for signal integrity (SI) and electromagnetic compatibility (EMC)
 - ◆ e.g. LVDS; PCI Express
- They use two traces driven with antiphase signals – usually called a ‘differential pair’
 - these traces are designed and routed as *differential transmission lines* on PCBs

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Introduction continued...

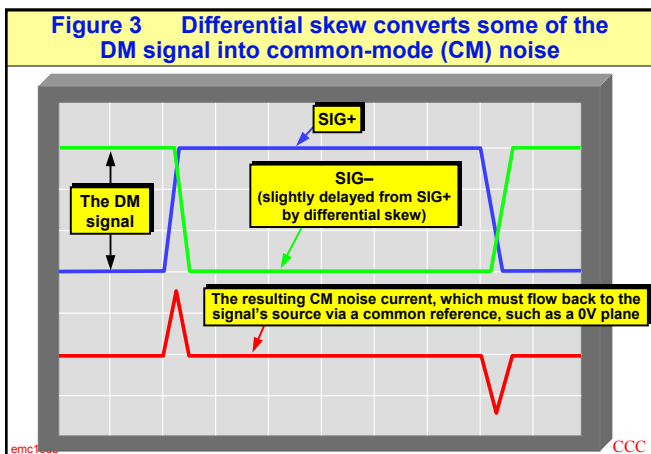
- But differential signalling suffers from *imbalances*, caused by...
 - Errors in the Z_{ODM} and Z_{OCM} of the traces in a pair
 - Arrival time differences between the + and - signals (i.e. differential skew)
 - Driver timing asymmetry; different driver impedances (pull-up versus pull-down)
 - Errors in matching the terminations over the frequency range of interest (not covered further here)

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Introduction continued...

- Trace-pair imbalances convert some of the differential-mode (DM) signal into unwanted common-mode (CM) noise currents...
 - worsening EMC (emissions) and signal integrity (SI)
 - and they also allow CM noise in the environment to be converted into DM signals (worsening immunity)
- Some causes of imbalance will be described...
 - as will some design techniques for controlling them, to help achieve good EMC and SI

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The effects of imbalance on differential signalling

- The 'balance' or 'symmetry' of a differential pair should be maintained over its full length...
 - otherwise SI and EMC (emissions and immunity) will be made worse
- Where the CM return path is not perfect...
 - e.g. gaps or splits in the common plane, or when the line connects to a cable with imperfect shielding...
 - a differential skew as large as 80ps can make emissions as bad as a single-ended signal

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Close-coupled trace pairs are often the best for EMC

- There is *always* imbalance, hence CM current flowing in the common reference (e.g. a plane)
 - close-coupling traces reduces CM currents
- Most THP PCB planes are imperfect due to the high degree of perforation caused by the vias
 - ◆ HDI (microvias) PCBs have much better planes
- For a given Z_{ODM} close-coupled traces are narrower – so trade-offs may be required

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Figure 4 Examples of differential line terminations (using the 'incident wave switching' method)

$R1A = R1B$, chosen to match the transmission line's CM ('even order') characteristic impedance (Z_{OCM})

$R2$ in parallel with $(R1A+R1B)$ matches the transmission line's DM ('odd order') characteristic impedance (Z_{ODM})

'RC', 'Thévenin' and 'Active' termination methods can also be used, as can reflected wave termination.

Classical termination (termination at *both* ends of the transmission line) is the best, but requires sensitive receivers

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Causes of imbalance

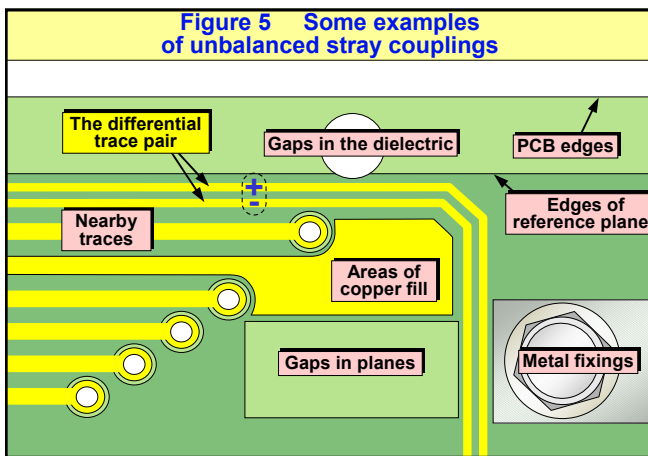
- Unequal stray coupling to the traces
- Differences between the two trace widths
- Propagation time differences for + and - signals
 - ◆ e.g. caused by woven PCB substrates such as FR4
- Driver timing asymmetry
- Different driver impedances (pull-up versus pull-down)
- Changing layers in the PCB
- Coatings on microstrip traces

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Unequal stray coupling to the traces

- Unequal stray coupling occurs when one trace in a pair is closer than the other to...
 - ◆ a gap in a PCB, or an edge
 - ◆ a gap in a copper plane, or an edge
 - ◆ an object (whether metal, glass, plastic, ceramic, etc.)
 - ◆ an area of copper fill pattern, or another trace
 - ◆ water, oil or other liquids
- Using stripline (ideally, coplanar stripline) helps 'shield' trace pairs from stray coupling
 - ◆ and using closely-coupled traces (routed very close together) also helps reduce stray coupling imbalance

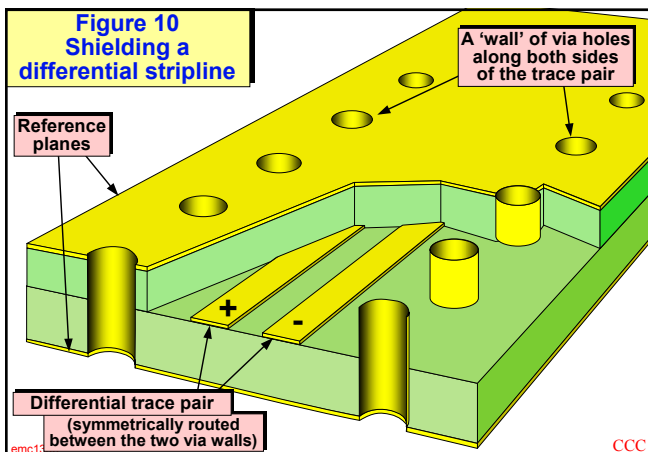
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Shielded striplines

- Trace pairs can be shielded from strays coupling to nearby objects, by placing 'walls' of via holes symmetrically along both sides...
 - with the vias connecting the top and bottom planes
 - ◆ and the vias spaced apart by less than 1/10th of the wavelength, at the highest frequency of concern
- This makes it easier to achieve a good balance
 - and the shielding also reduces the EMC impact of line imbalance from other causes
 - ◆ but does not prevent them from affecting SI

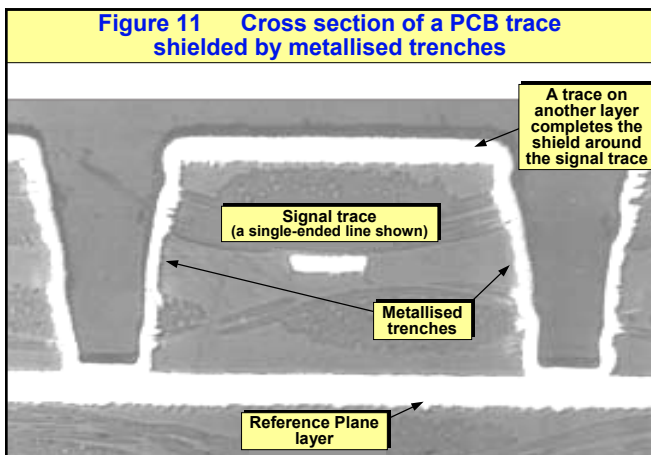
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Shielded striplines continued...

- Some PCB manufacturers can create fully shielded traces inside a PCB
 - by cutting trenches and plating them with copper
- This provides better shielding performance than 'channelising' with rows of via holes
 - but must be symmetrical to maintain line balance
 - and the good shielding performance reduces the EMC impact of any remaining imbalances
 - ◆ but doesn't reduce their effect on SI

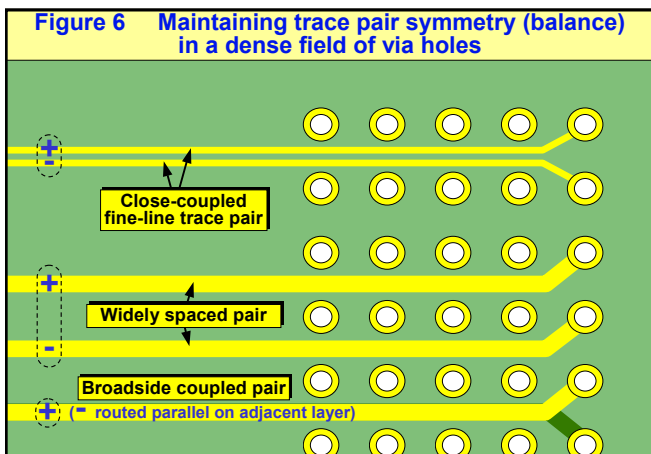
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Routing a differential pair through a dense field of via holes

- It is best to route the trace pair symmetrically between the vias
 - ◆ using fine-line traces or microvia (HDI) PCB technology as necessary
- To minimise costs, it might be acceptable to...
 - ◆ vary trace widths to compensate for imbalances
 - ◆ increase the spacing between the traces to route only one trace between vias (but use symmetrical routing)
 - ◆ use broadside routing

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Differences in trace widths

- Variations in trace widths can cause imbalance, and can be caused by...
 - uneven manufacturing processes that etch one trace more than the other
 - the limited resolution of the phototool (e.g. Gerber)
- Narrower trace widths suffer more
 - so when using very narrow traces to overcome some imbalance or other problems, there may be some trade-offs to make to optimise EMC

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Differences in trace widths continued...

- Techniques for controlling imbalance due to trace width variations include...
 - placing two or more 'test traces' on the PCB
 - ◆ and testing their DM and CM Z_0 before accepting any batch of PCBs delivered by their manufacturers
 - ◆ requires a 4-port VNA, now available as instruments (e.g. from Polar Instruments) and probes that can be operated by relatively unskilled people
 - ◆ routing critical traces at 20° - 70° to the phototool's digitisation grid

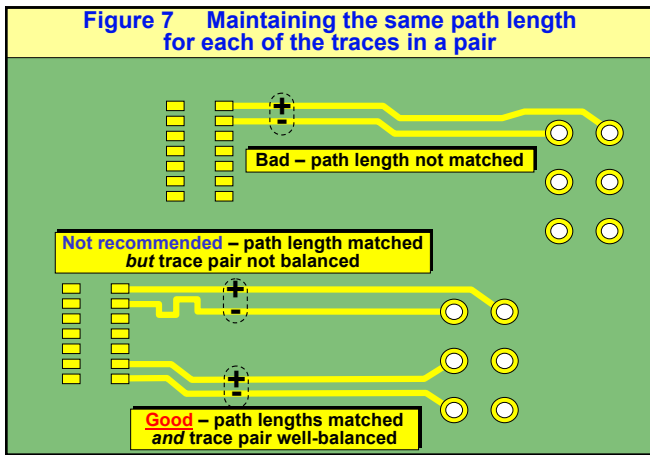
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Propagation time differences for the + and - signals

- Propagation time differences for the + and - signals cause differential skew directly
 - a major cause is differences between the lengths of the traces in a pair
 - needs to be $<1/10^{\text{th}}$ of the signal's rise/fall time for EMC to be significantly better than single-ended
 - e.g. for stripline in FR4, if signal rise/fall time is 150ps (equivalent to 22mm trace length) the path length difference should be $<2\text{mm}$
 - ◆ less, if there are other sources of differential skew

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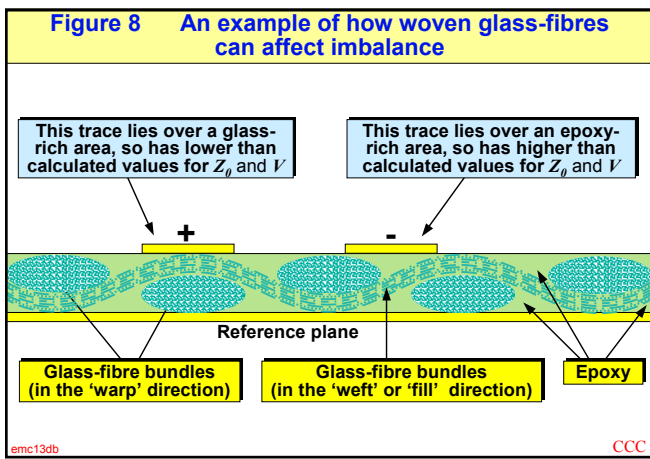
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The effects of woven PCB dielectrics

- Woven glass-fibre PCB dielectrics (like FR4) use glass-fibre with $\epsilon_r = 5.6$ and epoxy resin with $\epsilon_r = 3.2$ (both approx. values)
 - routing over a glass-rich region *reduces* Z_0, V
 - routing over an epoxy-rich region *increases* Z_0, V
- The resulting imbalance problems can be severe (as much as 5% of the line's propagation time)
 - but the problems can be reduced by routing at 30°-60° to the direction of the PCB's glass-fibres

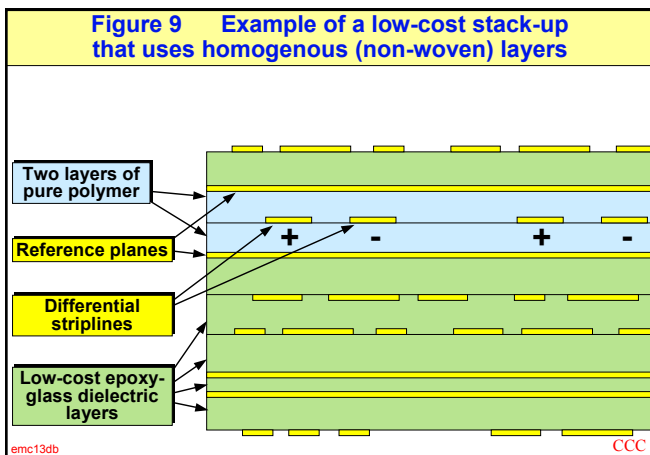
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Using homogenous dielectrics

- Homogenous dielectrics are good, but costly
 - ◆ they use non-woven materials, e.g. pure polymers
- To save cost, use just one or two homogenous layers in a PCB stack-up that is otherwise made of layers of low-cost woven glass-fibre dielectric
 - route the differential traces so that their Z_0 and V are governed by the homogenous PCB layer(s)
 - ◆ but make sure that the PCB manufacturer proves he can achieve good yields and PCBs that will be reliable over the products' lifecycles

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Problems caused by changing layers

- It is very difficult to control Z_{0DM} and Z_{0CM} and the CM return path through a layer change
 - and the unused 'stubs' of any via holes can cause big problems (especially with PCBs thicker than 1.6mm)
- So Gb/s differential transmission lines should be point-to-point, routed entirely on one layer
 - except at the ends, to connect to driver and receiver
 - ◆ when the total distance from 'end of trace' to silicon (including the IC's lead frame and bond wires) should be less than $<1/10^{th}$ the rise/fall time for good EMC

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Problems with coated microstrips

- Microstrip traces are usually coated with solder resists, 'silk screen' legends, etc.
 - ◆ the dielectric constants of these coatings are often unknown, or not very well controlled
- and if they cover more of one trace than the other, or are thicker over one trace, this causes imbalance
- Best dealt with by design (e.g. no coatings over differential pairs)
 - or by detailed specification of coating materials, and/or batch tests of PCB 'test traces'

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Driver timing asymmetry (between the + and - signals)

- Signal timing differences between the + and - outputs of the driver devices cause differential skew directly
 - some devices have very poor specifications
 - some have no specifications, or only 'typical' ones
- So always read the data sheets carefully
 - and choose devices on the basis of their *maximum* differential skew specifications

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Driver impedance asymmetry

- Typical drivers have different output impedances when they are pulling up, compared with when they are pulling down
 - so the waveshapes of the + signals might not be the exact opposite of the - signals
 - ◆ depending on the traces they are driving
 - another cause of imbalance that leads to CM noise
- So it is best to choose drivers with low (e.g. 10Ω) and 'symmetrical' output impedances

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Filtering

- It may be possible to low-pass filter some/all of the signals...
 - so that their imbalances would cause less of an impact on EMC (emissions and immunity)
- The rise/fall times of the filtered signals would need to be longer than the differential skew
 - ◆ the longer the better
- But only use filter capacitors in conjunction with series impedances (resistors or ferrites)

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Using field solvers

- PCBs can require many prototype-redesign iterations ('respins')
- Field solvers can reduce timescales and costs...
 - by designing differential pair routes for good balance *before* making the first prototype
- If field solver data can be included in circuit simulations...
 - analysis can include driver imbalances, for the best confidence in the first prototype PCB

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PCB Design for SI and EMC of Gb/s Differential Transmission Lines

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The reference numbers are from the PowerPoint notes associated with this presentation

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