

Full-Wave, High Speed Packaging Design

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“And here’s your new High Speed Package design project ...”

- Design a High Speed Package with more bandwidth, higher edge rates, faster clock speed and more throughput but make sure you:
 - Use the standard stack-up configuration
 - Use our preferred board material
 - Ensure that it meets the specs. for...
 - Input Impedance
 - Crosstalk
 - Eye Diagram
 - BER
 - Cost



“And while you are at it ...”

- Generate some...
 - S-Parameters, and TDR's for other departments
 - Equivalent circuit models for customers
 - Manufacturing and material tolerance studies
 - Eye diagrams and BER charts for a variety of frequencies
 - System Models



“Oh and don’t forget ...”

- Do it all in LESS time than ever before!



Issues Faced During Package Design

- Physical Design Issues
 - Design flow integration
 - Time to build/modify prototypes
 - Physical design constraints
 - Manufacturing variability
 - Material variability
- Electrical Performance Issues
 - S Parameters
 - System performance
 - Maximum clock speed
 - TDR response
 - Eye diagram
 - BER

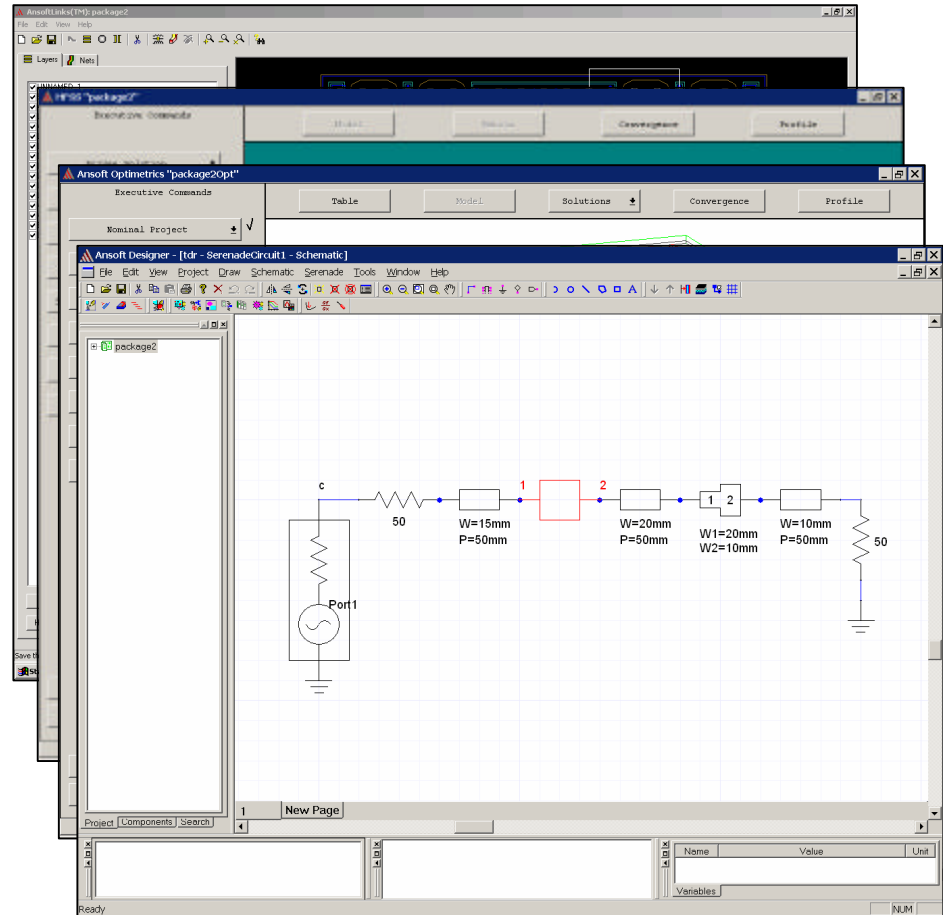
And other unexpected issues...

On with the design ...

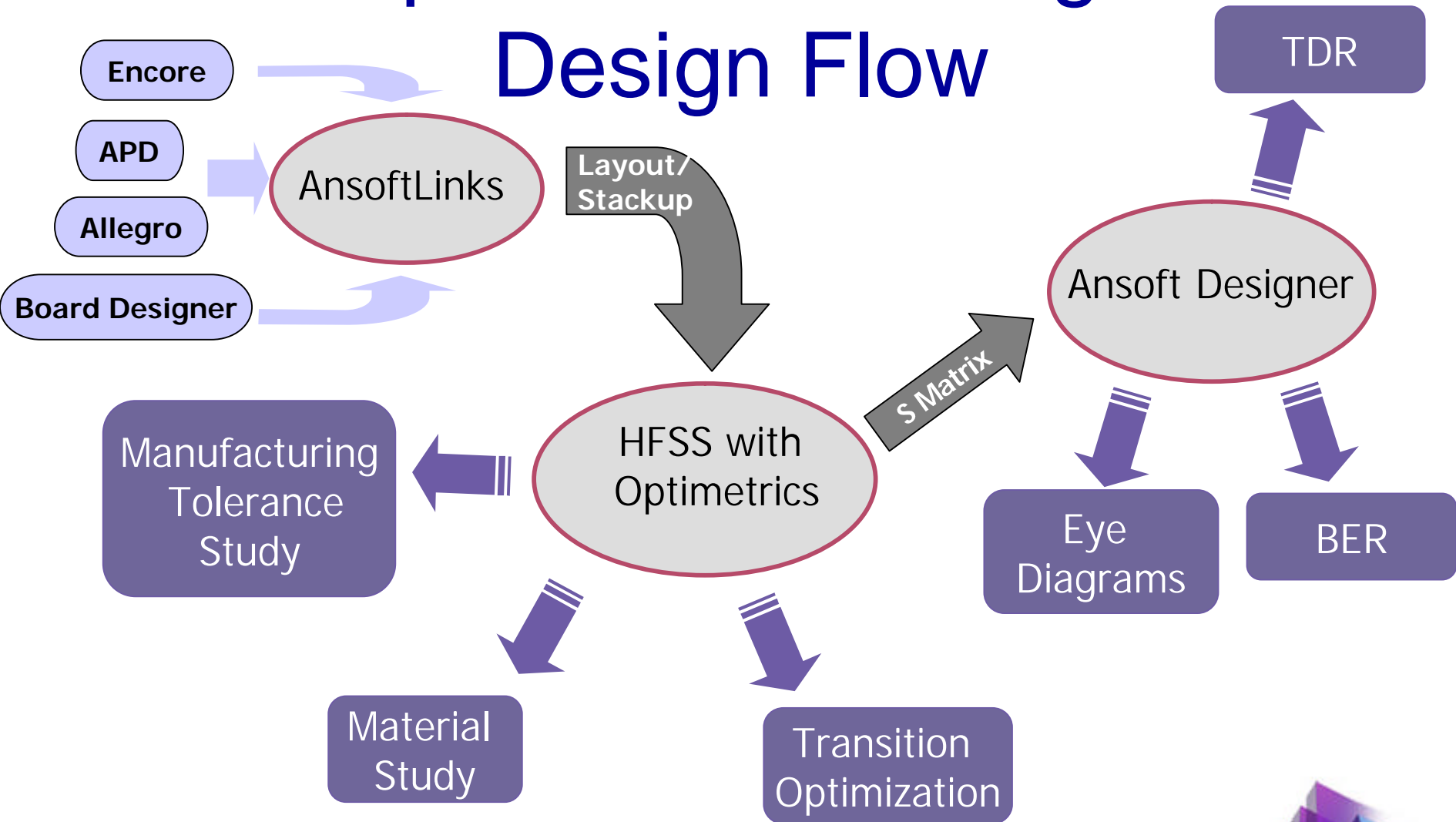
- Traditional design cycle
 - Design, Build and test
 - Re-design, rebuild, test, repeat
- The majority of the design and testing can be done with software tools
 - Layout Software, field, circuit, and system simulators
- Different simulation tools may not interface with the layout software, or even with each other
 - Disrupts the Design cycle
 - Creates additional work
- Ansoft offers a full design and simulations solution which will interface with layout software

The Ansoft Solution

- **AnsoftLinks™**
 - Integrates Ansoft into package design
 - Editing of vias, bondwires, etc..
- **HFSS™**
 - Accurate Full-wave analysis
 - Virtual prototyping
- **Optimetrics™**
 - Parametric studies
 - Optimization
- **Ansoft Designer™**
 - Circuit and System analysis
 - Frequency and Time Domain

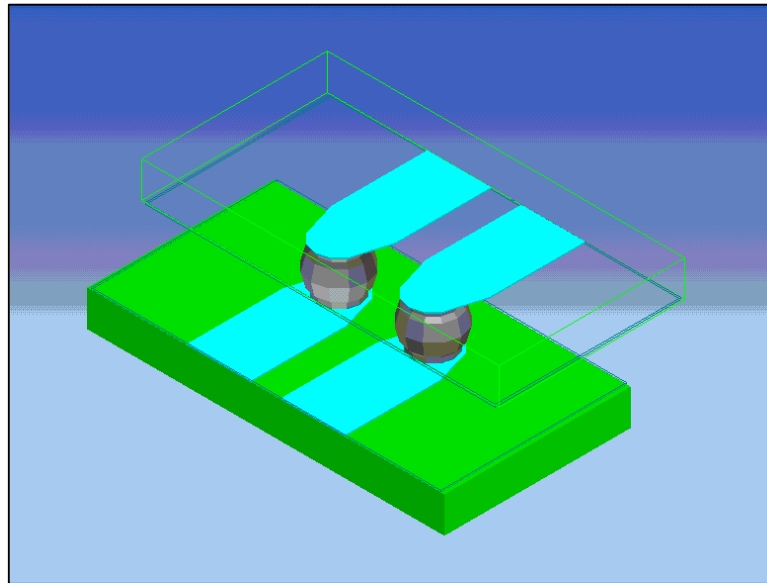


A Proposal for an Integrated Design Flow



A Test Case to Verify Methodology

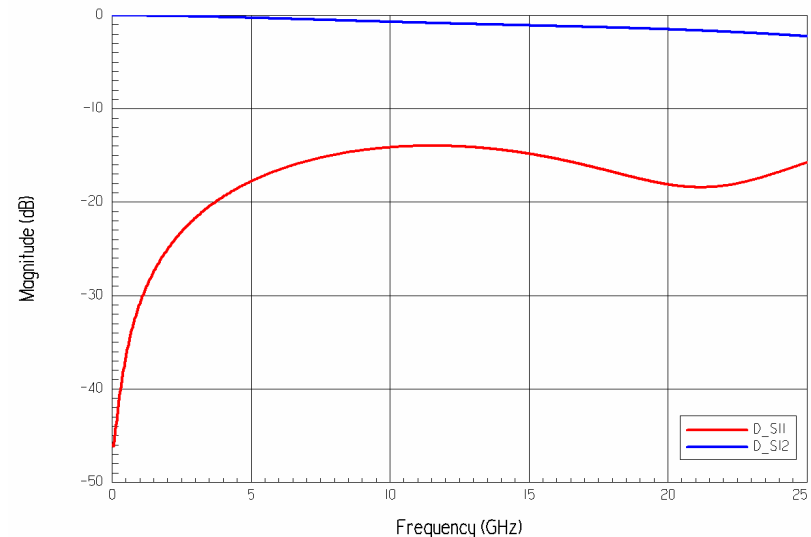
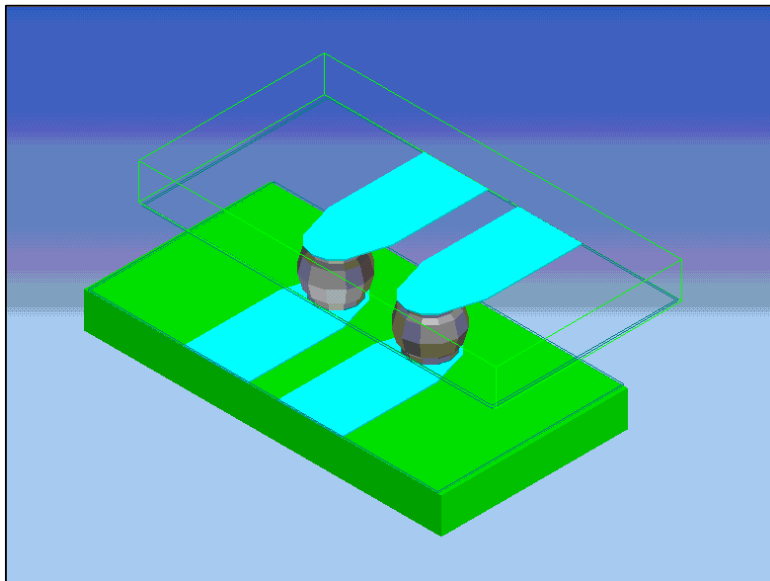
- Start with HFSS Model. Two solder ball transition model



- Export HFSS S-parameters to Ansoft Designer for time domain analysis
- Compare with measured TDR results

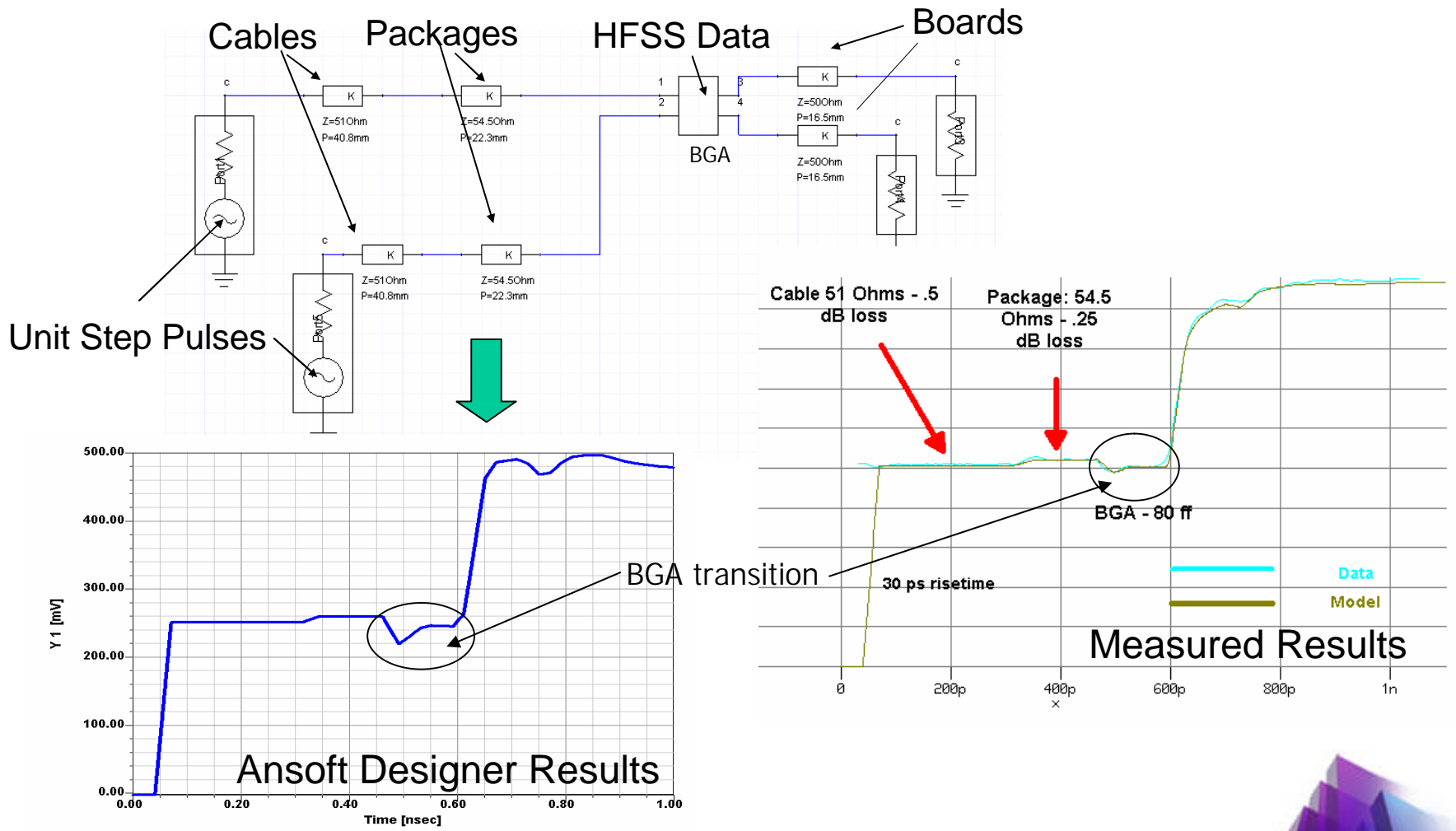
HFSS Results for the Test Case:

- HFSS model and the frequency response



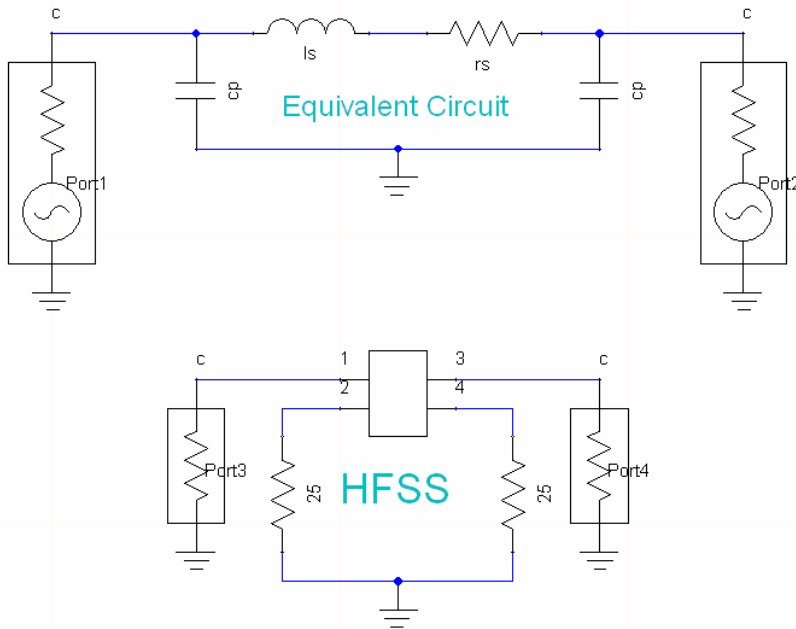
differential S-parameters

Designer TDR for the Test Case



An Equivalent Circuit for Test Case

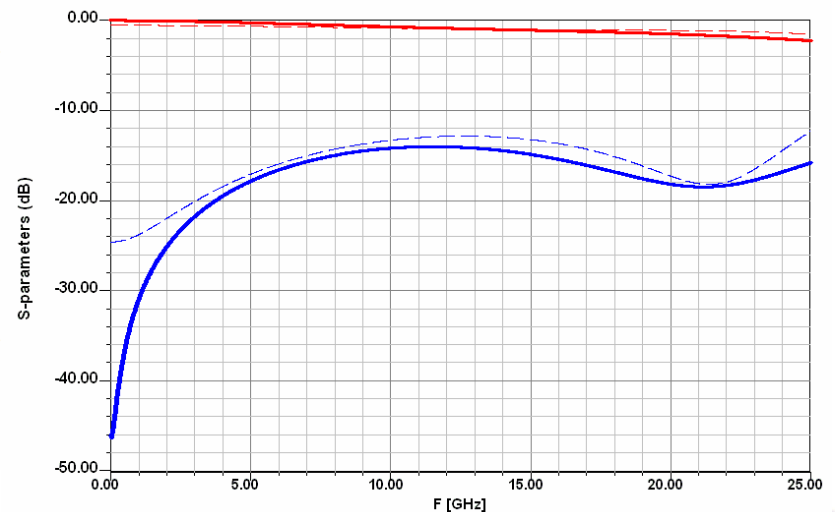
- Equivalent circuit development with Ansoft Designer.



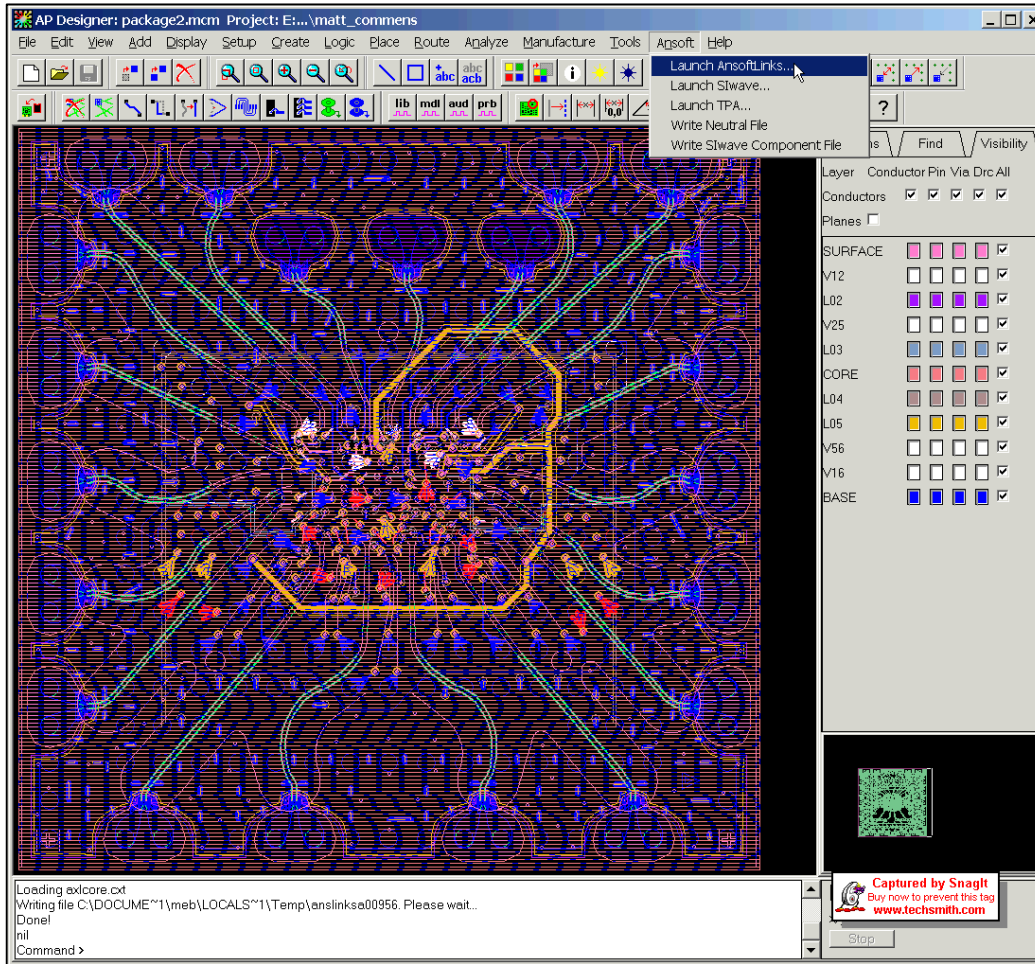
$C_p=0.082$ pF

$L_s=0.729$ nH

$R_s=12.65$ ohms



A “Real World” Problem



Package design courtesy of John Dunn, Tektronix.
<http://www.tek.com>

Package viewed in Cadence APD

“Into” the Design Flow

- Importing the structure into HFSS with AnsoftLinks

Package in An

Package in Cadence APD

Final structure in HFSS

AP Designer: package2.mcm Project: E:\...matt_commens

File Edit View Add Display Setup Create Logic Place Route Analyze Manufacture Tools Ansoft Help

Launch AnsoftLinks...
Launch SIwave...
Launch TPA...
Write Neutral File
Write SIwave Component File

Layer Conductor Pin Vis Drc All

Conductors

Planes

SURFACE

V12

L02

V25

L03

CORE

L04

L05

V56

V16

BASE

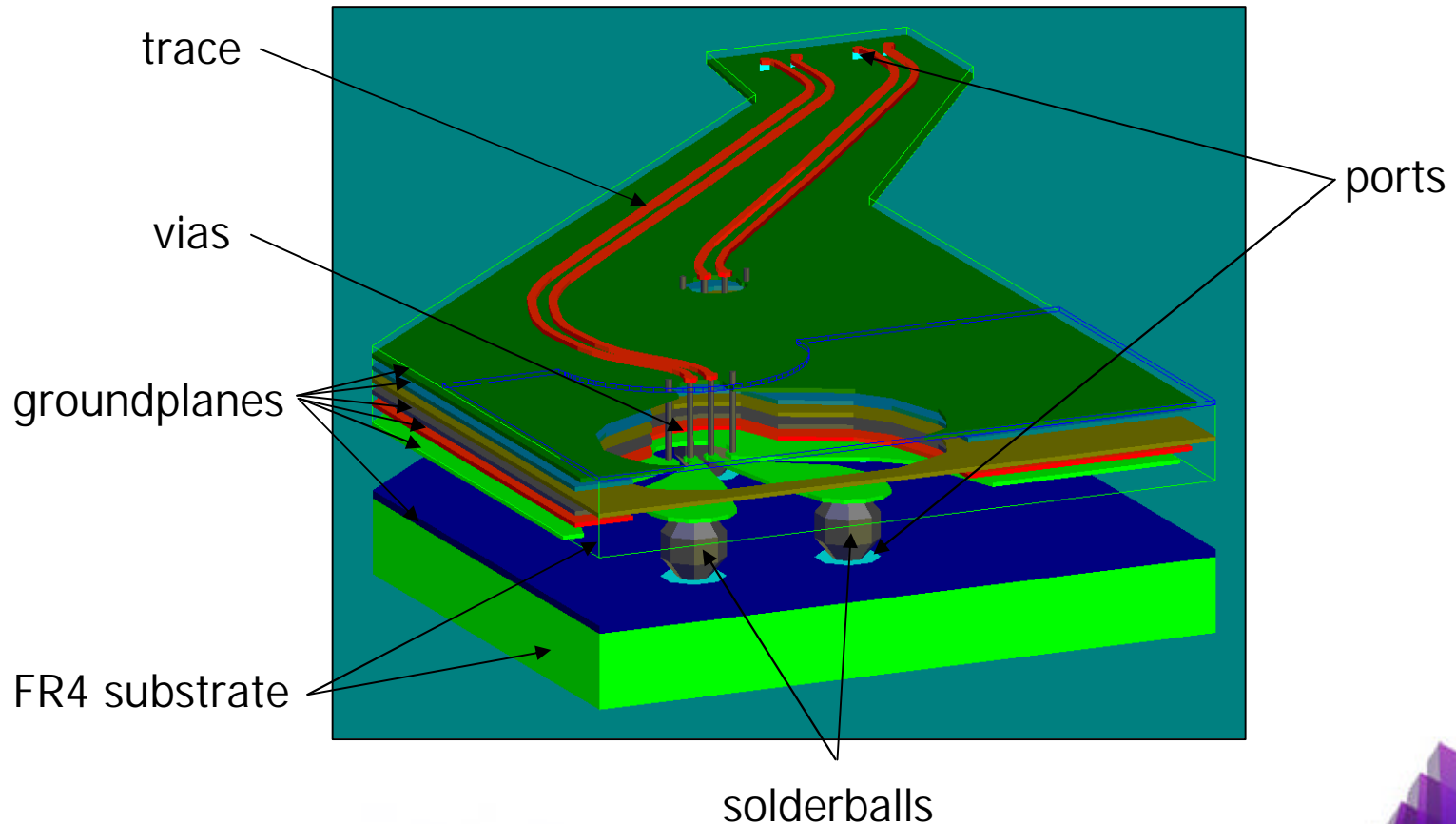
Loading excore.ct
Writing file C:\DOCUME~1\meb\LOCALS~1\Temp\anslinksa00956. Please wait...
Done!
nil
Command >

Captured by Snagit
Buy now to prevent this tag
www.techsmith.com

Stop

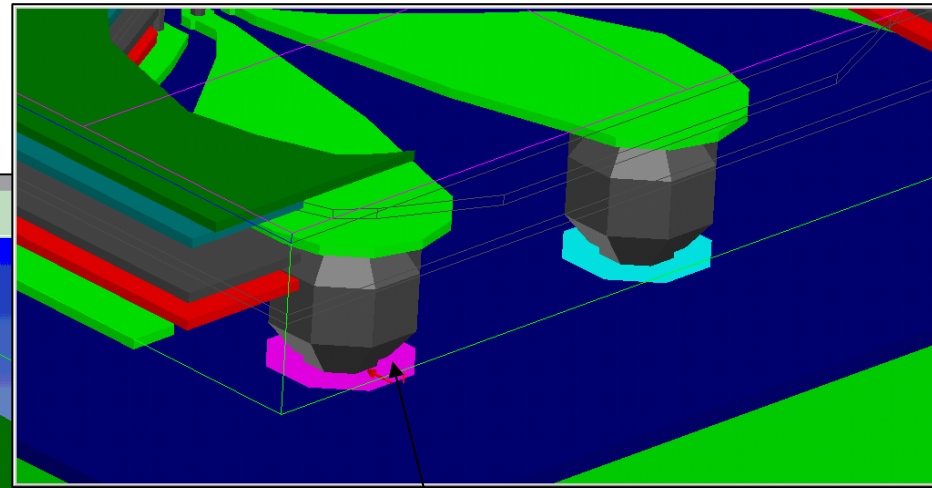
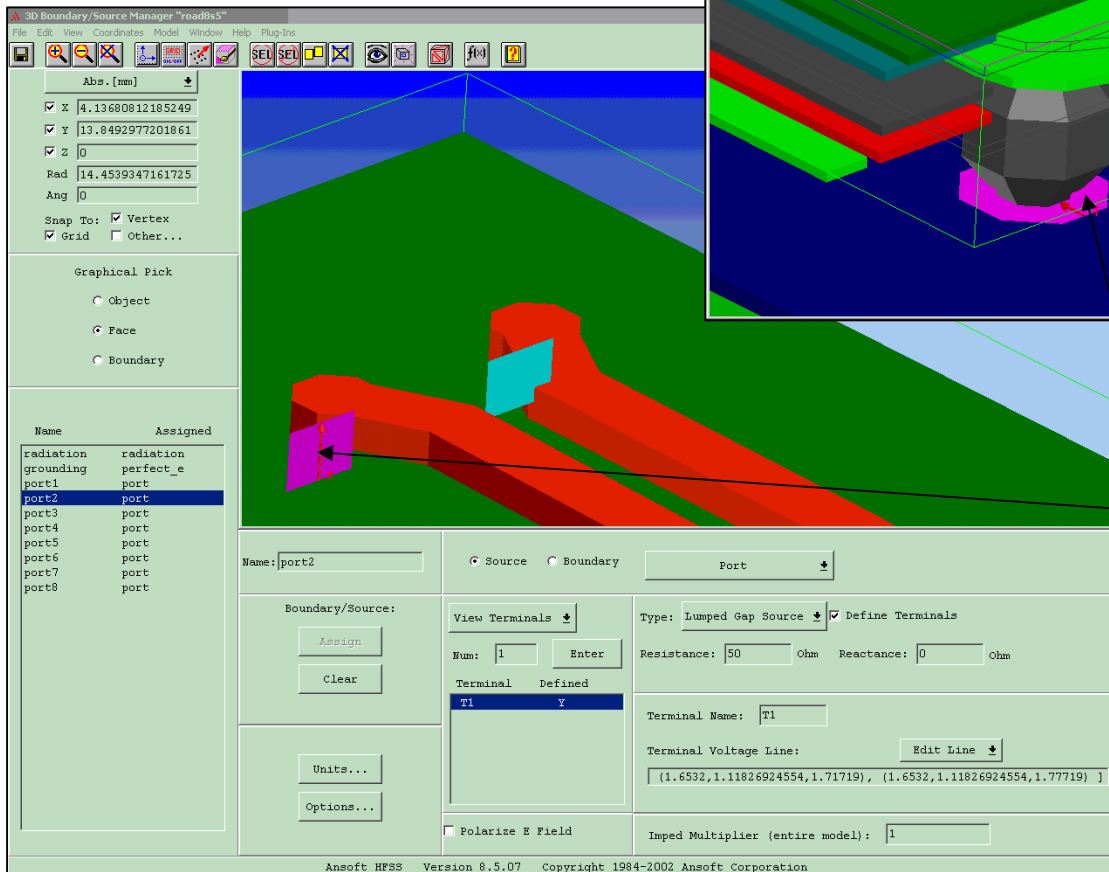
The Initial HFSS Model

- Inside HFSS, material properties, boundary conditions and excitations (ports) are defined.



The Initial HFSS Model

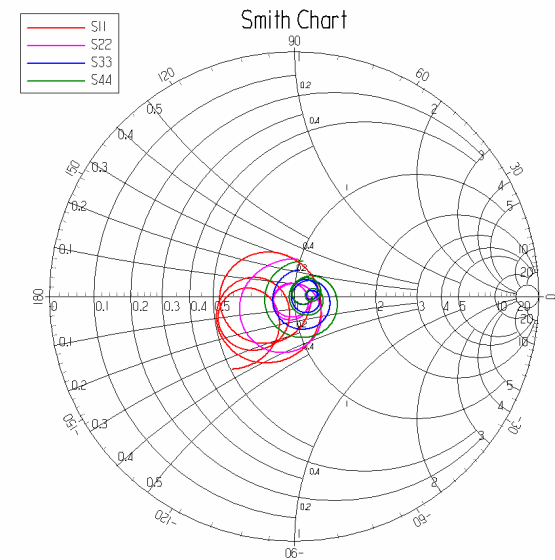
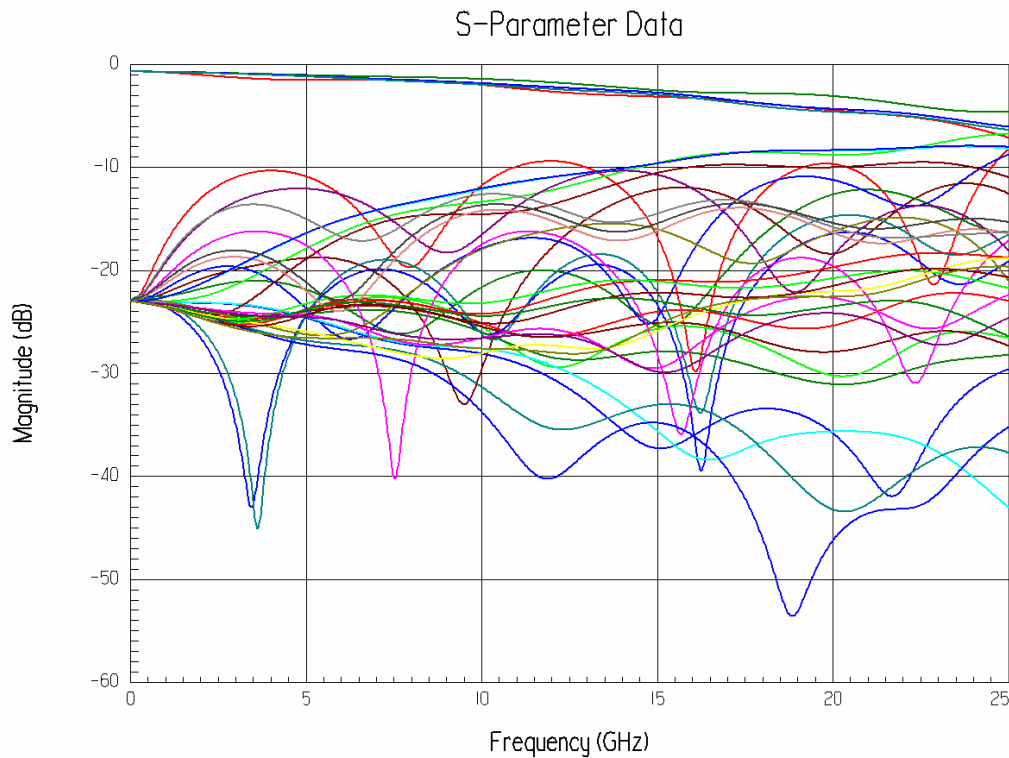
- Boundary Conditions and Ports



Lumped Gap Ports

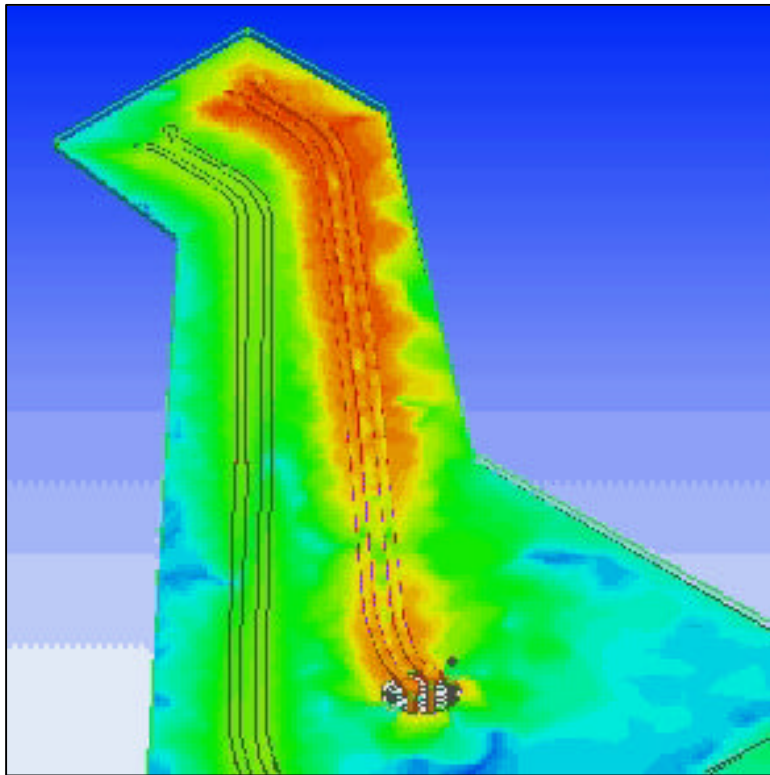
HFSS Results: S-parameters

- 2D Results: Single ended S-parameters (dB) and Smith Chart

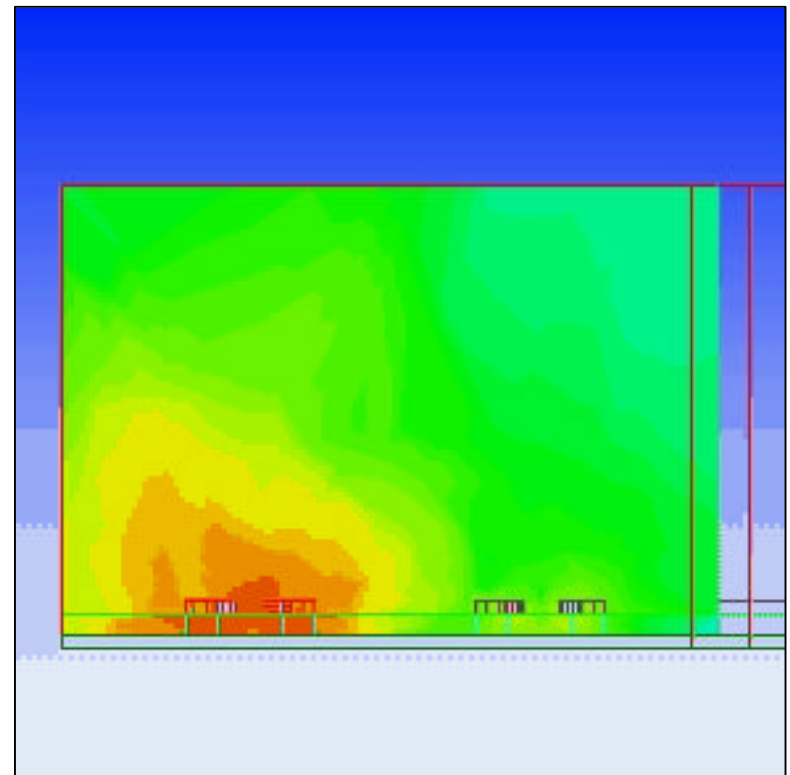


HFSS Results: Fields

- 3D field results: E-Fields for differential excitation.



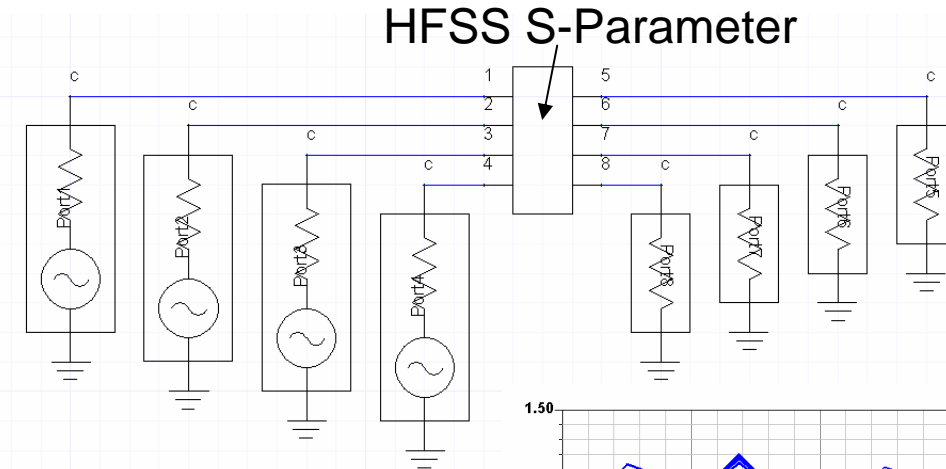
Along traces and groundplane



Through cutplane

Ansoft Designer Model

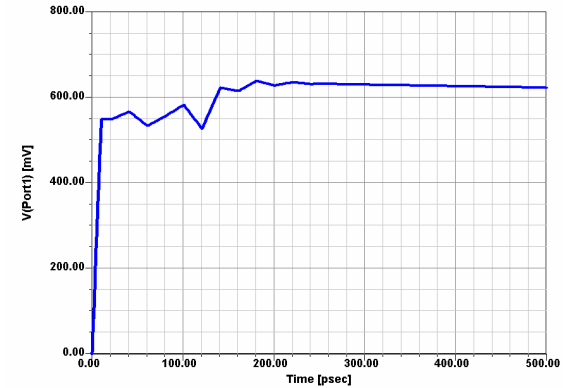
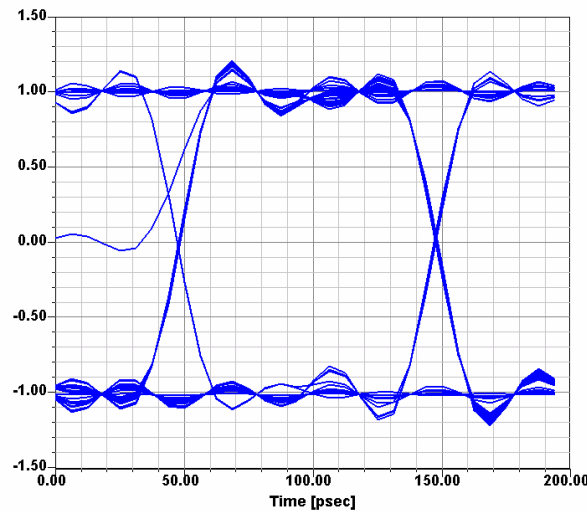
Schematic



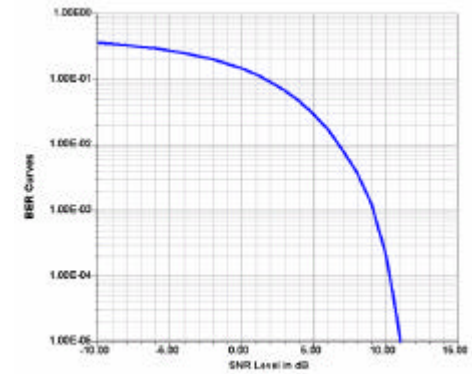
HFSS S-Parameter

Unit Step Pulses

Eye diagram



TDR

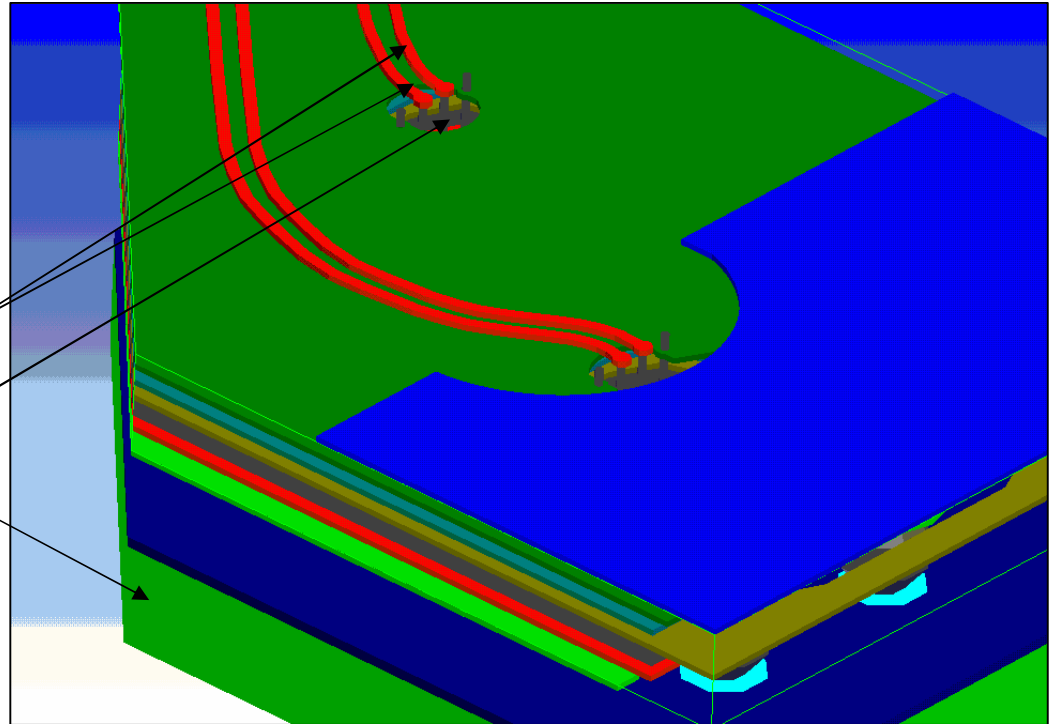


BER

Exploring the Design Space: Optimetrics

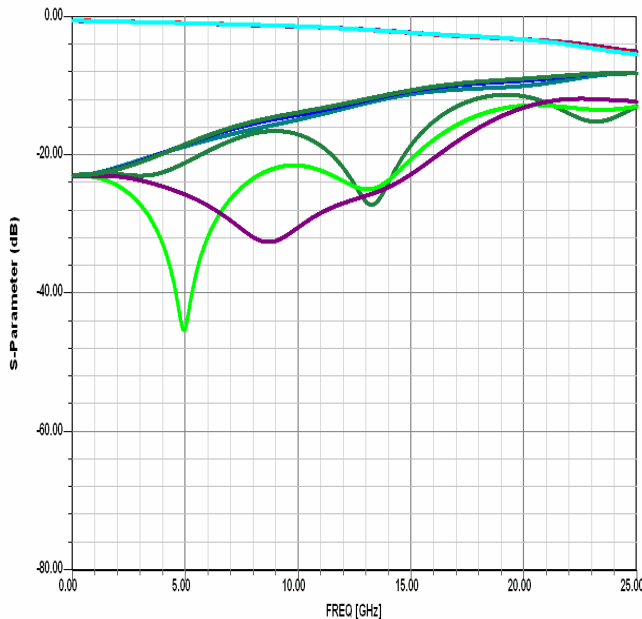
- Optimetrics will be used to perform parametric studies of the following:

- Trace width variability.
- Via thru-hole transition.
- Dielectric constant

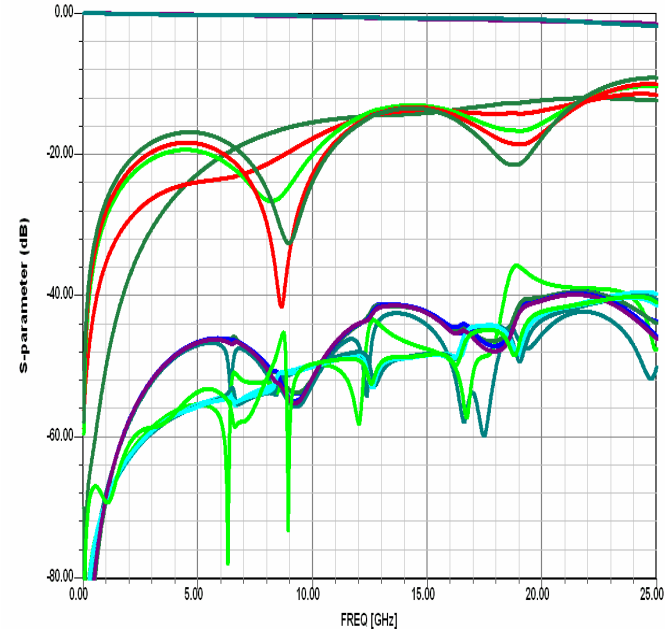


Impact of Manufacturing Variability

- Study effects of manufacturing tolerance.
- Vary trace width of differential pair, 0.060 mm +/-

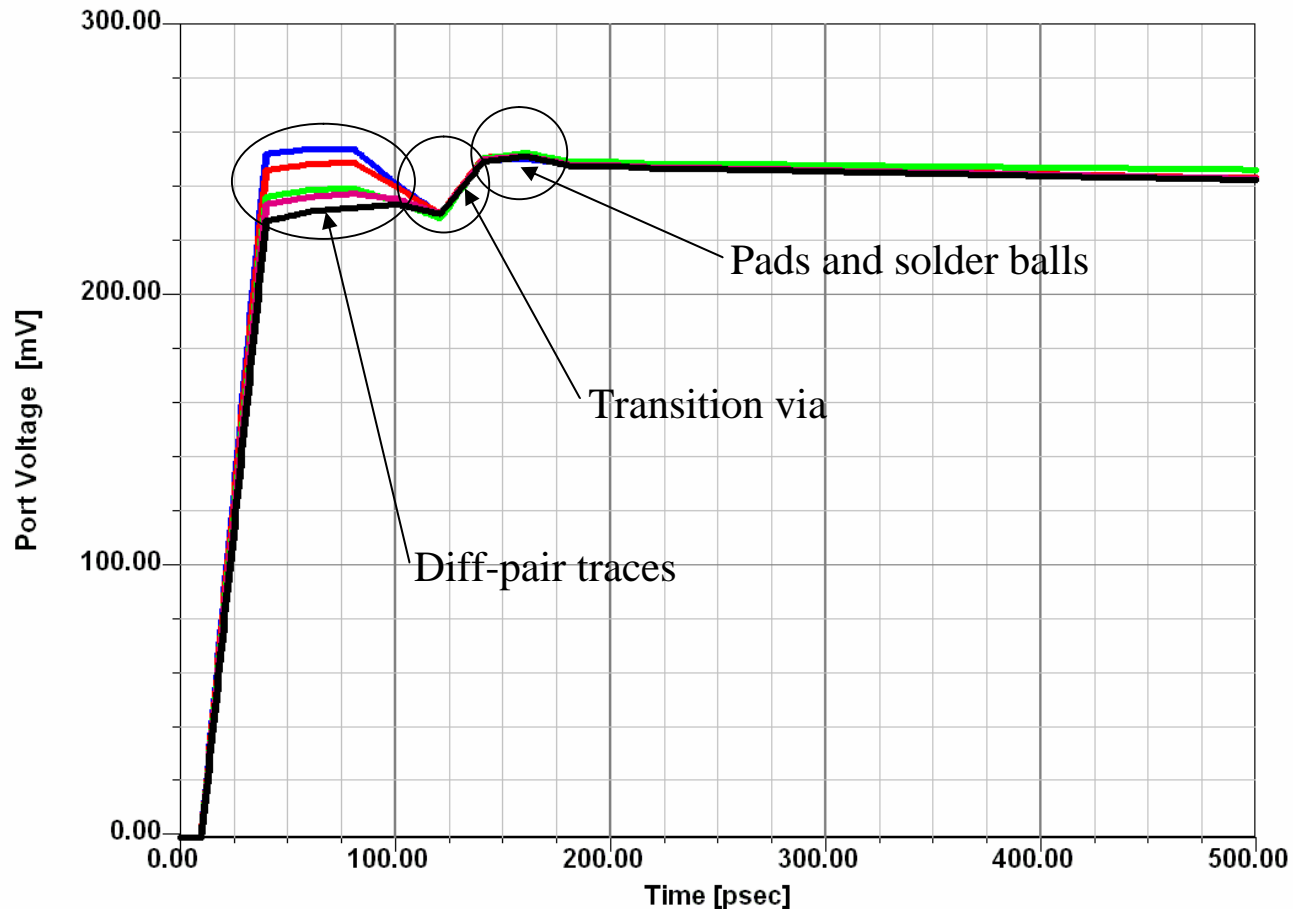


Single-ended S-parameters

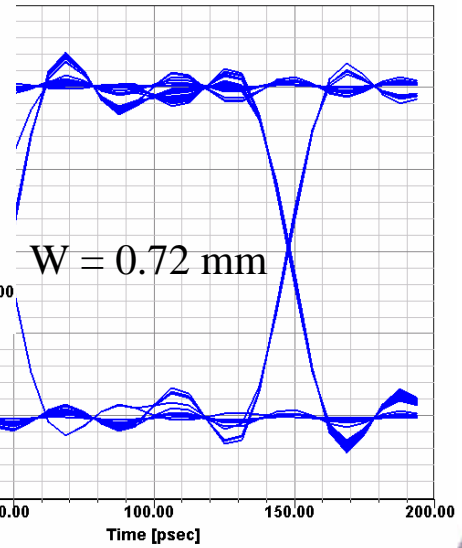
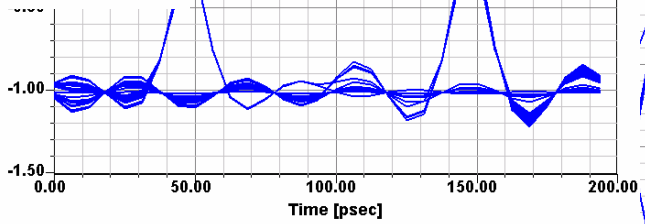
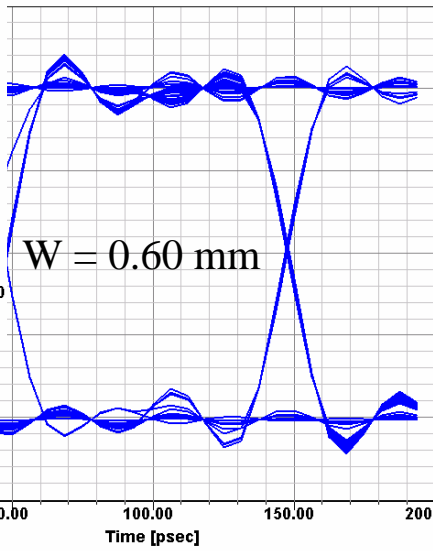
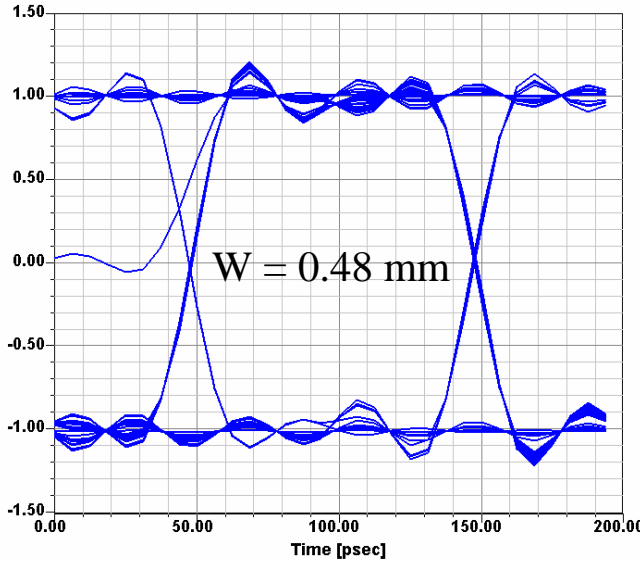


Differential S-parameters

Time Domain Responses of Trace-width Study

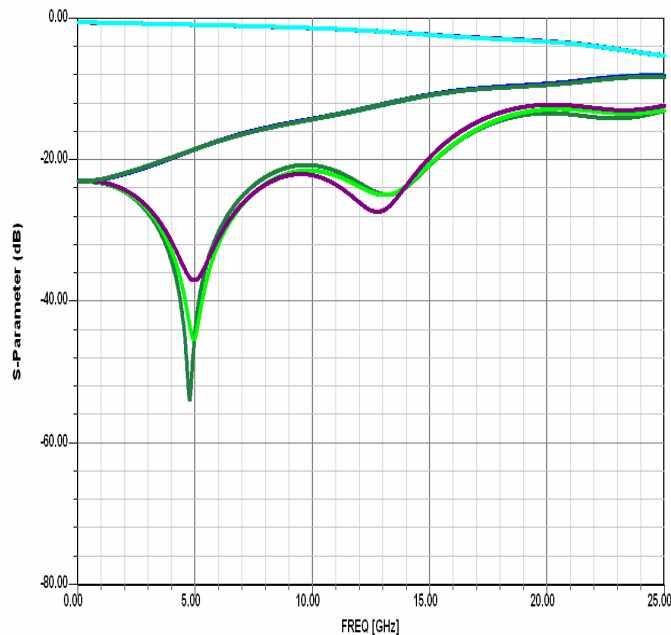


Eye Diagrams of Trace Width Study

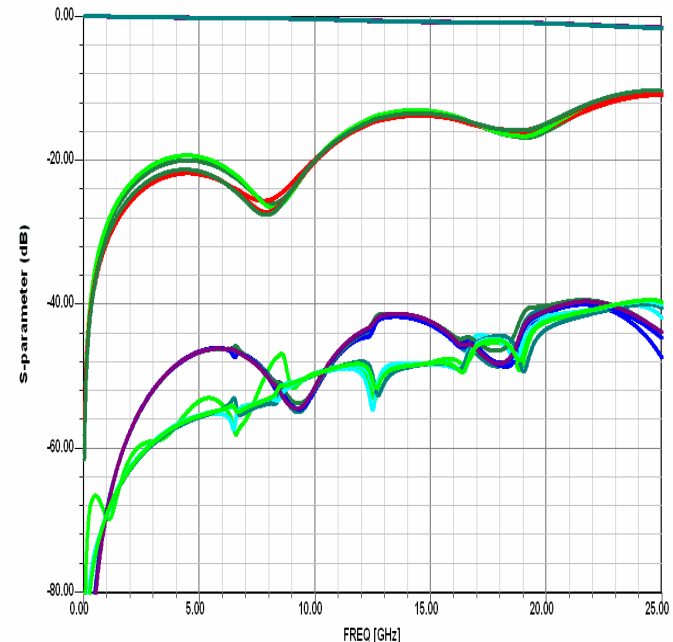


Study the Size of the Via Transition

- Study effect of thru-hole diameter for differential vias.
- Vary diameter, 0.50 +/- 0.10 mm.

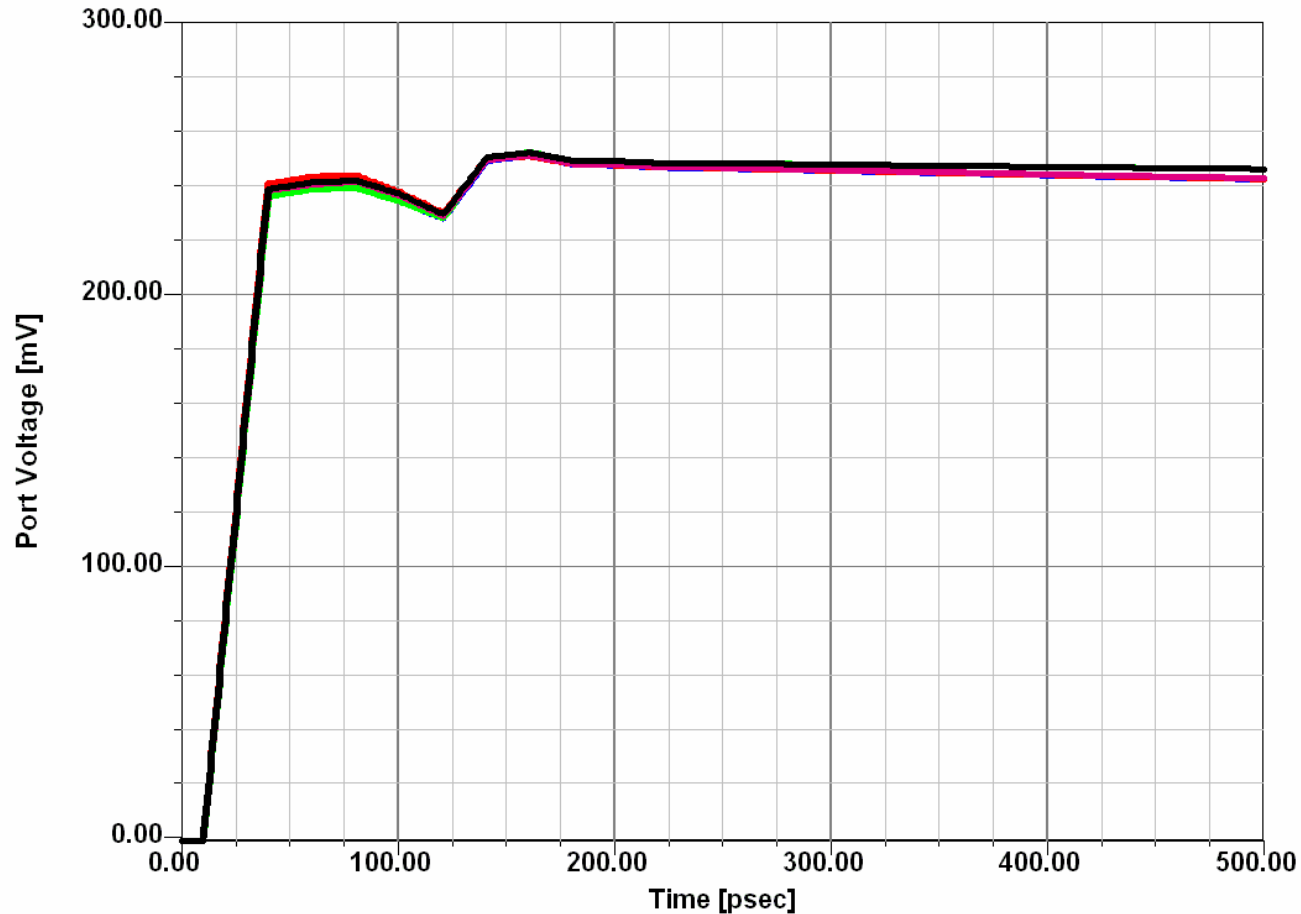


Single-ended S-parameters

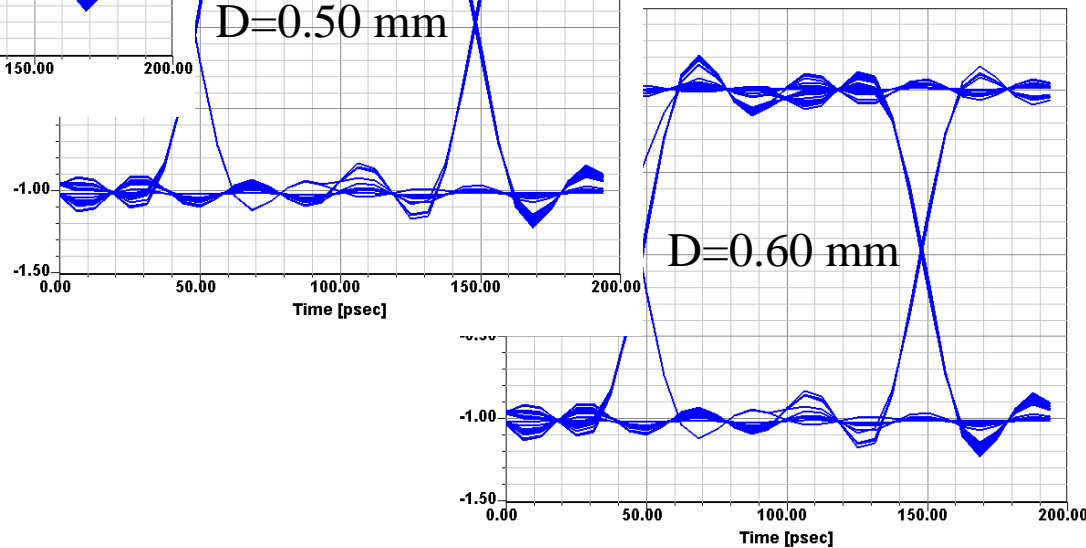
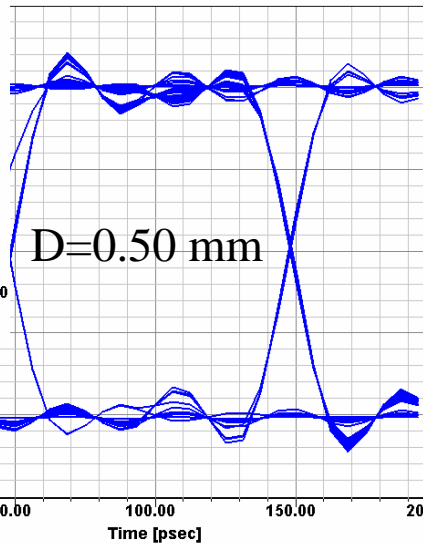
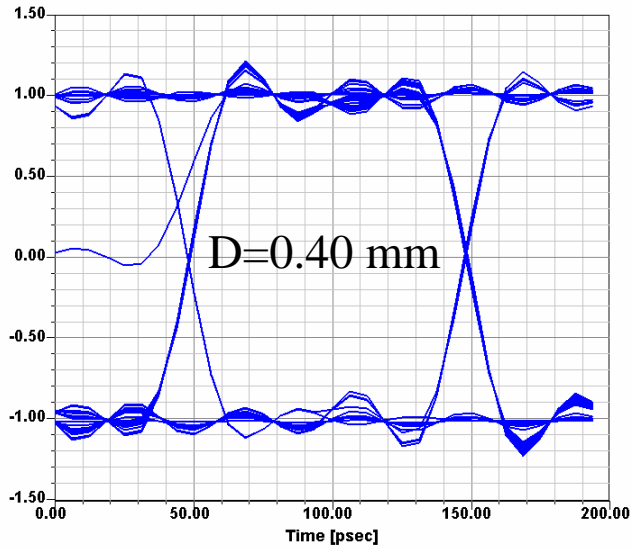


Differential S-parameters

Time Domain Responses of Thru-hole Diameter

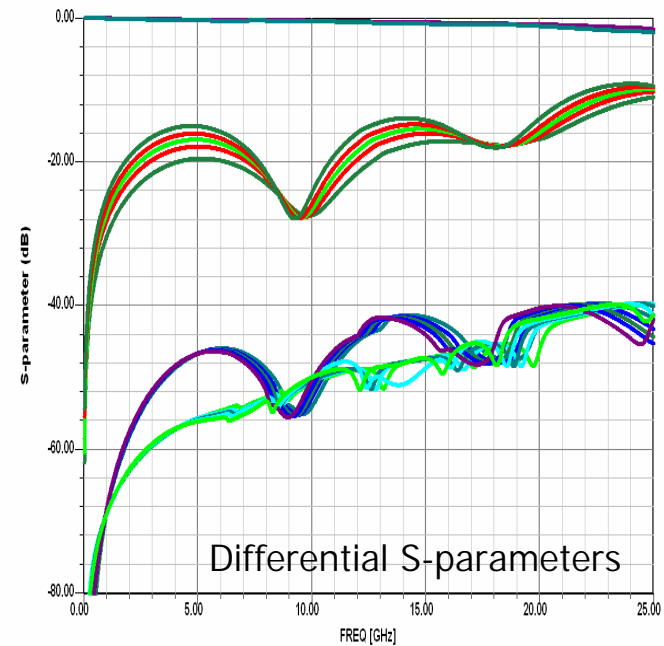
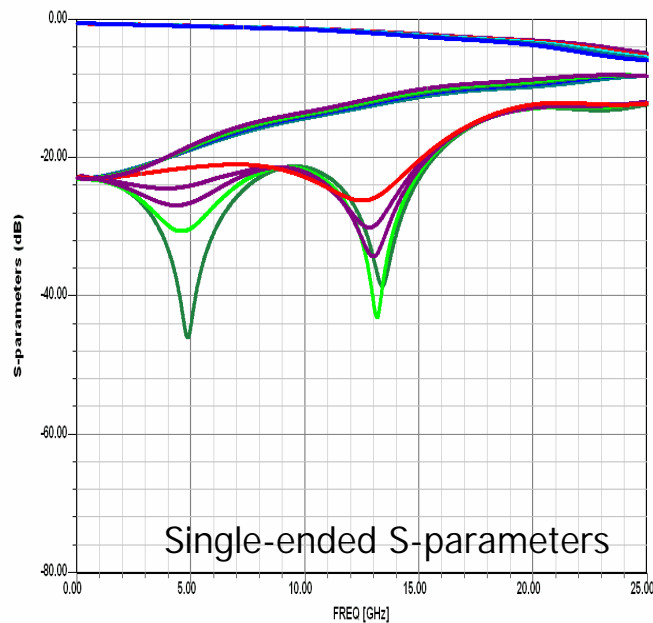


Eye Diagrams of Thru-hole Study

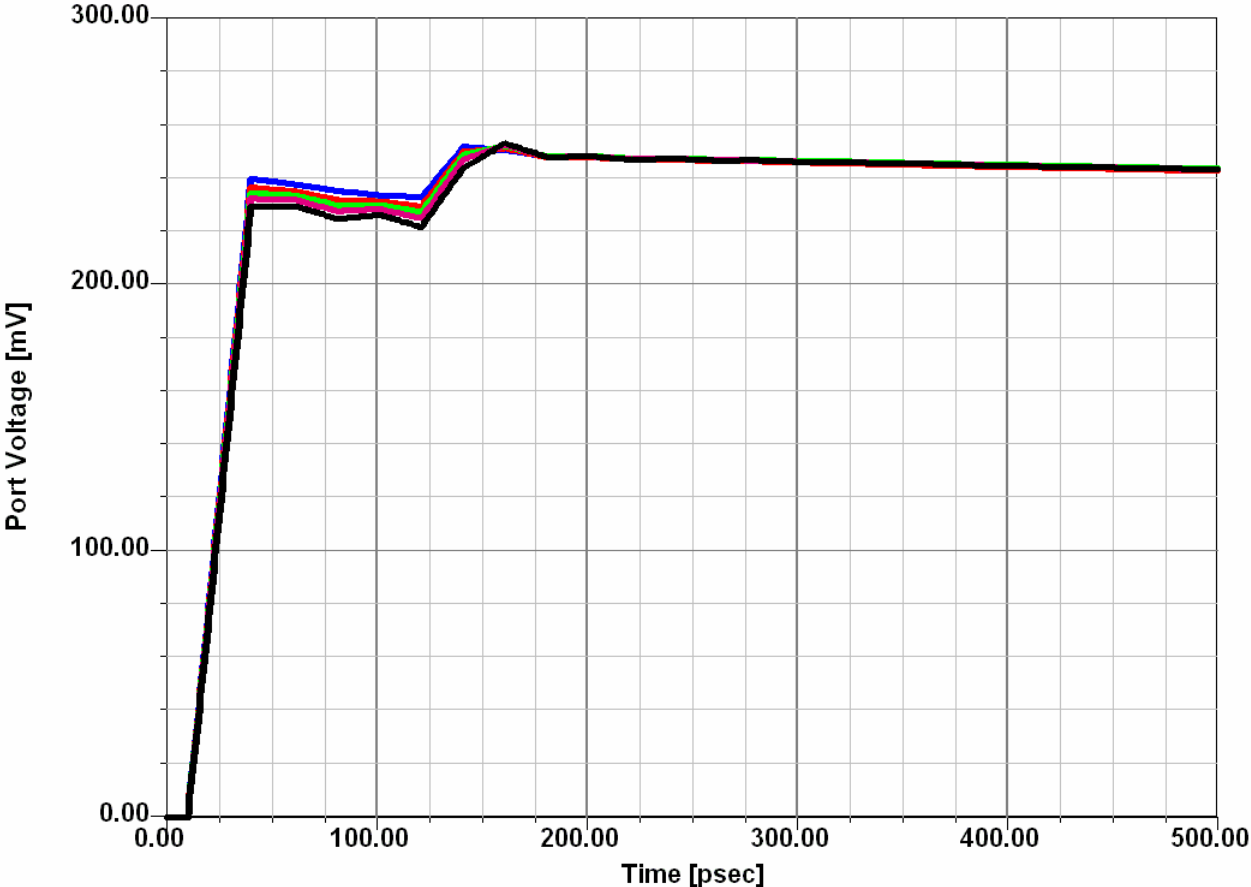


Determining the Effect of Material Variability

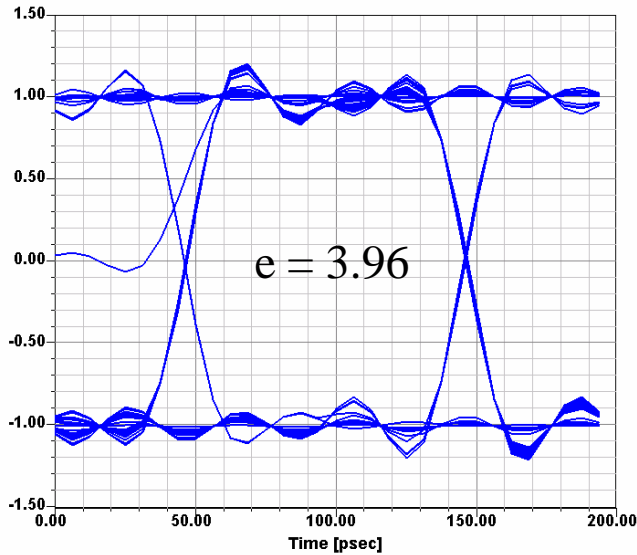
- Study the effect of material variation in substrate dielectric constant
- Vary dielectric constant of substrate, $\epsilon_r = 4.4$, +/- 10%



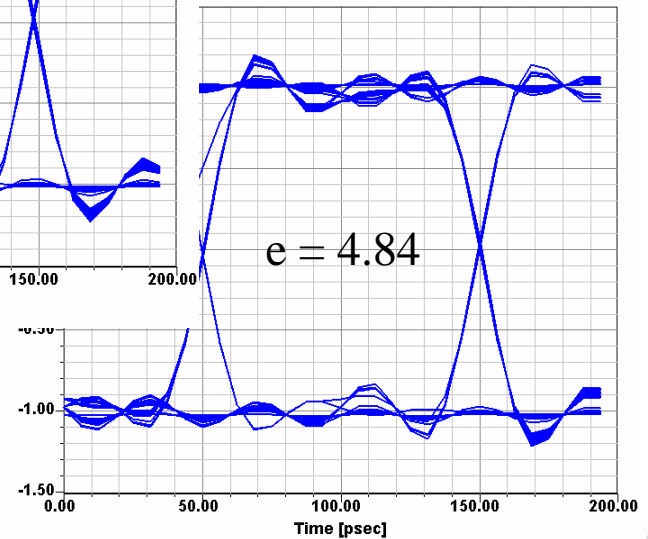
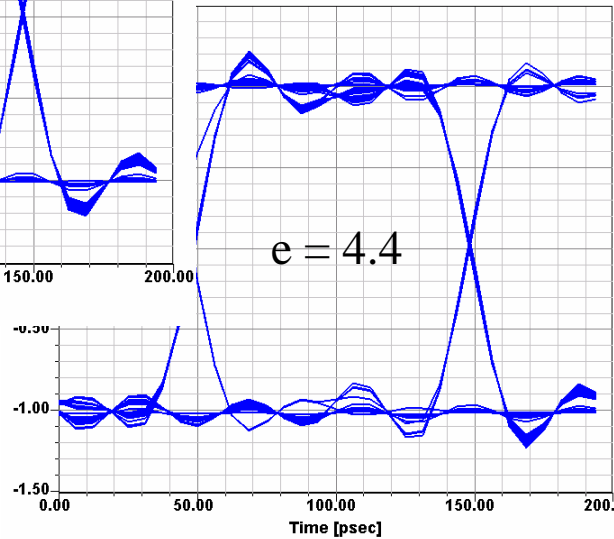
Time Domain Response as a Function of Material Variation



Eye Diagrams of Material Study

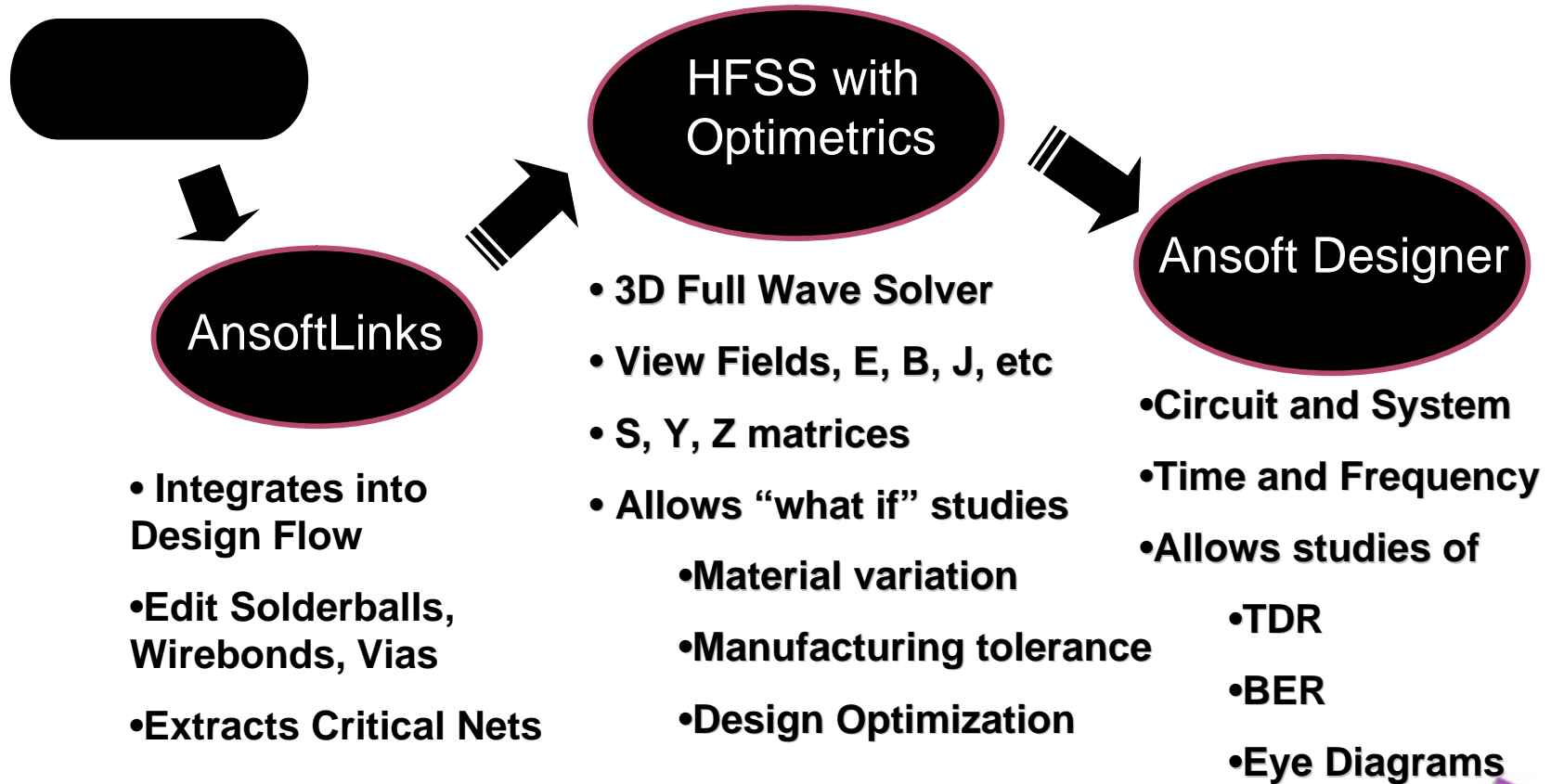


Study



Conclusions (1)

Design Flow



Conclusion (2)

Understanding Frequency and Time Domain Responses

- Combination of AnsoftLinks, HFSS and Ansoft Designer allows for a complete understanding of package.
- Solution provides ability to “hook into” an existing design flow
- Analyze a package in the frequency domain using HFSS then investigate the time domain behavior in Ansoft Designer.
- Eliminates issues of different software vendors, loss of time for translation, and high prototyping cost of the design cycle. This will enable an engineer to....

