Interdigitated Capacitor

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Outline

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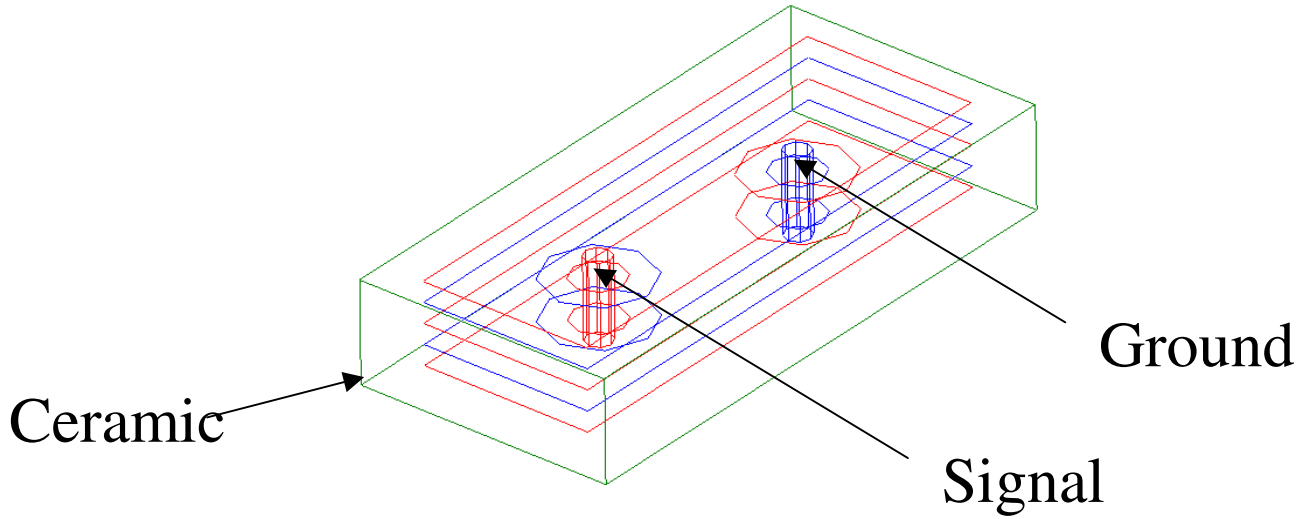
- Manufacturing
- Characteristics
- Methodology
- Results
- Future work
- Conclusion
- Acknowledgment

Why Interdigitated Capacitor?

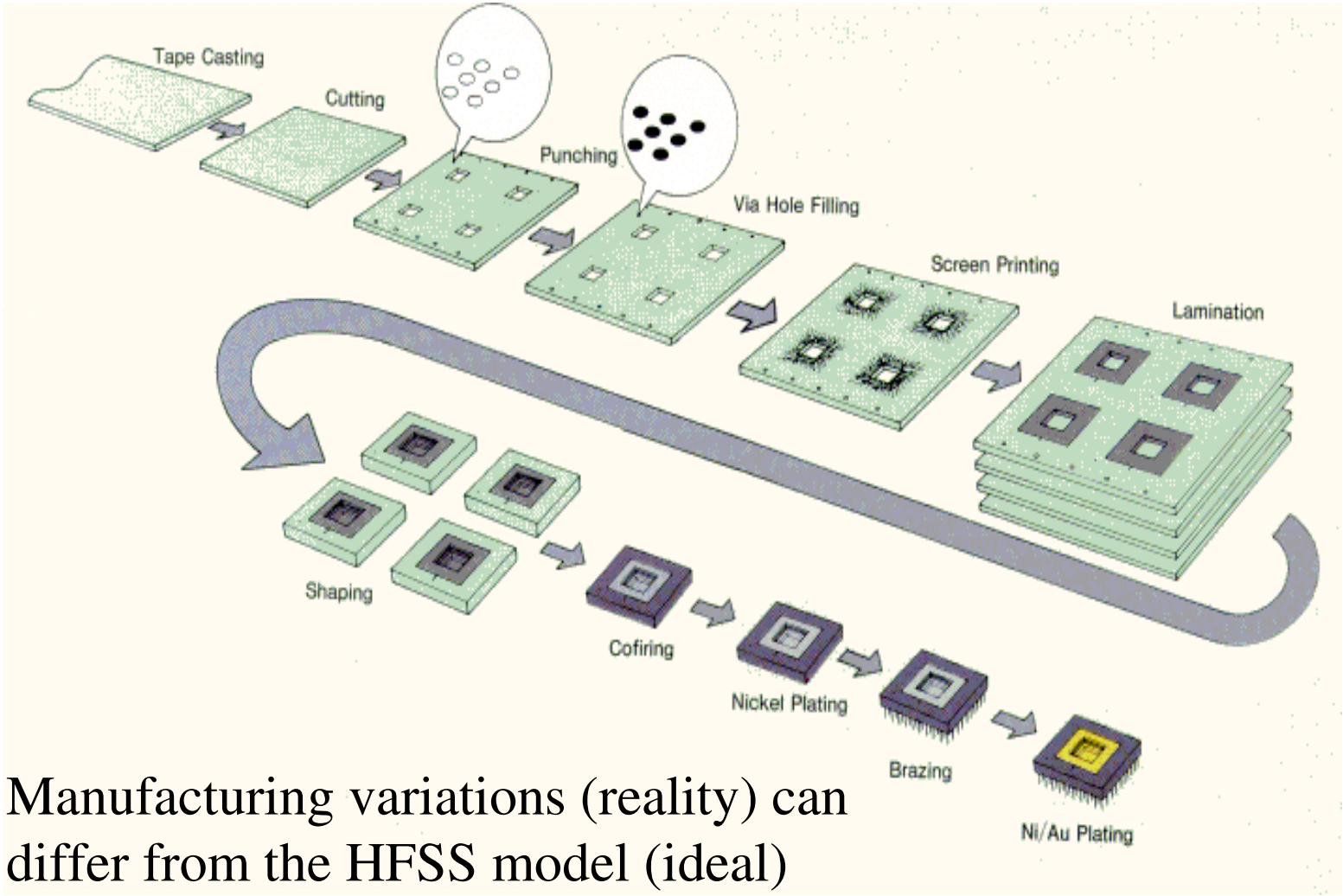
- Wire bonds
- Discrete components
- Cost factor (Assy cost)
- Size factor (too much space)
- Consistency problem because L is proportional to wirebond length

Package



- Simplified illustration of a more complicated Multi-Layer package
- Can't use simple equation because of fringing and vias
- Need to use HFSS

Manufacturing

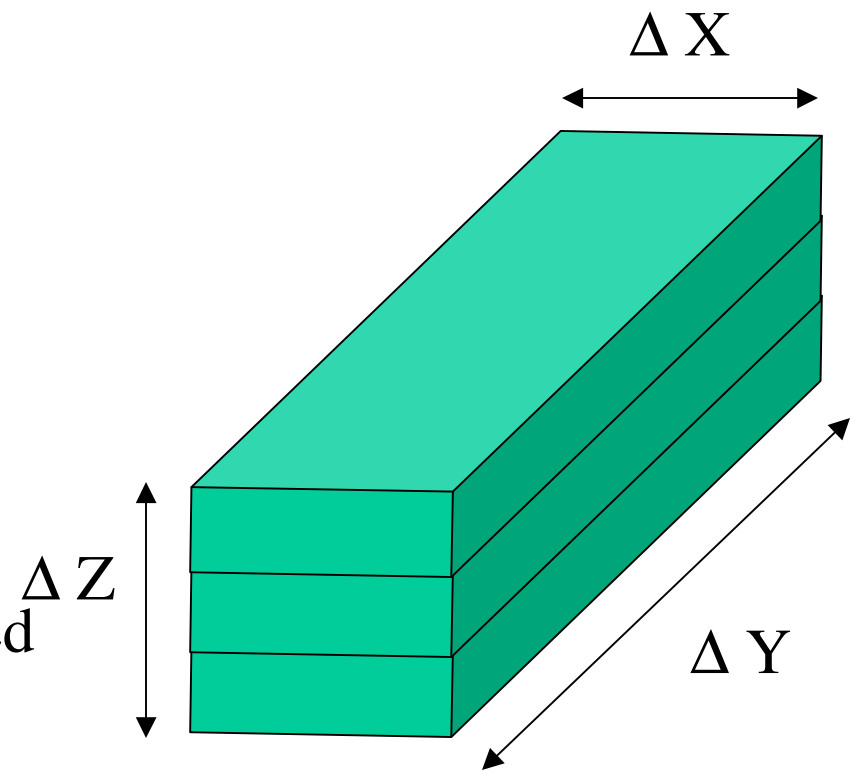


Manufacturing variations (reality) can differ from the HFSS model (ideal)

Ceramic Shrinkage

- Ceramic shrinks because of firing
  - Δ X ~ 15% +/- x
  - Δ Y ~ 15% +/- y
  - Δ Z ~ 20% +/- z

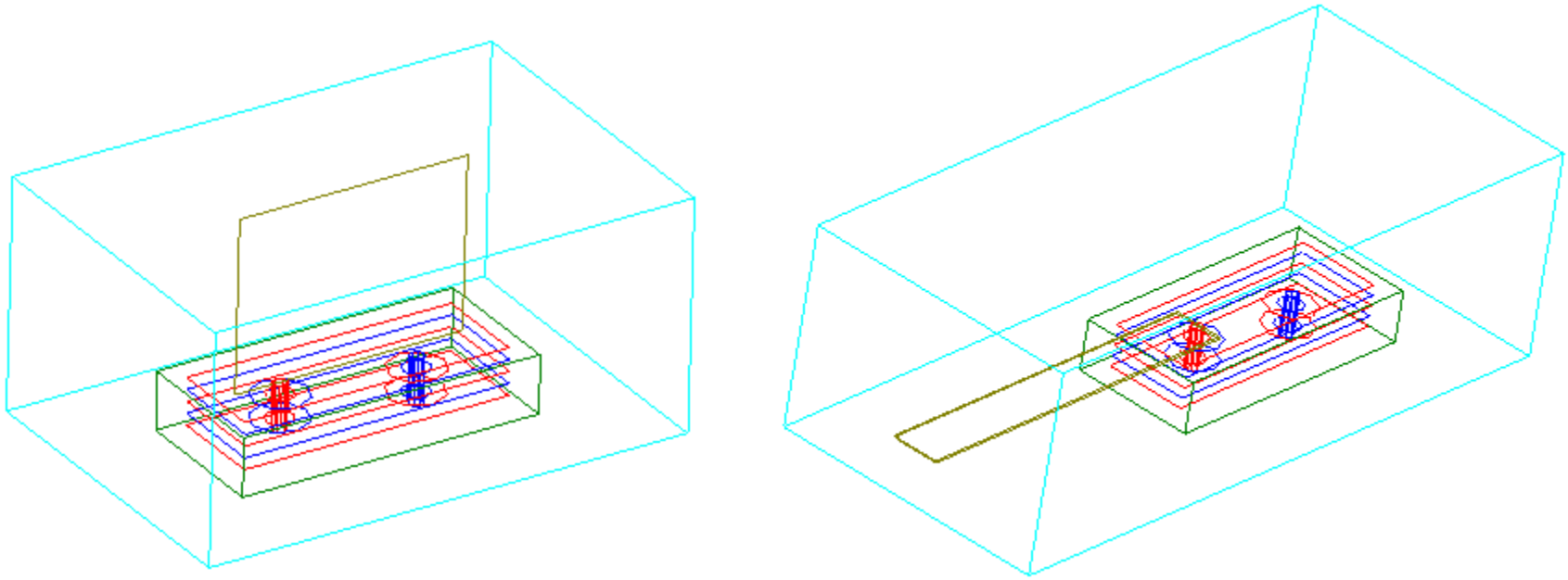
Shrinkage is accounted for, but there is a tolerance associated with shrinkage



Characteristics

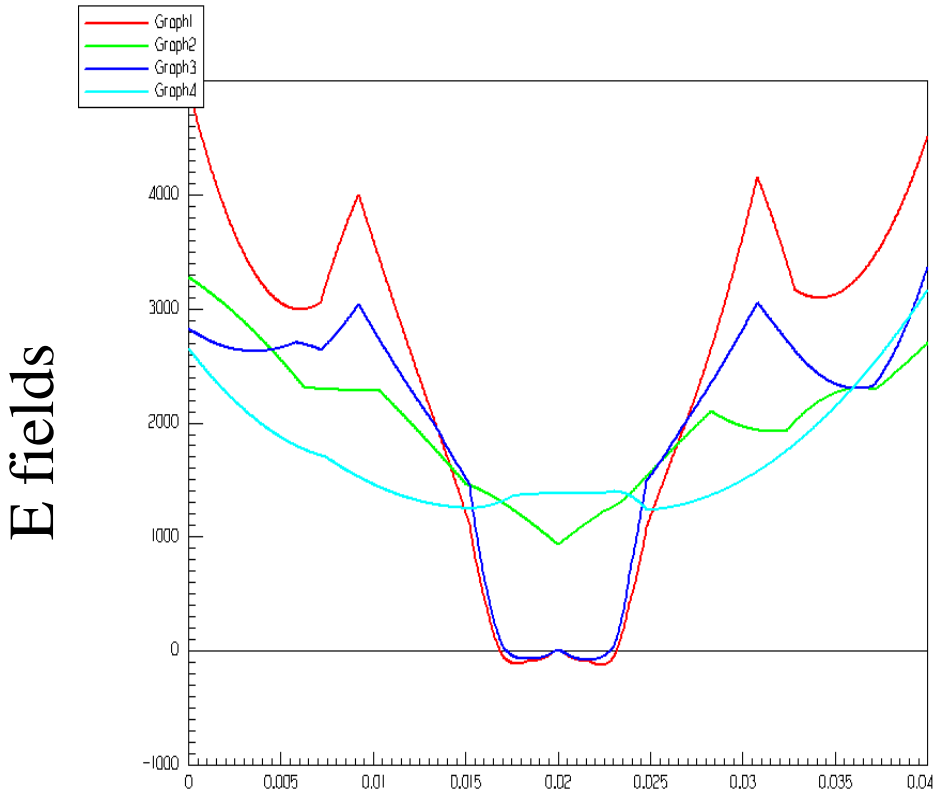
- Frequency= L - band
- Large Capacitor = A pF
- Small Capacitor = B pF
- Tolerance = 3%
- Max volume requirement of
  - large capacitor = $X_a Y_a Z_a$
  - small capacitor = $X_b Y_b Z_b$

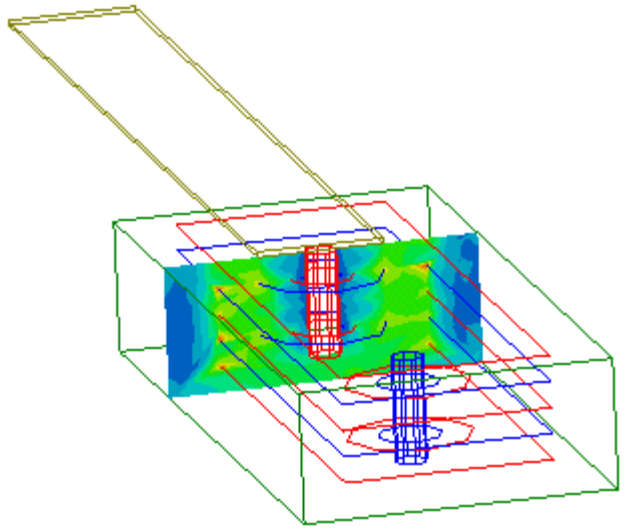
Launch



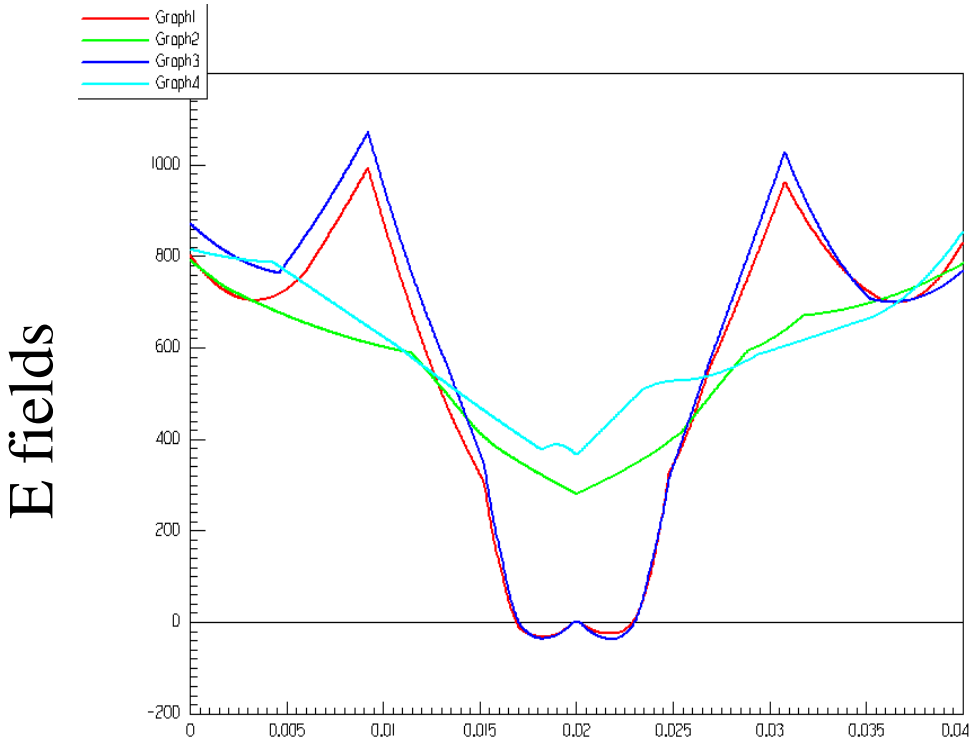
- Stripline launch
- Lead (side) launch
- Same result-No difference in HFSS work

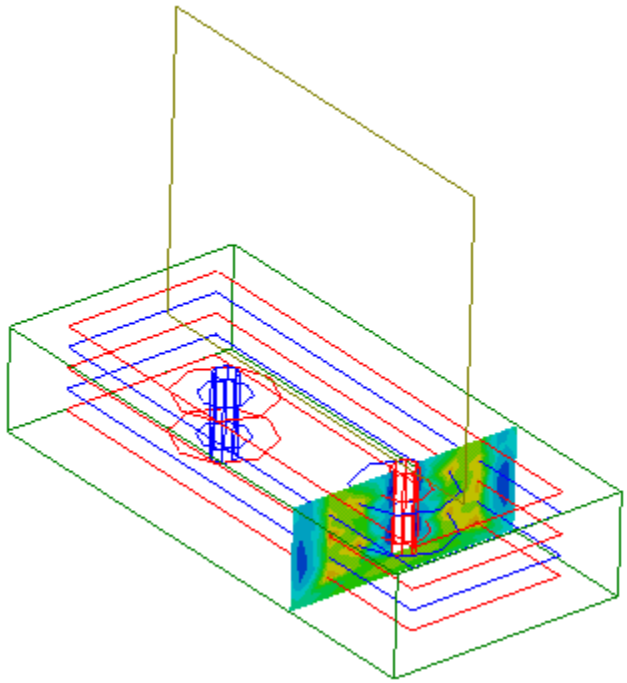
Lead launch


Graph1
Graph2
Graph3
Graph4
4000
3000
2000
1000
0
-1000
0
0.005
0.01
0.015
0.02
0.025
0.03
0.035
0.04
E fields
Distance

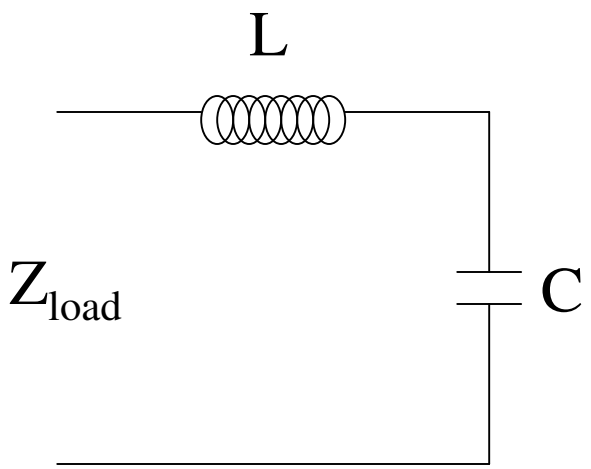


Stripline launch





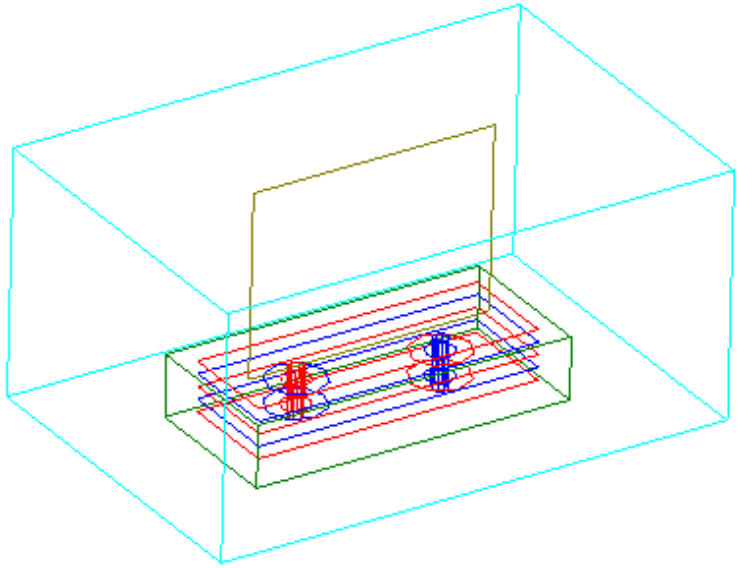
Circuit Model



- Total Impedance of a circuit is the sum of
  - Capacitor Impedance
  - Inductor Impedance

Methodology

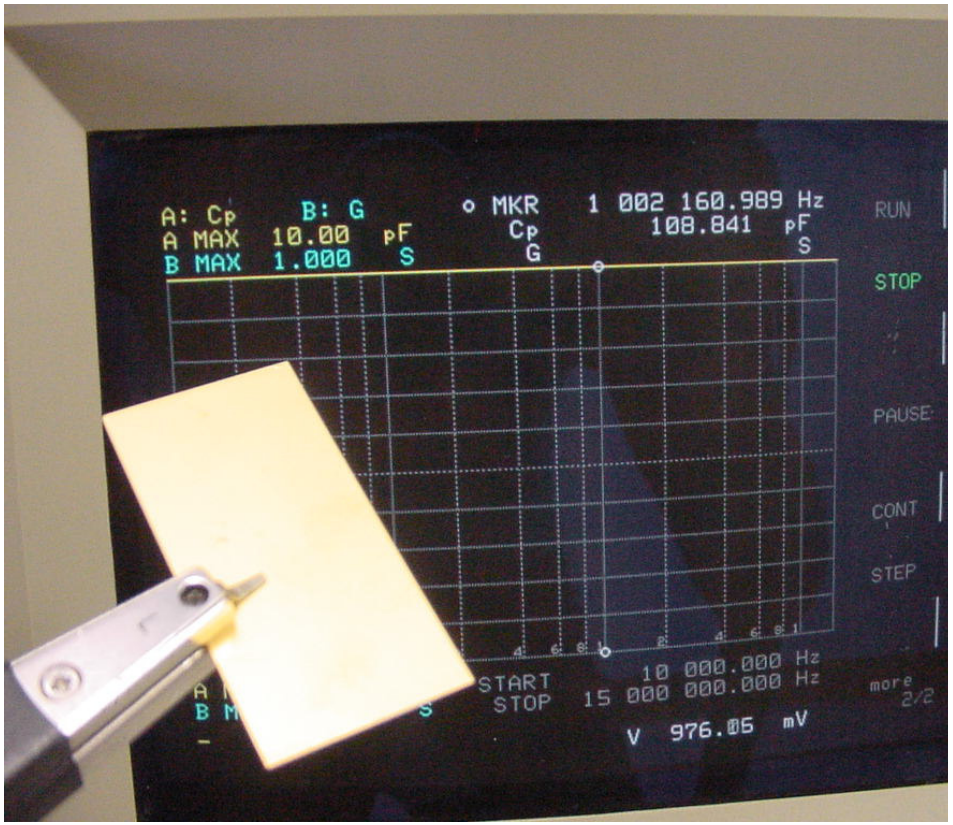
- Using Ansoft HFSS:
  - De-embed to the start of the capacitor
  - Extract the Characteristic Impedance and the Scattering parameters $\Gamma(\omega)$
  - Calculate Z_{load}
  - Calculate C & L at two different frequencies using two equations with two unknowns



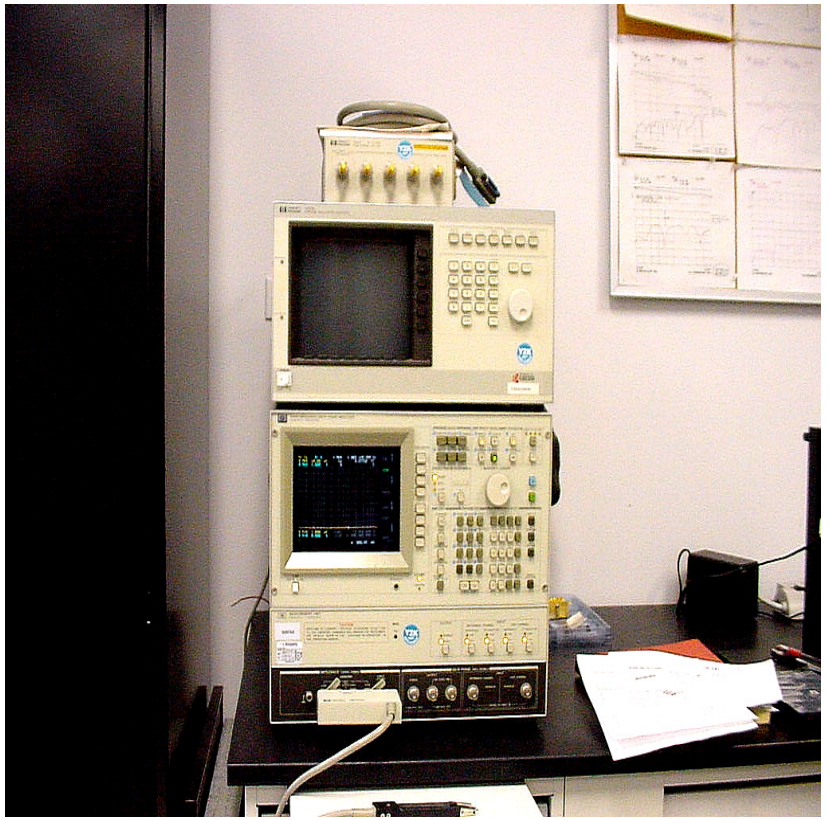
Manufacturing Considerations

- Match overall size
  - Heat sink set
  - Lead frame set
  - Depth set
  - Can’t add or take out layers
- Ceramic tape size is fixed
  - Manufacturers tape thickness is 5 mils or thicker, discrete
- Matching print patterns to reduce cost

Measuring Equipment



Test probe shown measuring a parallel plate capacitor



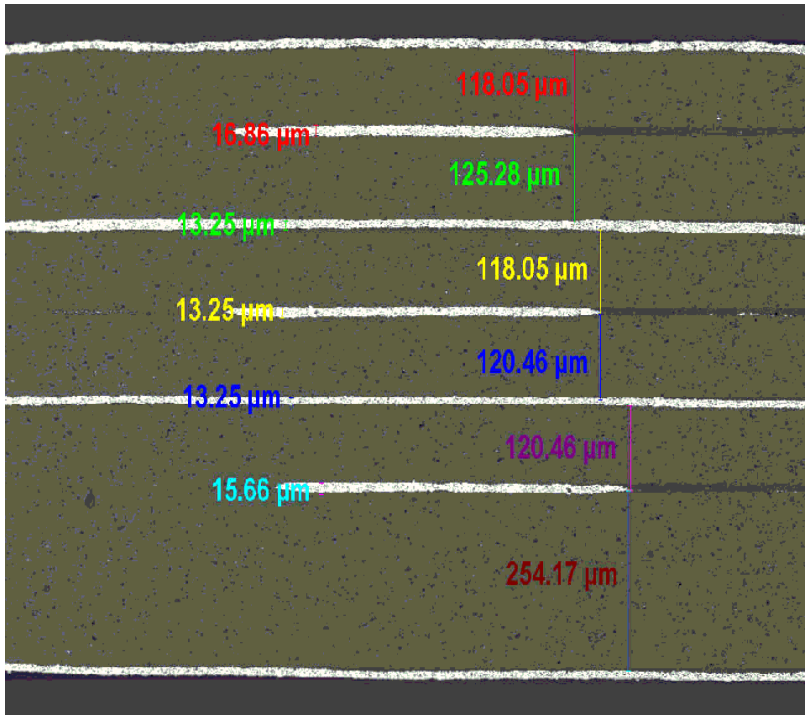
HP Analyzer (4194A)

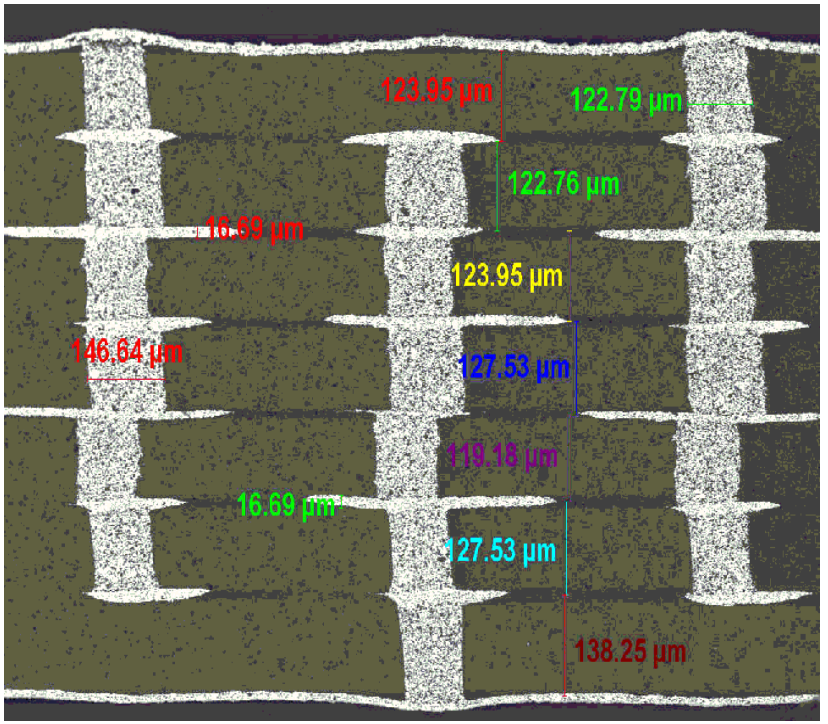
Results 1

- First manufacturing attempt was within **4%** of theoretical values
- Cross-sectioned to validate methodology
- The values of the capacitance were high due to variations in Dielectric thickness
  - Dielectric tape on the thin side
  - Firing ceramic causes shrinkage
  - Capacitor value is inversely proportional to the thickness

Actual Variation in Thickness

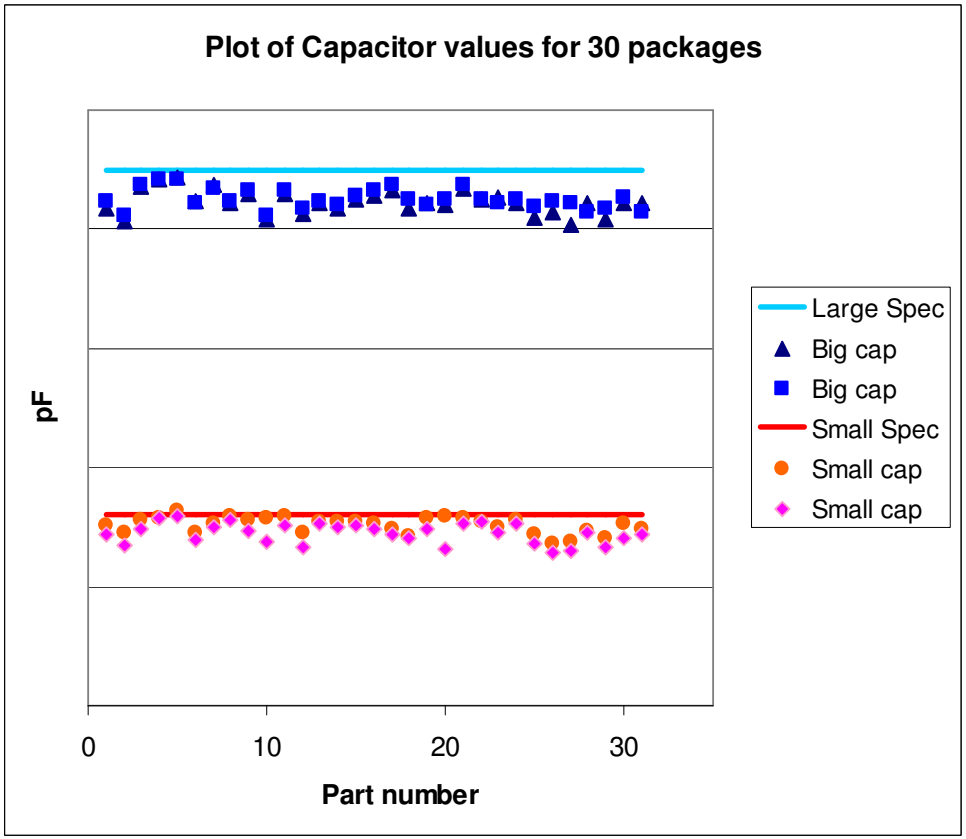
- Thickness differences from two sources
  - Layers on the thin side (4.3 – 4.7 mils Vs. 5 mils)
  - Thickness of metallization not considered (=> Thickness of Dielectric material variation in the same layer)





Results 2

- Averaged the actual thickness and used that value to re-simulate the capacitor model
- Used appropriate ε_r
- Capacitor values were within **0.2%** of simulated models with average cross-sectioned thickness



Future Work

- Customer used fixture when measuring the capacitors(fixture adds more capacitance)
  - Higher capacitance values (1.2pf in both cases)
- Kyocera plan
  - Model the fixture
  - Correlate to customer's measured data
  - Meet customer specifications by less than 1%

Conclusions

- Capacitance values meet designed targets
  - Slightly low trend (within 1%)
- Correlation between HFSS simulation and measurement is excellent if the model and the built package is the same

Acknowledgment

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- Mario Aquino
  (Analysis)