The Role of Monolithic Transmission Lines in High−Speed Integrated Circuits

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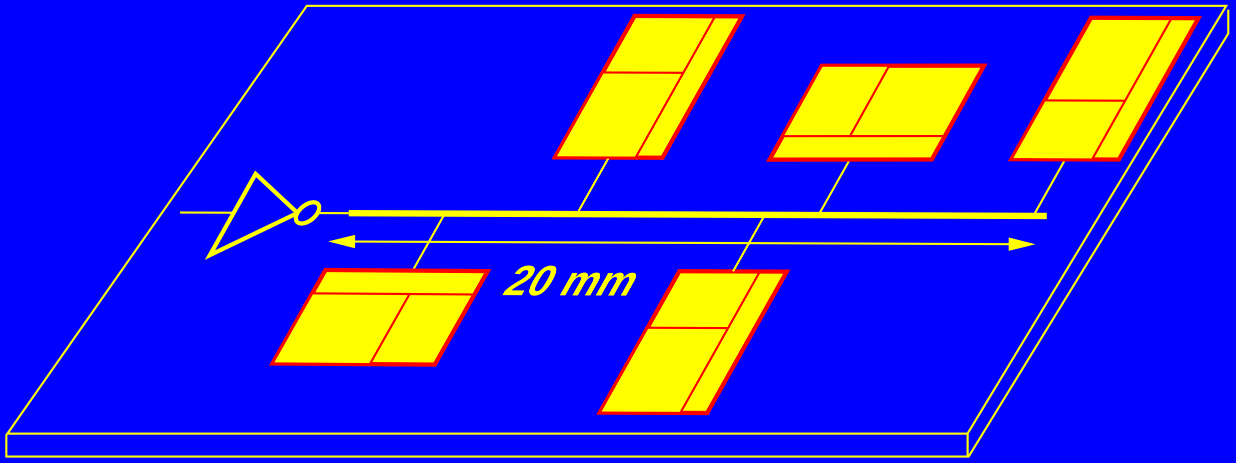
Outline

- Introduction
- T Lines in CMOS Technology
- Modeling Issues
- T Lines as Circuit Elements
- Circuit Applications
- Conclusion

Motivation

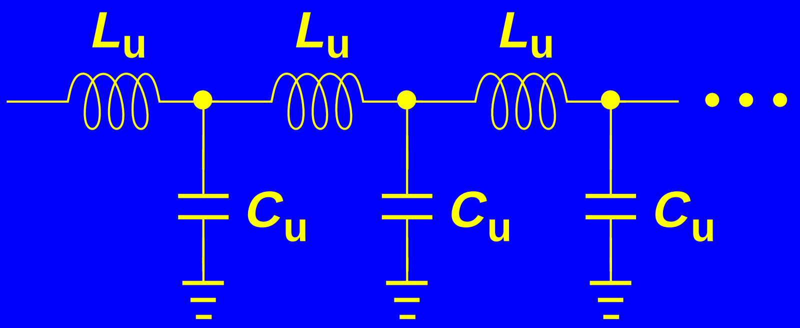
- Chip dimensions are increasing:



- Data rates are rising: at 40 GHz, the wavelength is about 6 mm.
- Both skin effect in interconnects and substrate resistance impact the performance.
- Dielectric loss may also manifest itself at high frequencies.

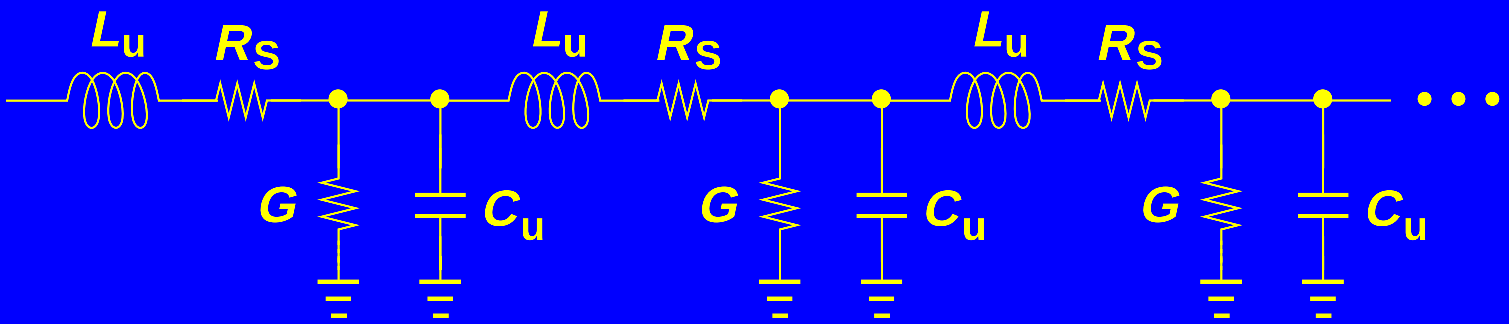
Five–Minute Review of T Lines

Ideal T Line



$$Z_0 = \sqrt{\frac{L_u}{C_u}} \qquad v = \frac{1}{\sqrt{L_u C_u}}$$

Lossy T Line



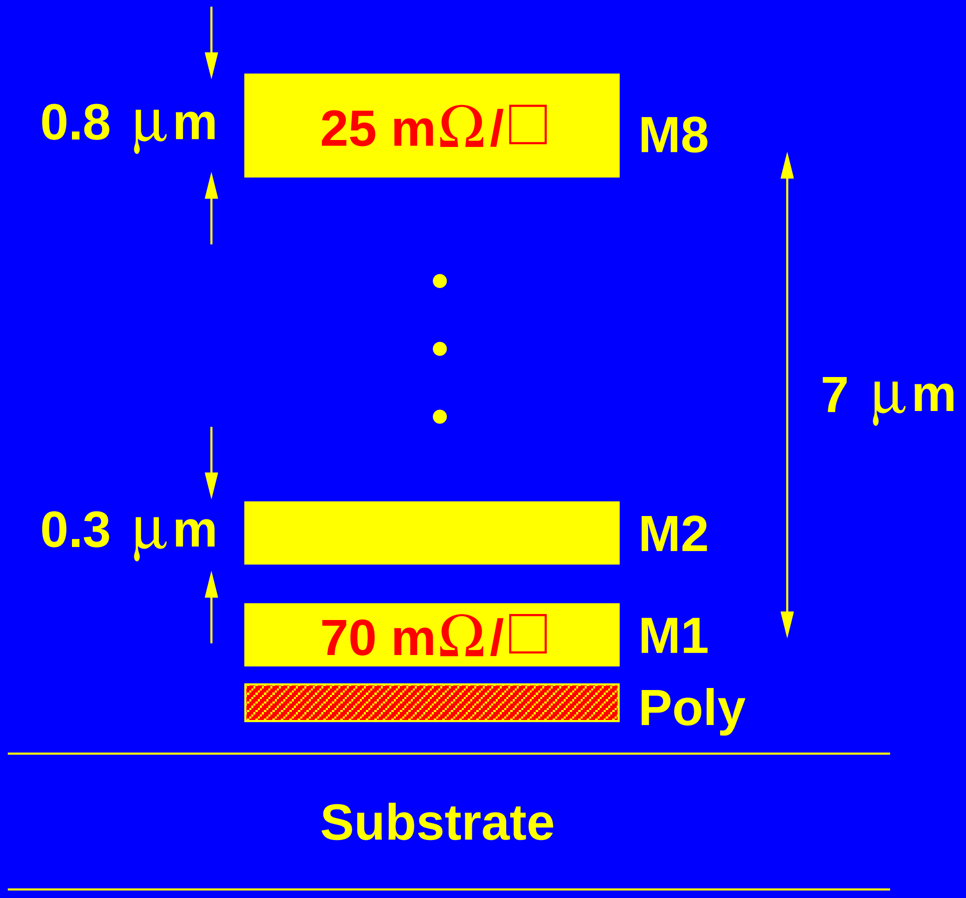
$$Z_0 = \sqrt{\frac{R_S + j\omega L_u}{G + j\omega C_u}} \qquad V(x) = V_0\, e^{-\alpha x} \cos(\omega t - \beta x)$$

$$\alpha = \frac{1}{2}\left(\frac{R_S}{Z_0} + G Z_0\right)$$

Important T Line Parameters

- Inductance
- Capacitance
- Loss
- Wave Velocity
- Field Confinement

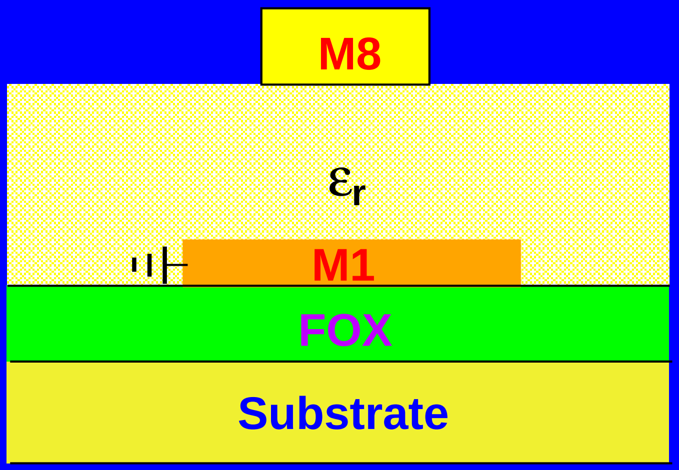
Backend of Typical CMOS Technology



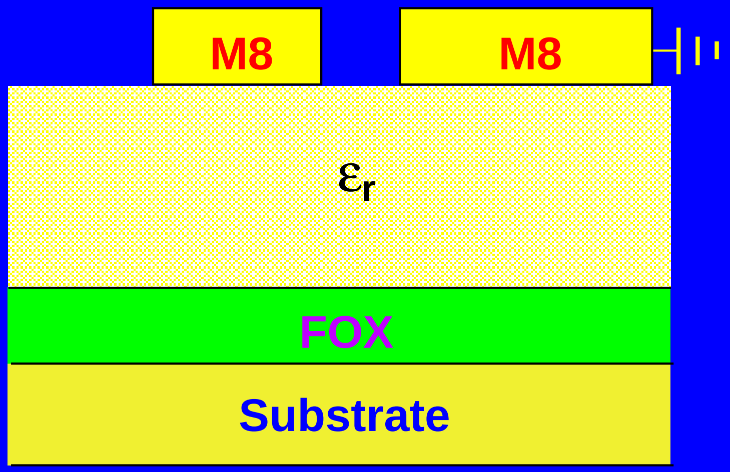
- **Eight metal layers allow many new passive device structures.**

Monolithic T Line Structures

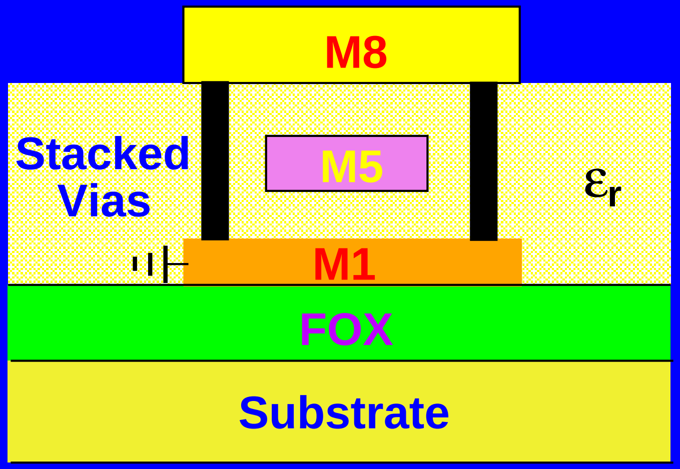
Microstrip Line



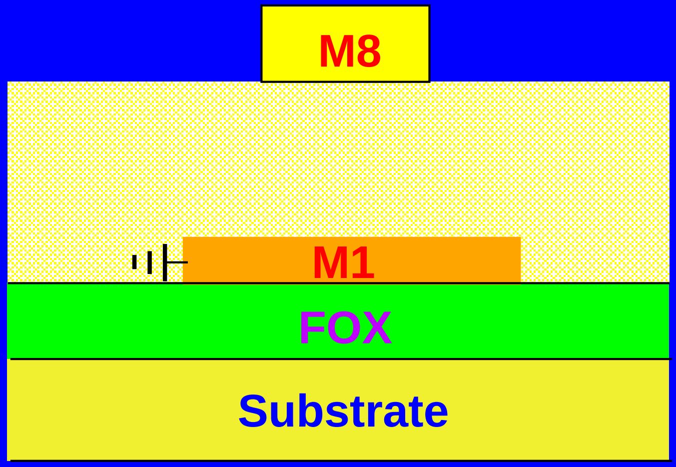
Coplanar Line



Stripline

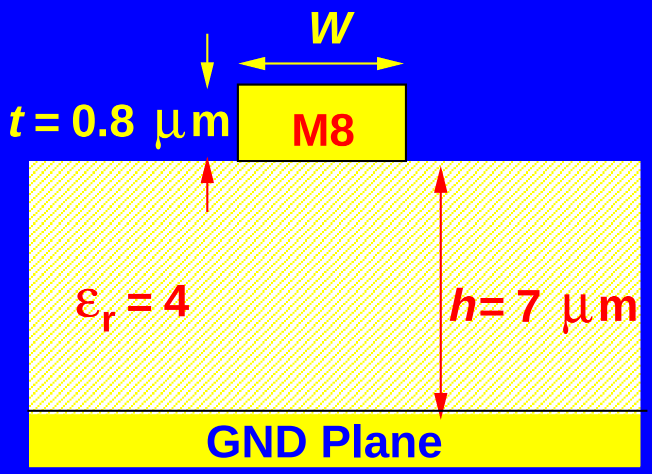


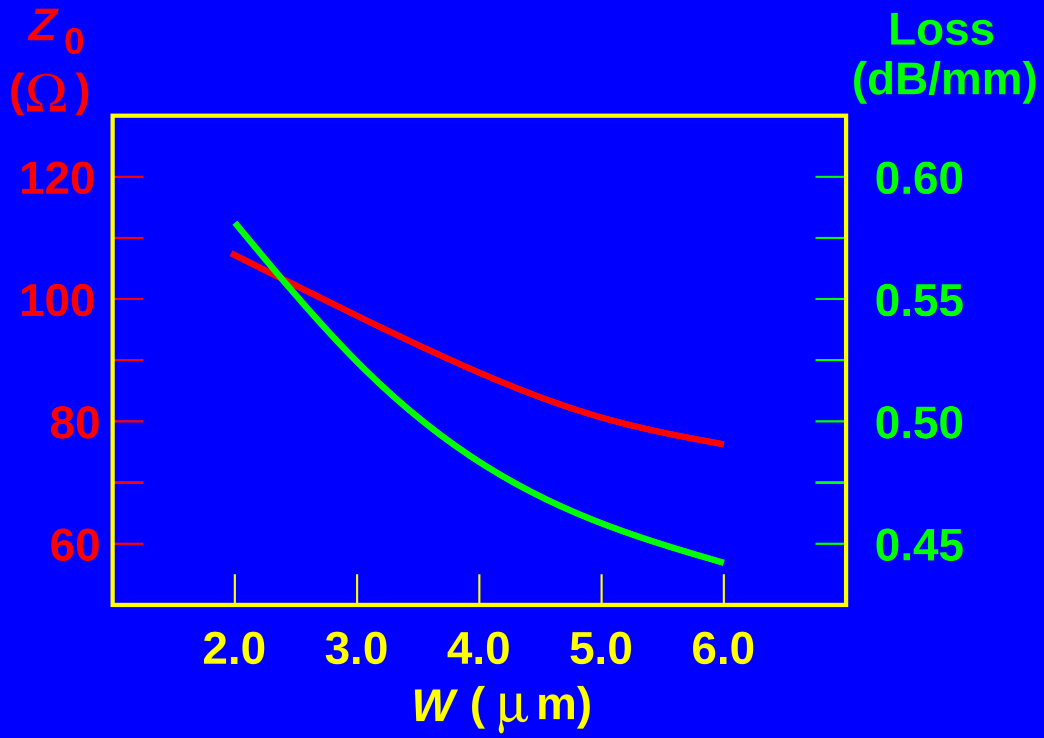
Microstrip Line



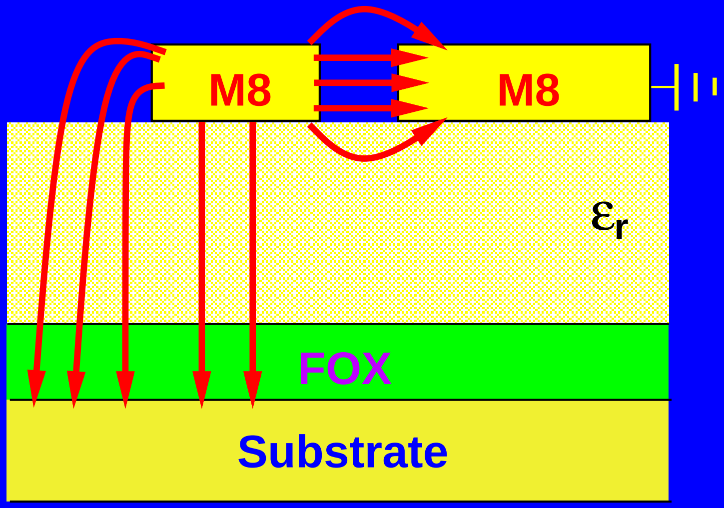
- ❐ Moderate Inductance
- ❐ Moderate Capacitance
- ❐ Low Loss
- ❐ Reasonable Field Confinement

Example: Performance at 40 GHz



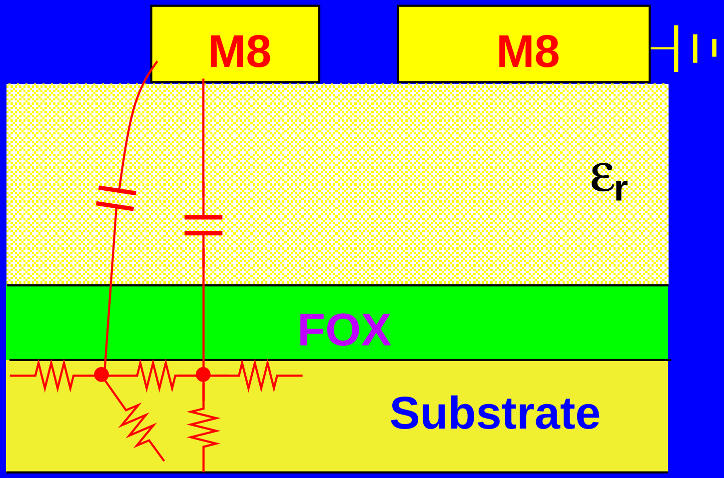


Coplanar Line

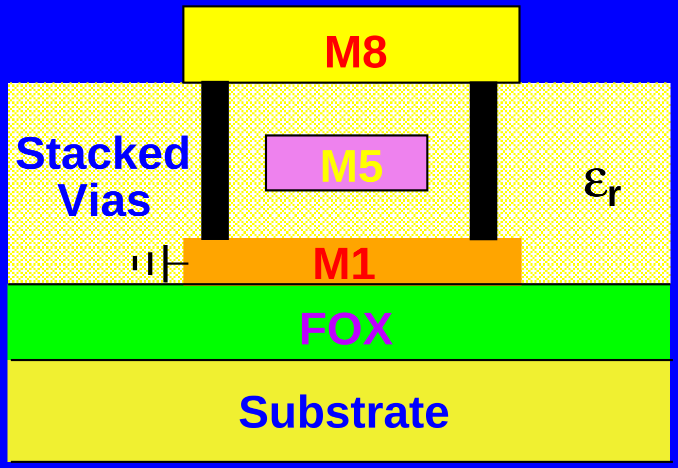


- ❒ Moderate Inductance
- ❒ Low Capacitance
- ❒ Higher Loss
- ❒ Poor Field Confinement

Substrate Coupling:



Stripline



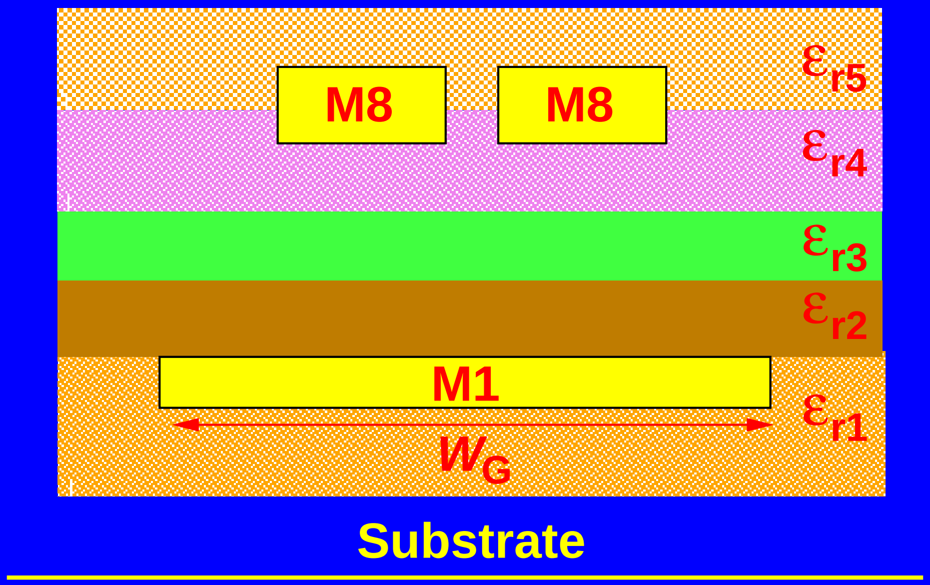
- Moderate Inductance
- High Capacitance
- Low Loss
- Good Field Confinement

Modeling Issues

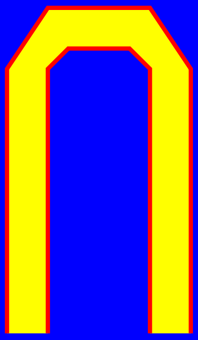
- Discrepancies Among Field Solvers
- Limited Capabilities of Field Solvers
- Circuit Models
- Skin Effect

T Line Complexities

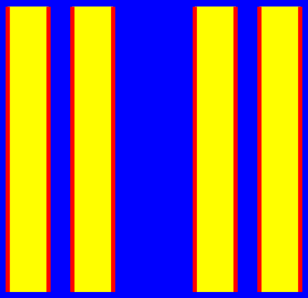
Differential Lines



Bends

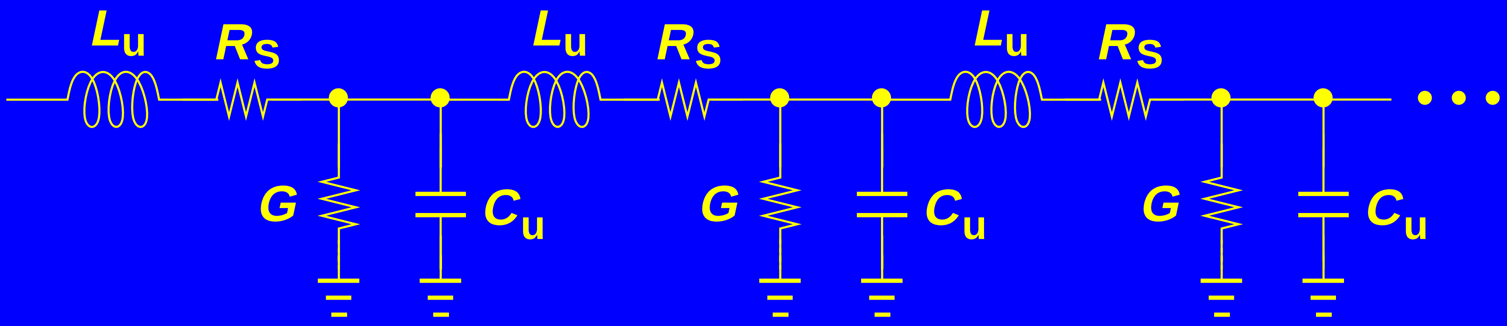


Double Differential Lines

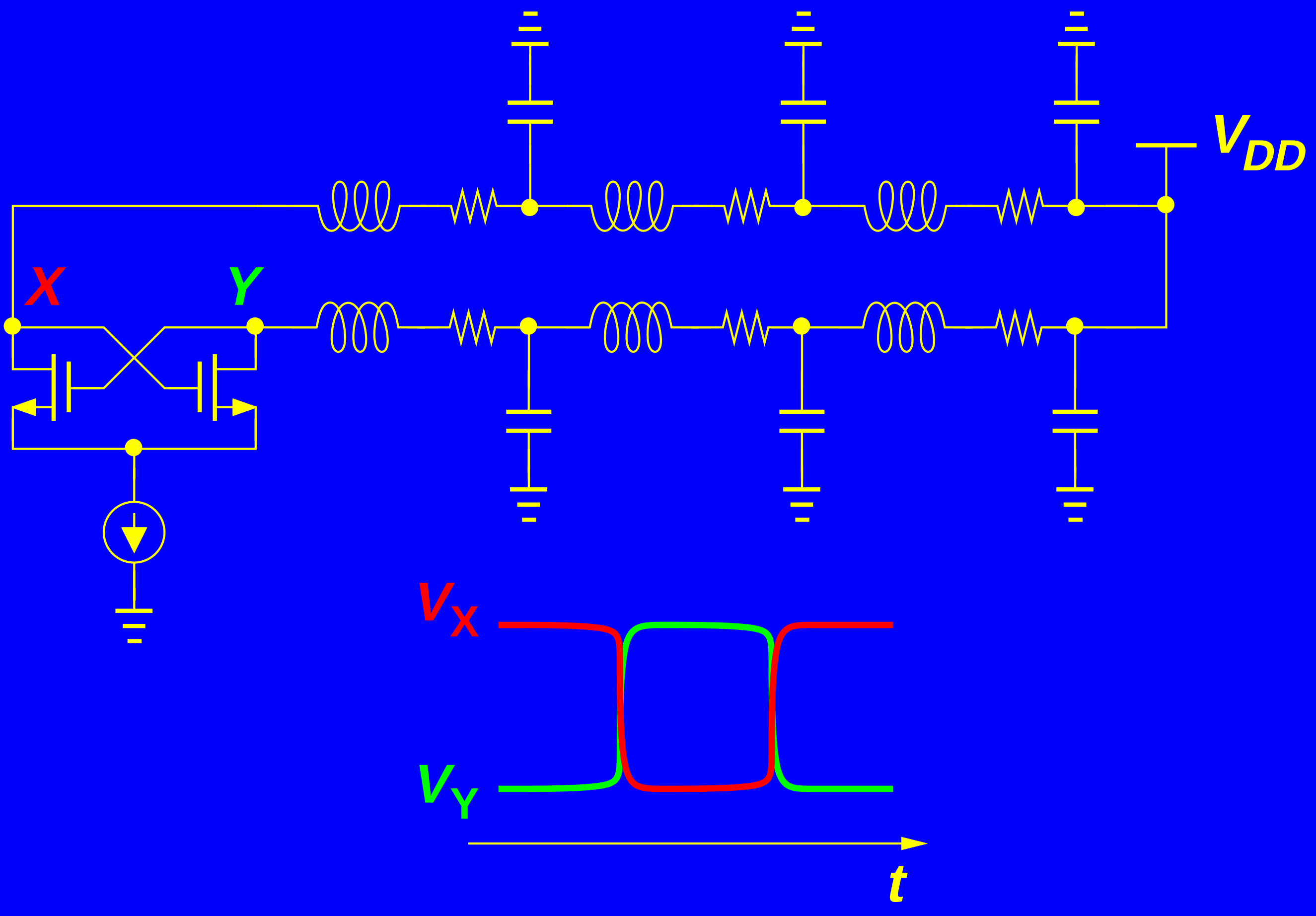


Circuit Modeling

- ❐ T line models in circuit simulation programs are still quite inadequate.
- ❐ Circuit models of T lines can provide greater insight and simulation flexibility.
- ❐ Standard model assumes constant loss and is only suited to narrowband circuits:



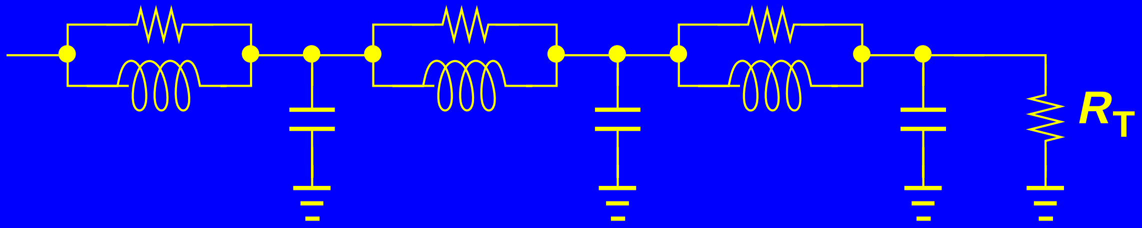
Example of Modeling Problem



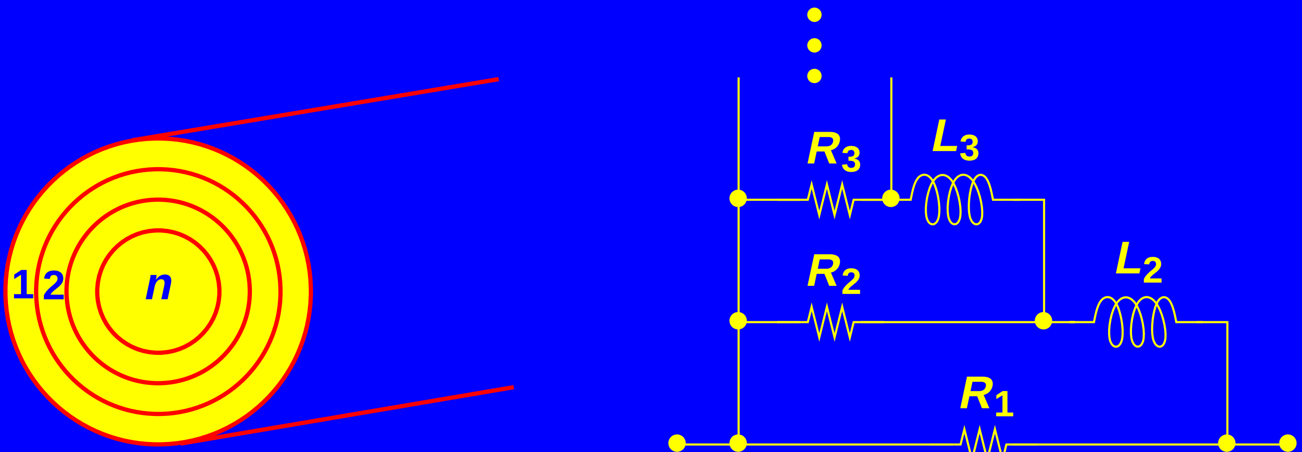
- Need a broadband model even for some narrowband circuits.

Broadband Model

- Modeling loss as a parallel resistance fails to include low−frequency wire resistance:

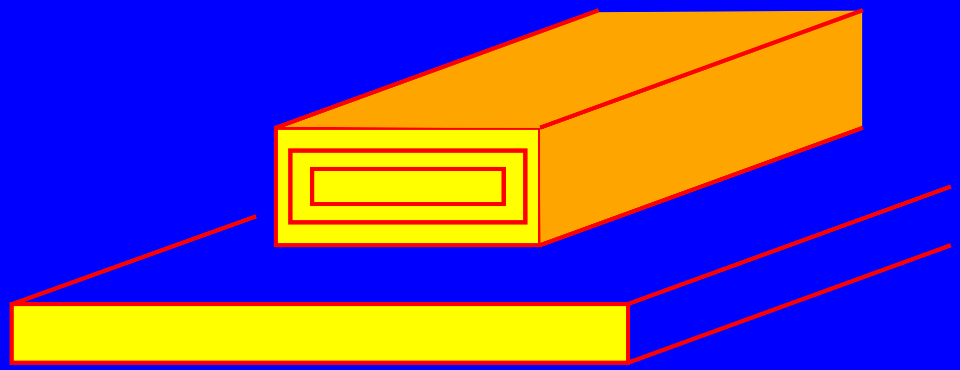


- Broadband skin effect modeling:



Ref. [4]

Application to Microstrips



- Need to compute inductance and resistance of rectangular pipes atop a ground plane.

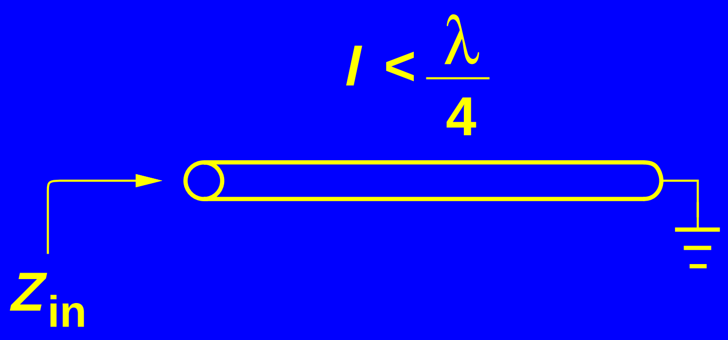
T Lines as Circuit Elements

- Small Inductors
- Controlled−Impedance Interconnects
- ESD Protection

Small Inductors

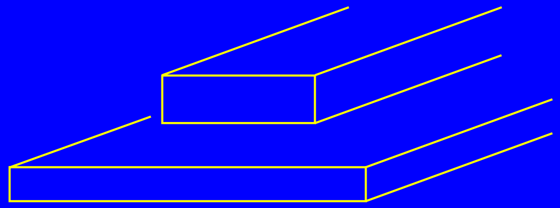
$$Z_{in} = Z_0 \tan \frac{2\pi}{\lambda}$$

$$L_{eq} \approx \frac{Z_0 \cdot l}{v} \approx L_u \cdot l$$



$$l < \frac{\lambda}{4}$$

Microstrip Example:

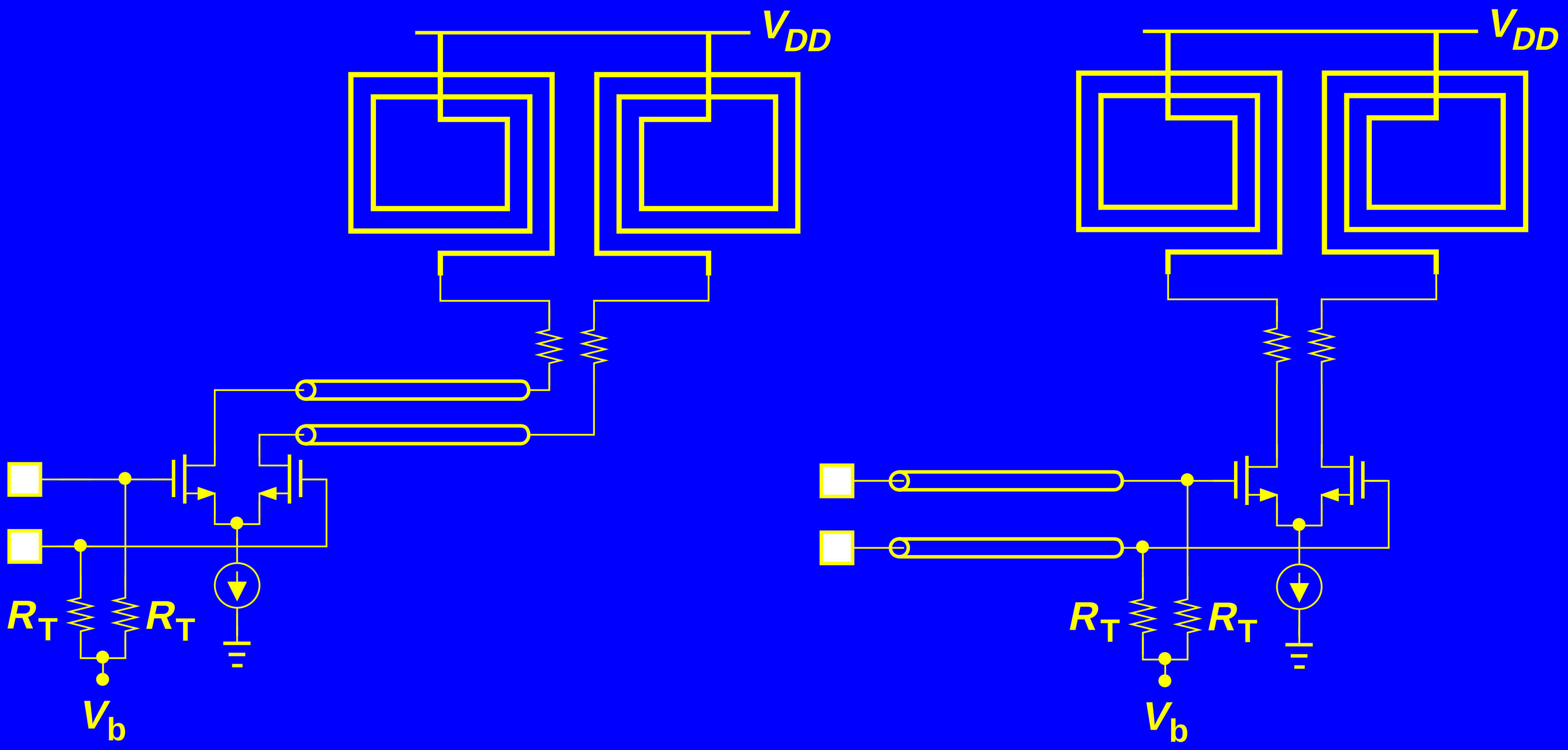


$$W = 3\ \mu\text{m},\ l = 1\ \text{mm} \Rightarrow L_{eq} = 0.523\ \text{nH}$$

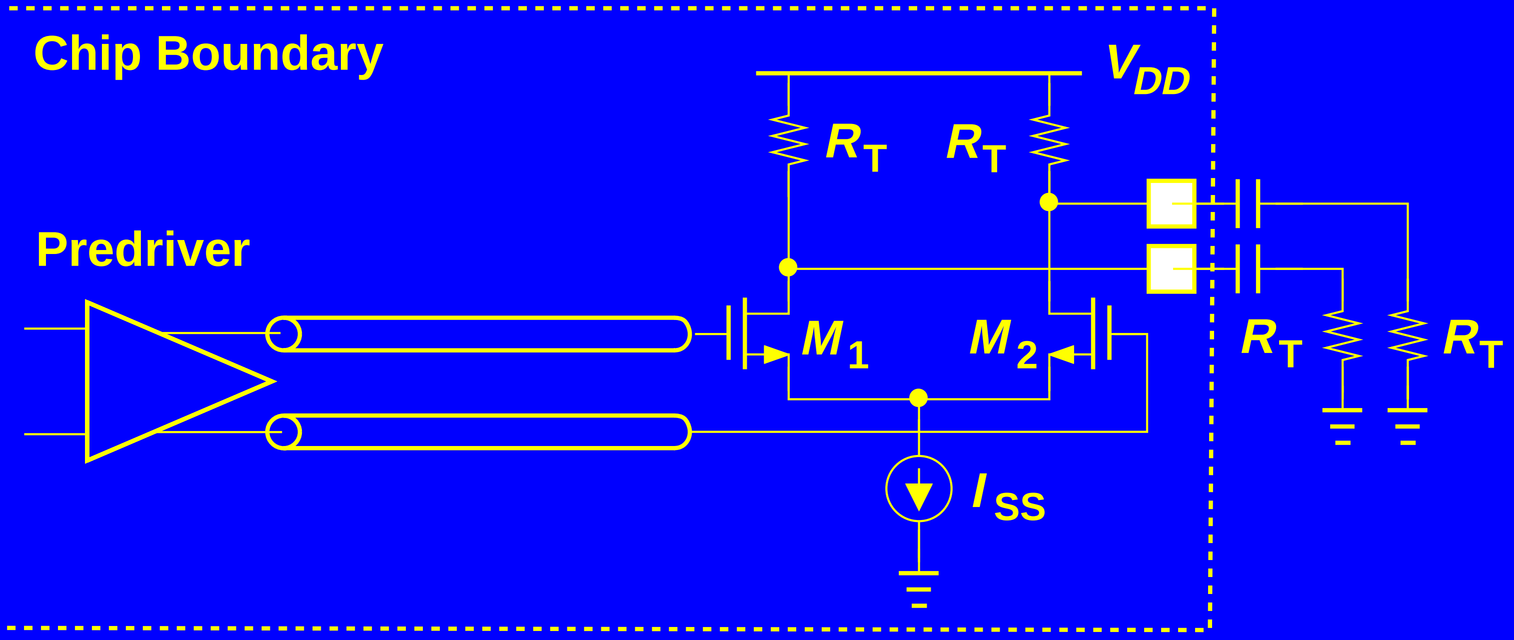
$$Q = 14\ @\ 40\ \text{GHz}$$

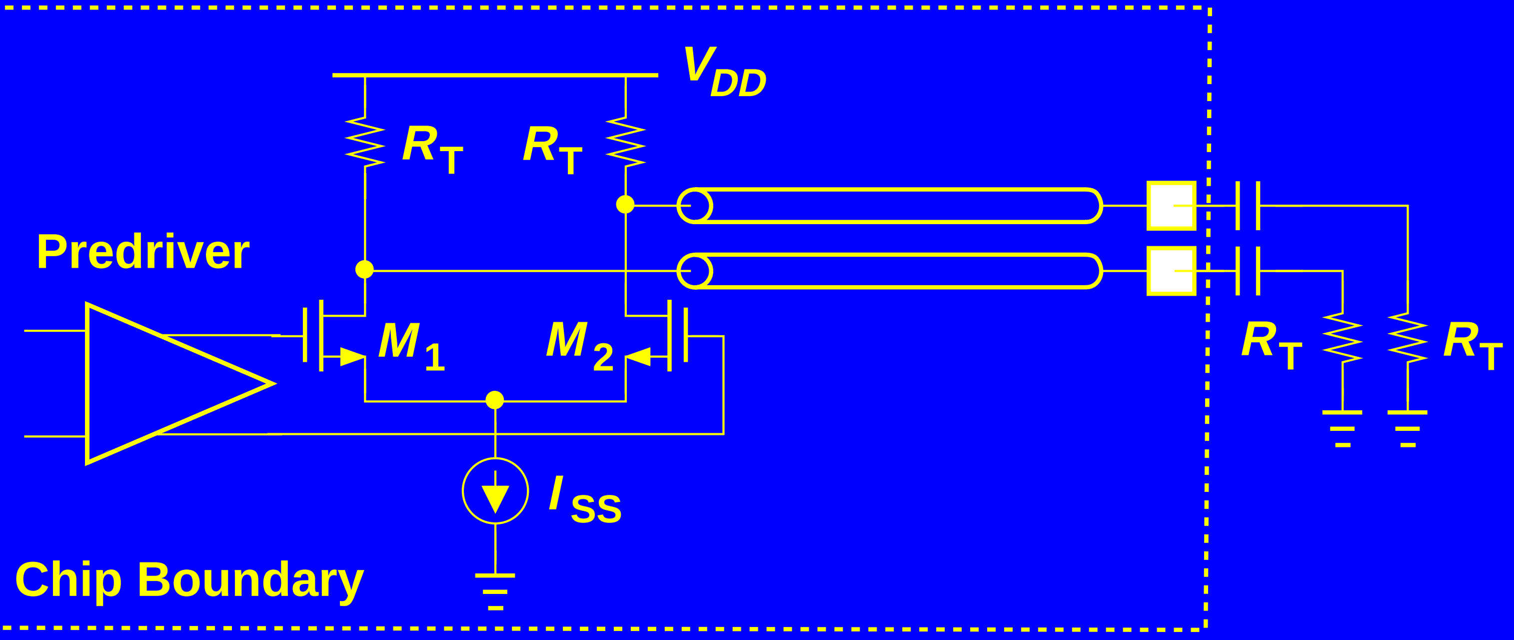
- ❐ Microstrips produce small substrate currents and their parameters can be calculated more accurately than those of spiral inductors.

Controlled–Impedance Interconnects (I)

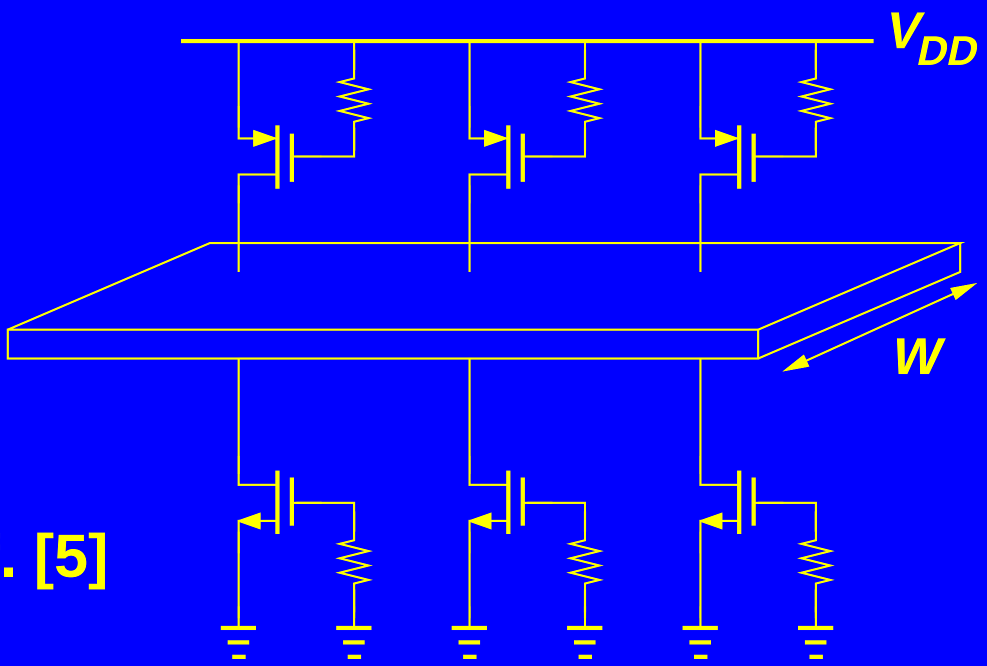


Controlled–Impedance Interconnects (II)





ESD Protection



Ref. [5]

Example:

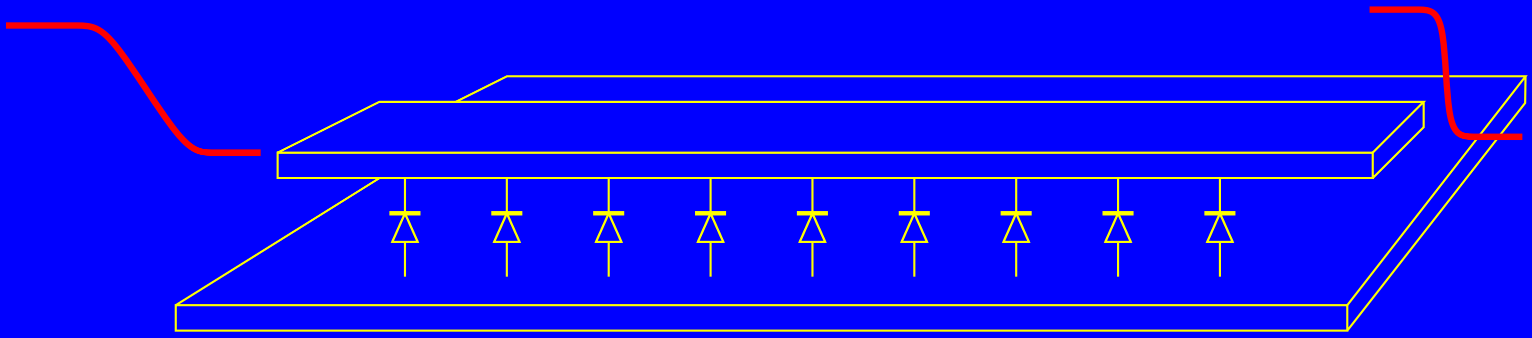
$W = 3\ \mu\text{m},\ Z_0 = 50\ \Omega \Rightarrow C_{ESD} = 250\ \text{fF/mm}$

- T Line may need to be long, occupying large area and introducing substantial loss.
- Junction diodes of MOSFETs introduce additional loss.

Circuit Applications

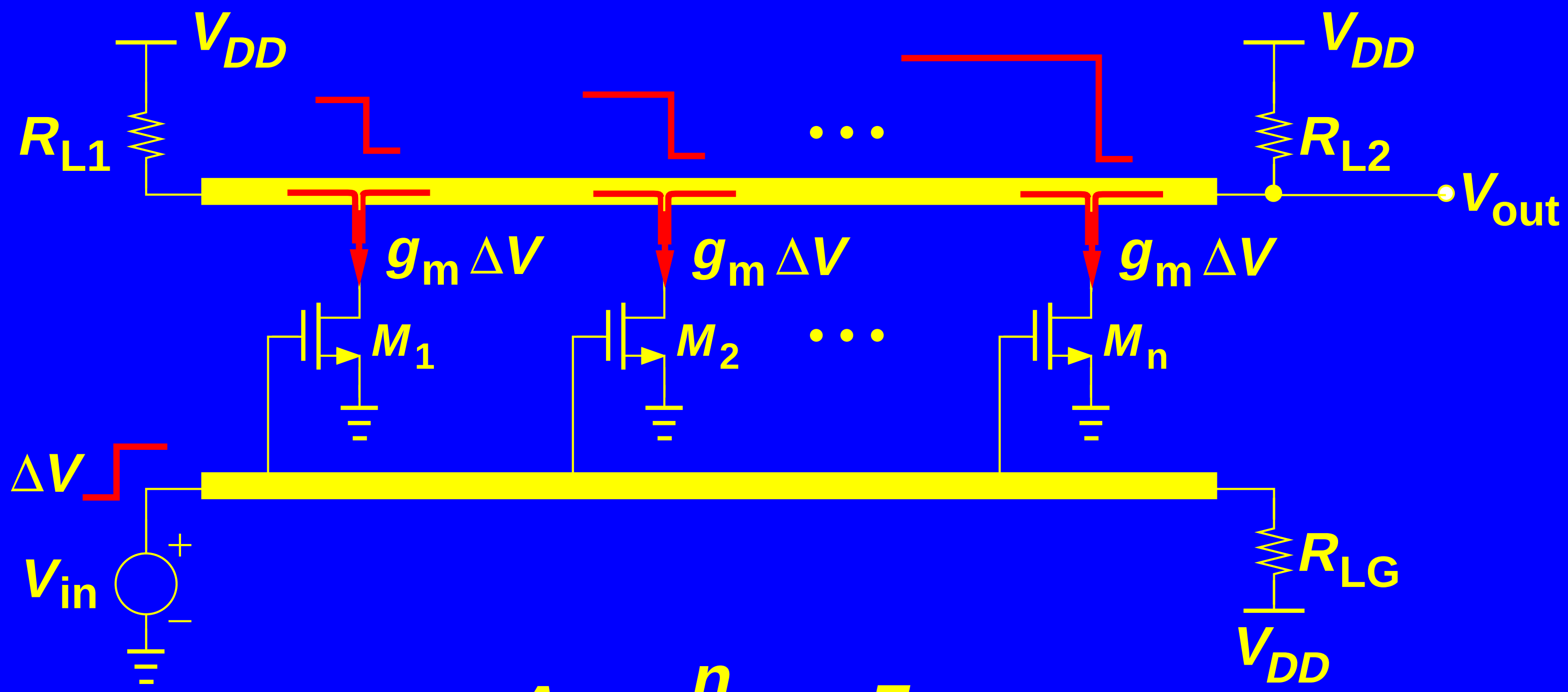
- ❐ Pulse−Sharpening Circuits
- ❐ Distributed Amplifiers
- ❐ Distributed Oscillators
- ❐ Rotary Oscillators

Pulse Sharpening



- Can produce picosecond rise times in CMOS.
- Application in high−speed sampling of analog and digital signals.
- But, the rise time becomes longer.

Distributed Amplifier



$$A_v = \frac{n}{2} g_m Z_{0L}$$

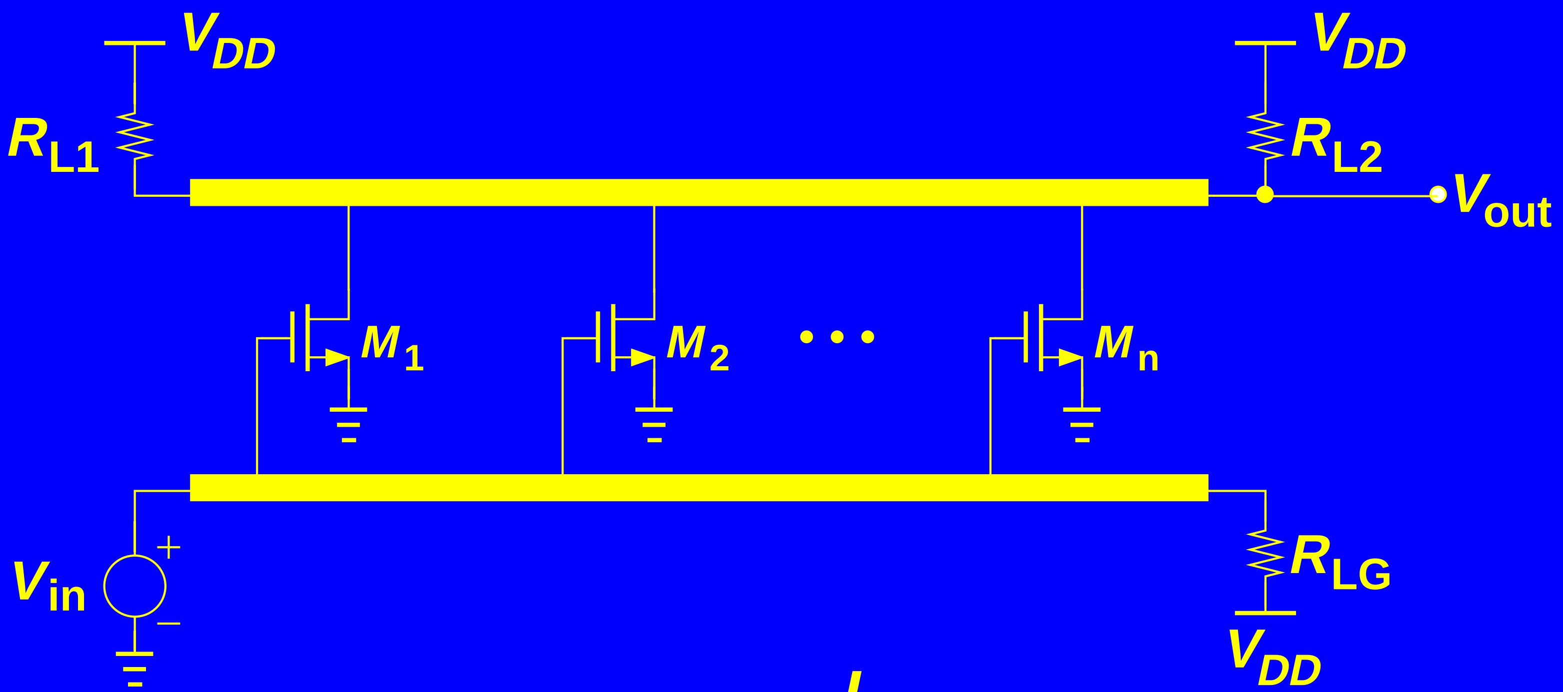
If line capacitance and loss are negligible:

$$A_v = \pi f_T \frac{l}{v_{0L}}$$

Design Issues

- Voltage Headroom
- Loss in Input and Output T Lines
- Output Resistance of MOSFETs
- Miller Multiplication of C_{GD}
- Input Impedance

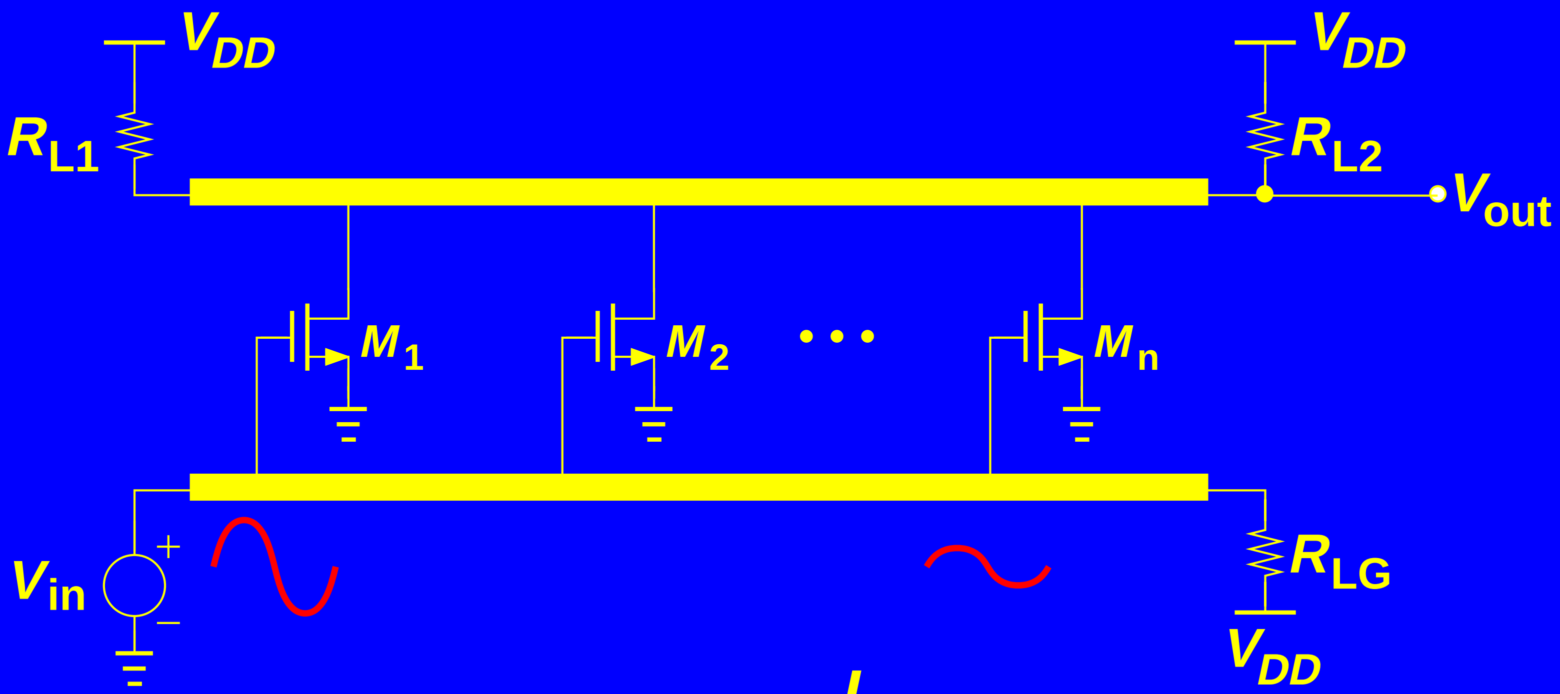
Voltage Headroom



$$A_v = \pi f_T \frac{I}{V_{0L}}$$

- Maximum f_T requires large overdrive voltage.
- Maximum I requires large bias current.

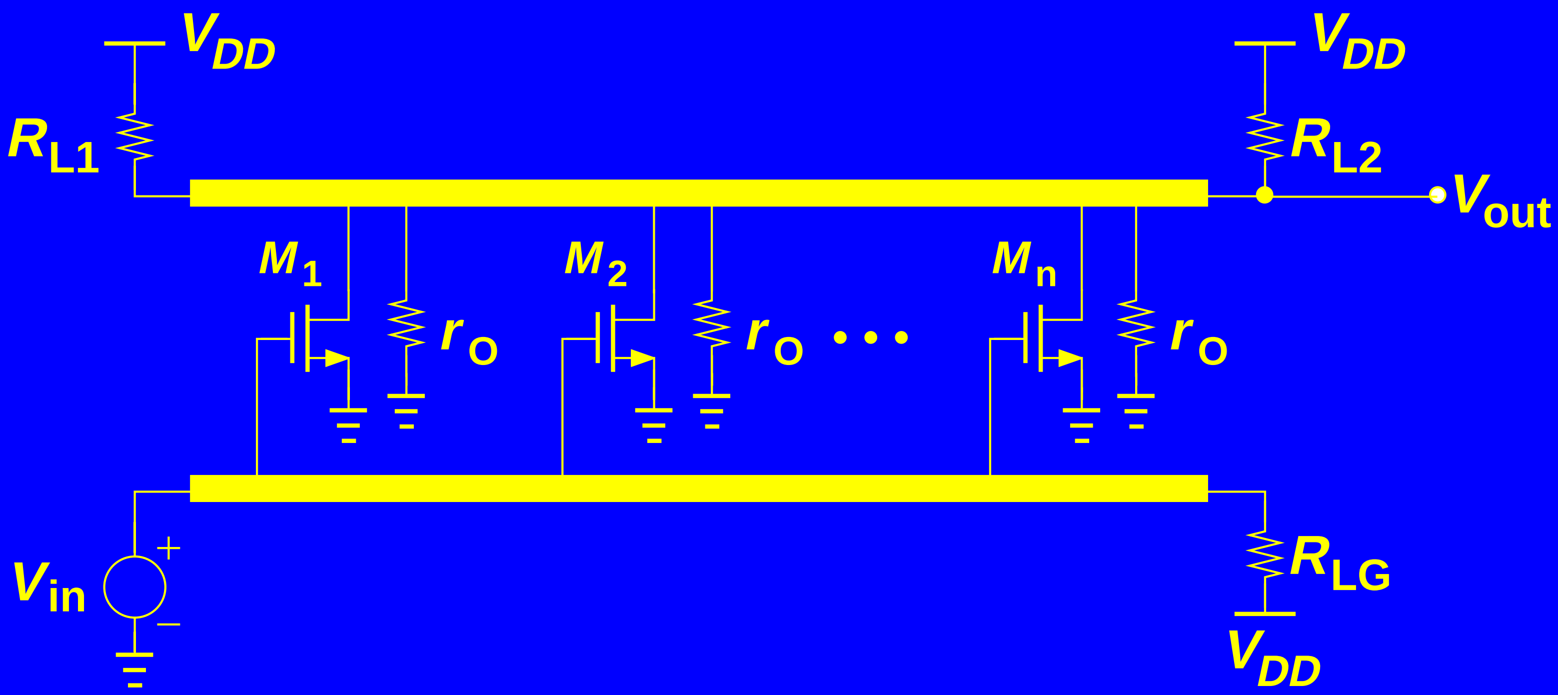
T Line Loss



$$A_V = \pi f_T \frac{I}{V_{0L}}$$

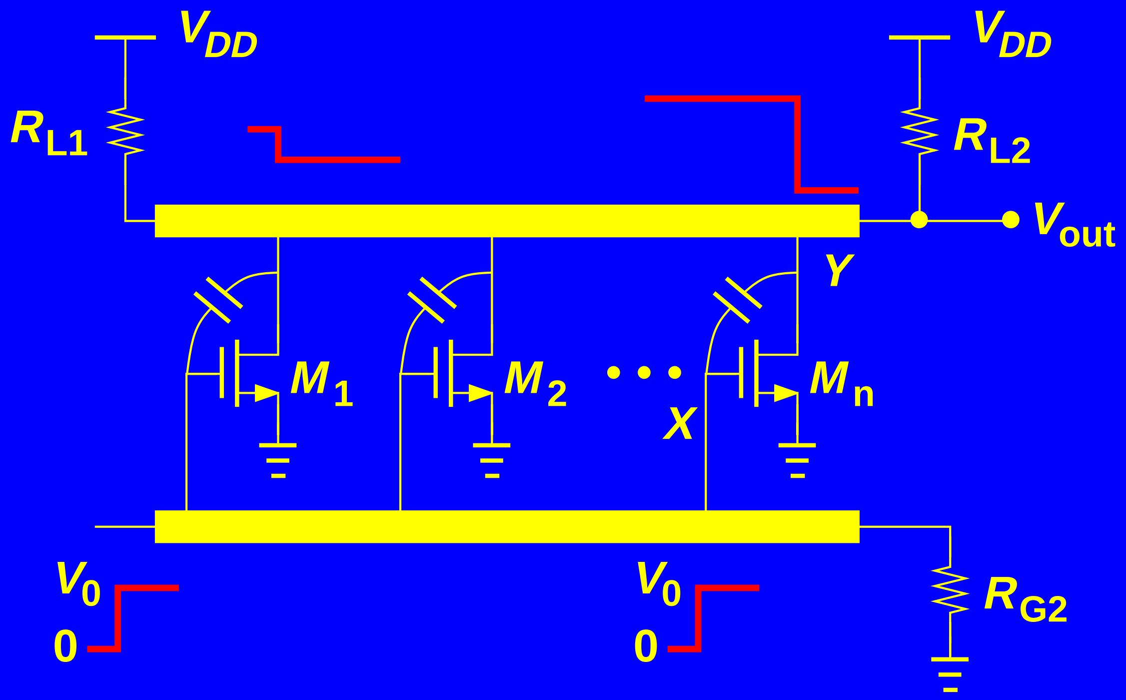
- Even low–frequency resistance of wires introduces significant attenuation at input.

Transistor Output Resistance

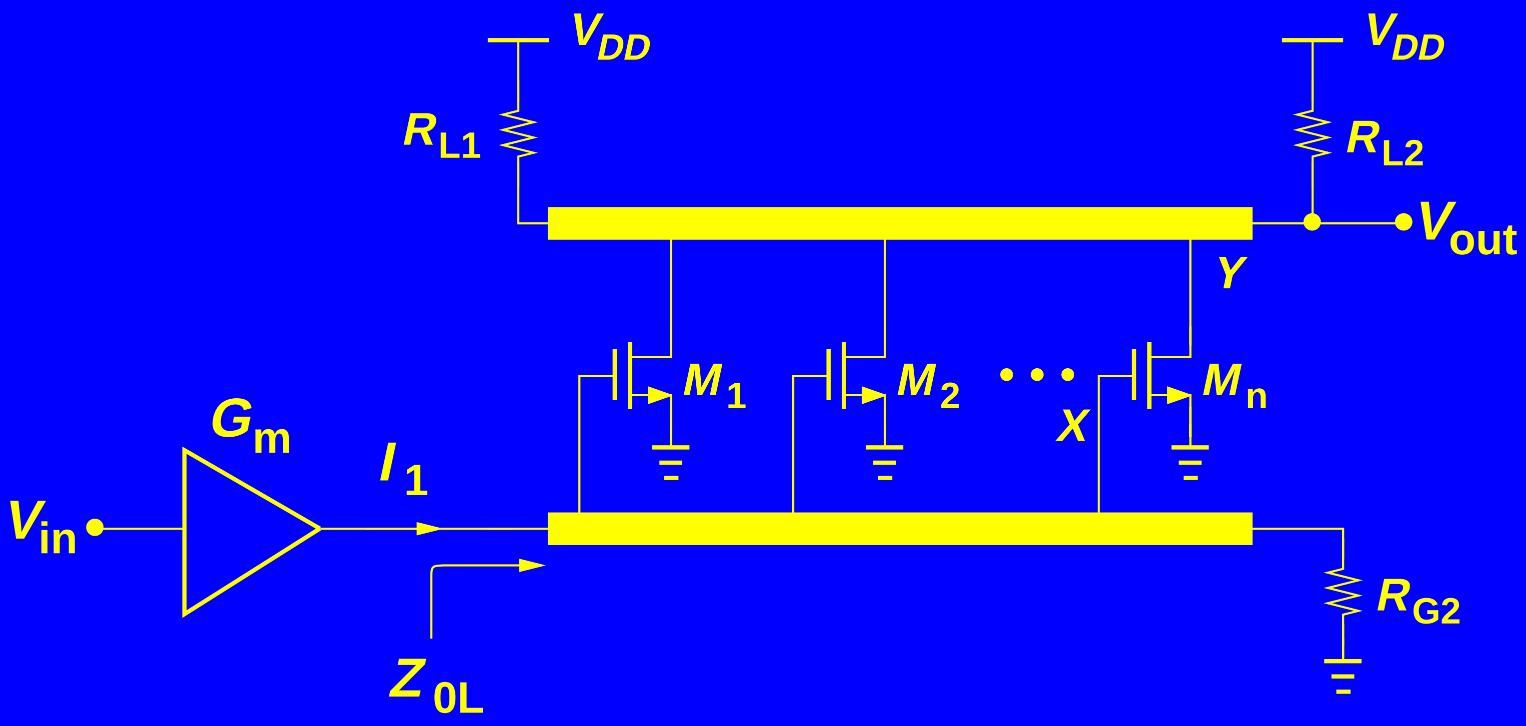


$$\alpha = \frac{1}{2}\left(\frac{R_S}{Z_0} + \frac{n}{r_O} Z_0\right)$$

Miller Multiplication



Input Impedance

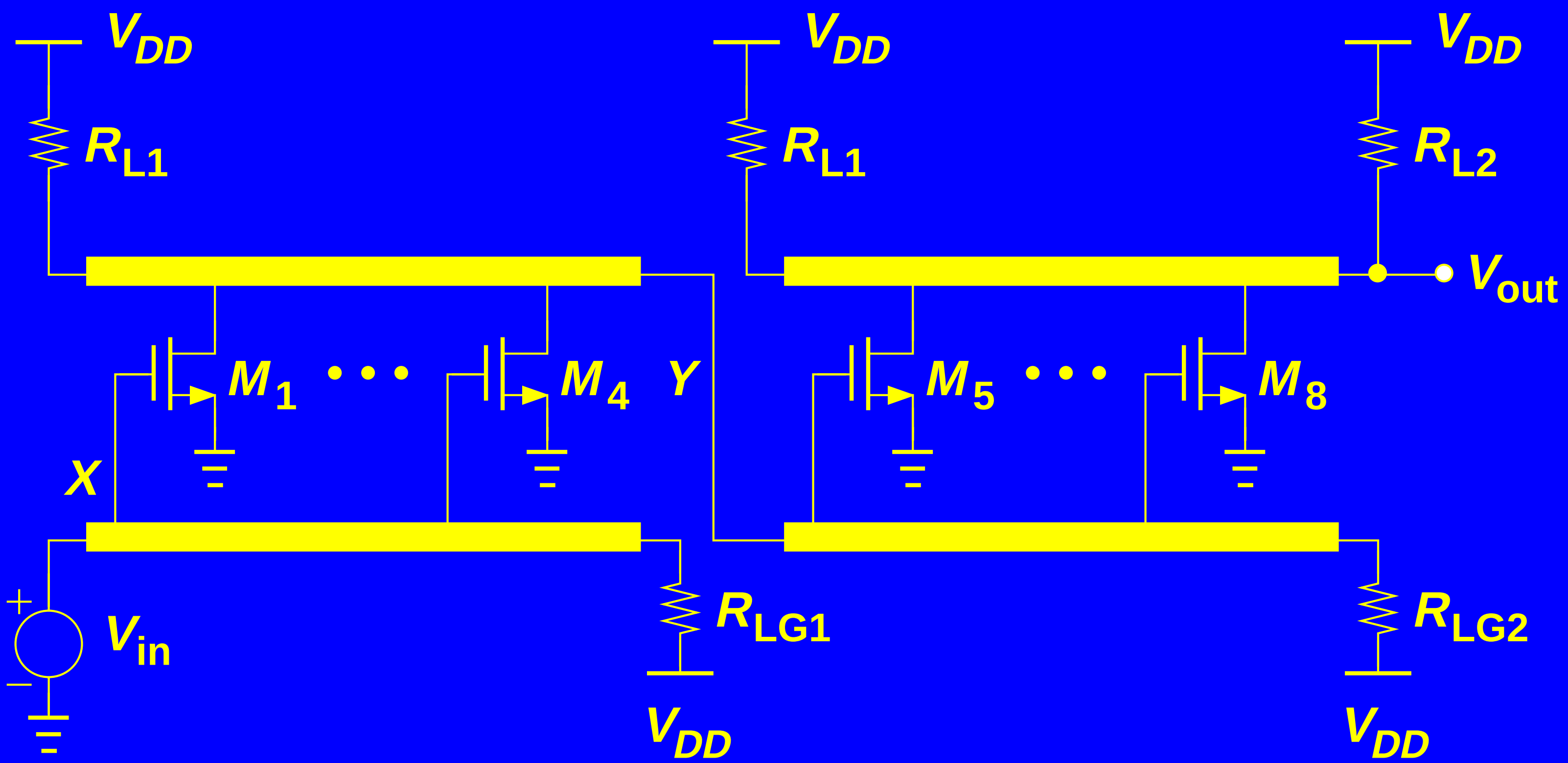


$$V_{out} = I_1 Z_{0L} A_{v,DA}$$

$$Z_{0L} A_{v,DA} = \pi f_T \cdot l \cdot L_u$$

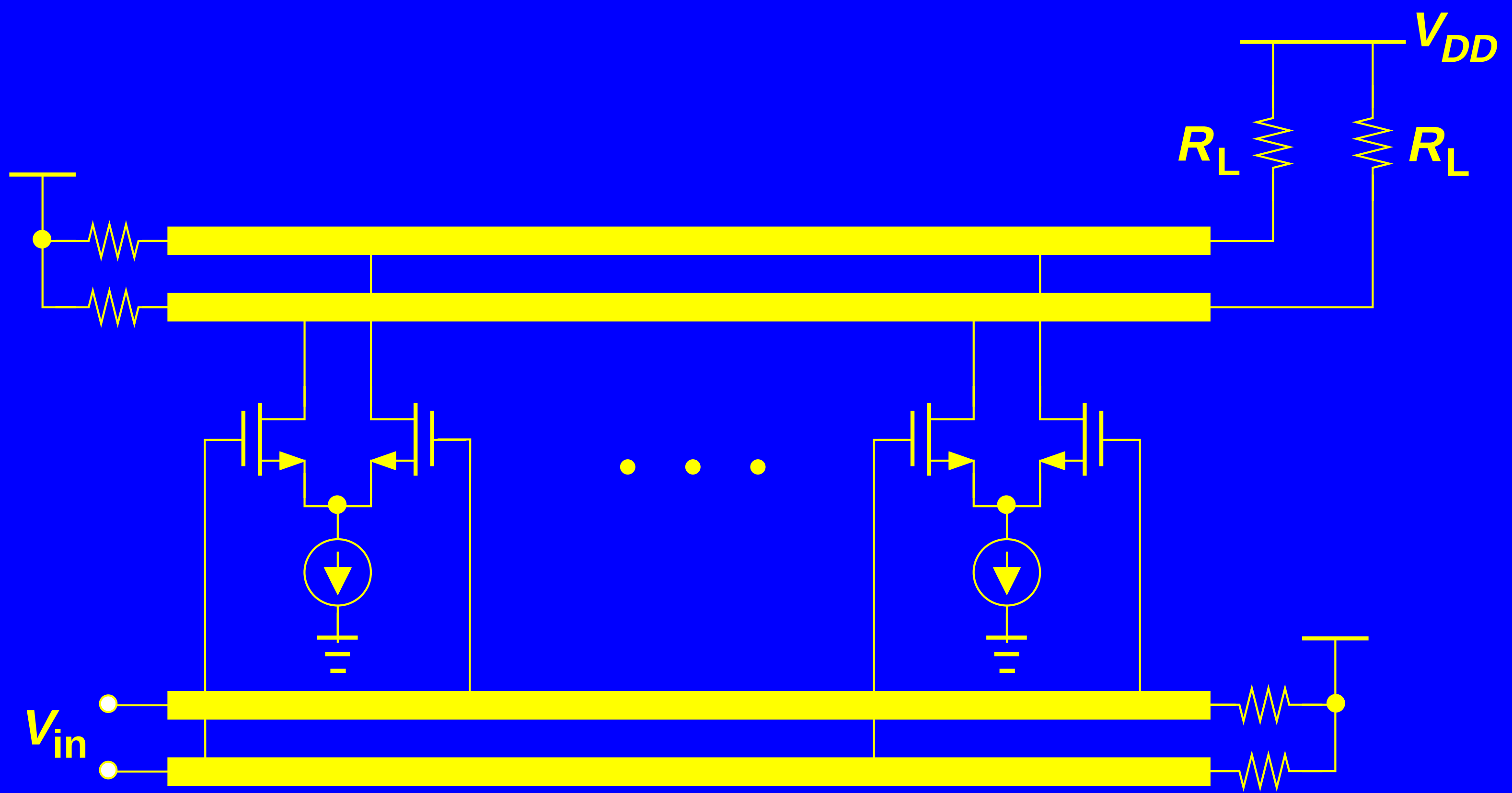
$$\frac{V_{out}}{V_{in}} = \pi G_m \cdot f_T \cdot l \cdot L_u$$

Cascaded Distributed Amplifiers



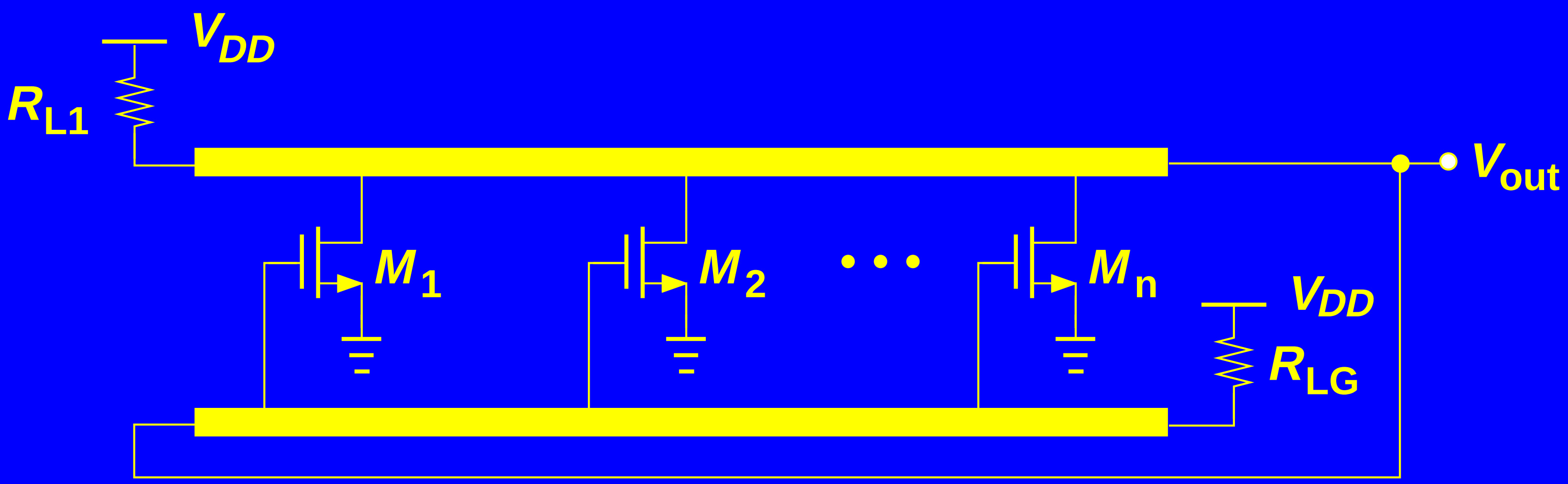
- Voltage headroom becomes a more serious issue.

Differential Distributed Ampifier



- Must route four T lines, a bias line, and a ground line.
- Difficult to maintain layout symmetry.

Distributed Oscillator



- Line delay must yield a phase shift of 180 degrees:

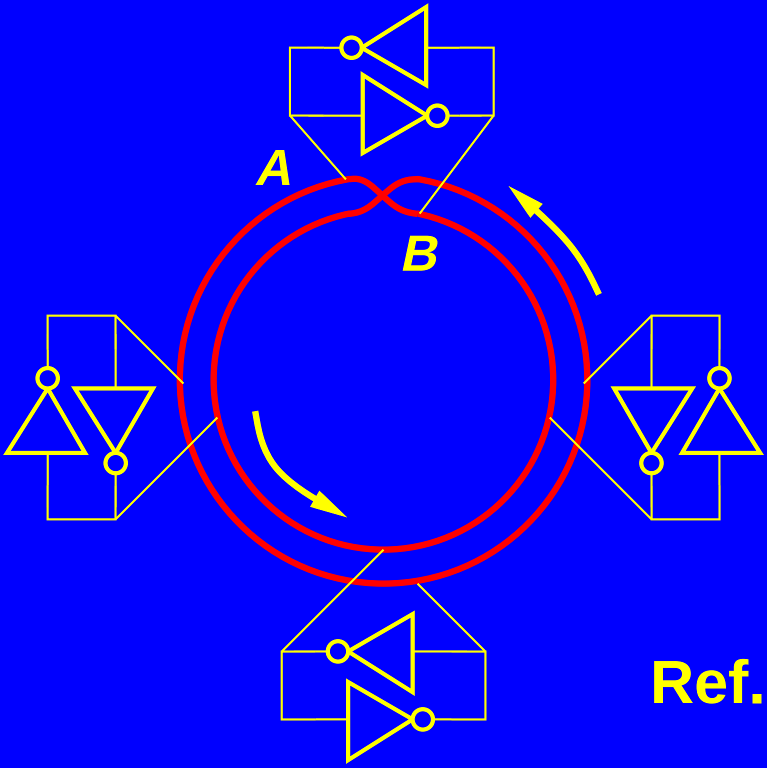
$$\frac{l}{v_{0L}} = \frac{1}{2\,f_{osc}}$$

- Minimum gain for oscillation:

$$A_V = \frac{\pi\, f_T}{2\, f_{osc}} = 1 \;\Rightarrow\; f_{osc} = \frac{\pi}{2}\, f_T$$

- Difficult to make differential.
- Difficult to sense intermediate phases.

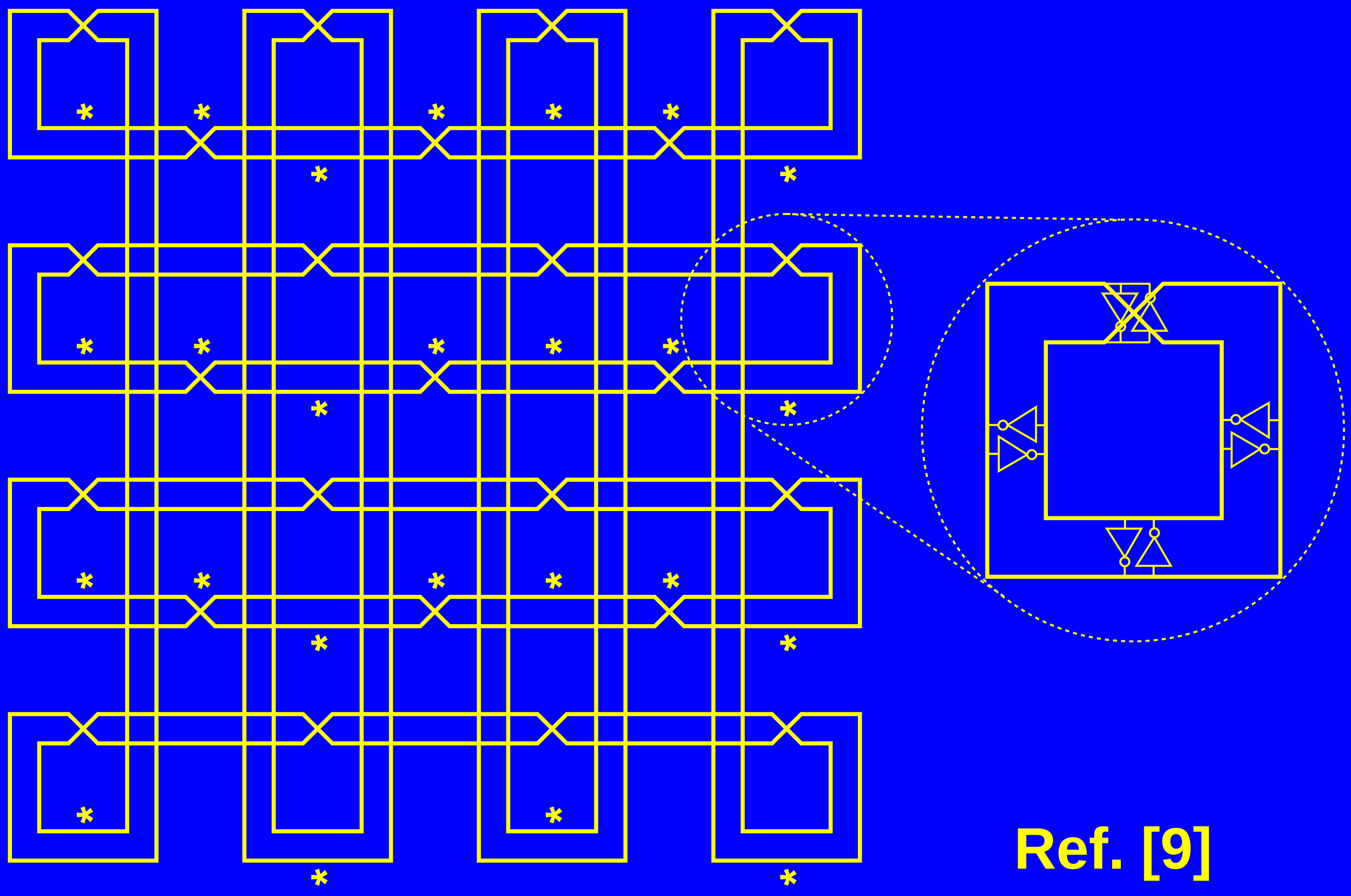
Rotary Oscillator



Ref. [9]

- Oscillation frequency given by phase velocity of loaded line and total length from A to B.

Clock Distribution by Rotary Oscillators



Ref. [9]

- ❒ **Difficult to phase lock the array.**
- ❒ **Other modes of oscillation?**

Conclusion

- Many high−speed circuits must deal with T line effects.
- T lines need not remain undesirable components.
- Modern CMOS technologies offer T lines with reasonable performance.
- T lines can serve in distributed ESD structures, amplifiers, and oscillators.
- T lines provide fertile grounds for new device and circuit topologies.