

# Power Integrity

- Analysis in a split plane PCB

Feng Yu  
Zhejiang University

# In this presentation

- We discuss a method for power integrity analysis in a high speed PCB with split power planes.

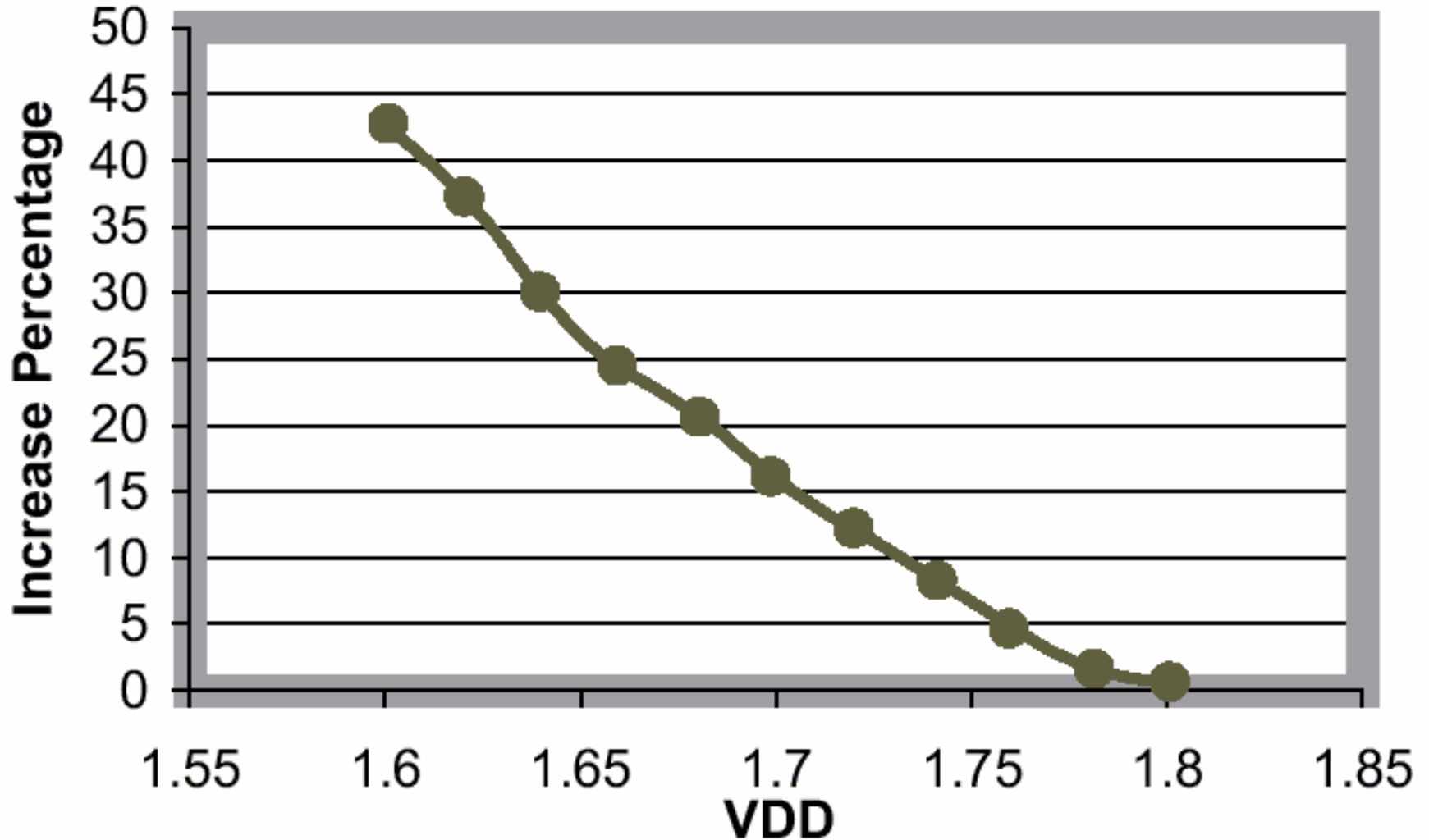
# New trend in high speed design: Power Integrity

- Power integrity becomes a big issue and will be inevitably more and more important.

- Power integrity is becoming a critical issue in chip(IR), package( $Ldi/dt$ ) and PCB design. Power fluctuation affects delay budget in chip and produces noise on board.
- Power integrity is also important for mixed signal boards( e.g.. w. A/D, D/A) and EMI.

- Lower voltage, split planes, poor stack up design, miss used decouple caps, and SSN/SSO all lead to power integrity problems.

# Delay Variation for a 0.18um process



- Cell delay increased by 40% with 10% Power drop.

- Engineers used to depend on experience and over-design to deal with power problems. This method can not cope with increasing frequency and complexity.

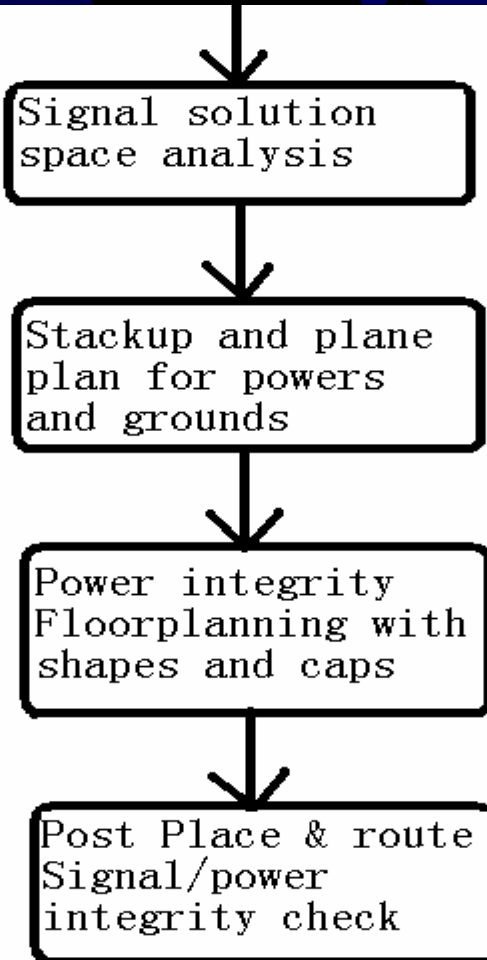
# Power Integrity tool Solution:

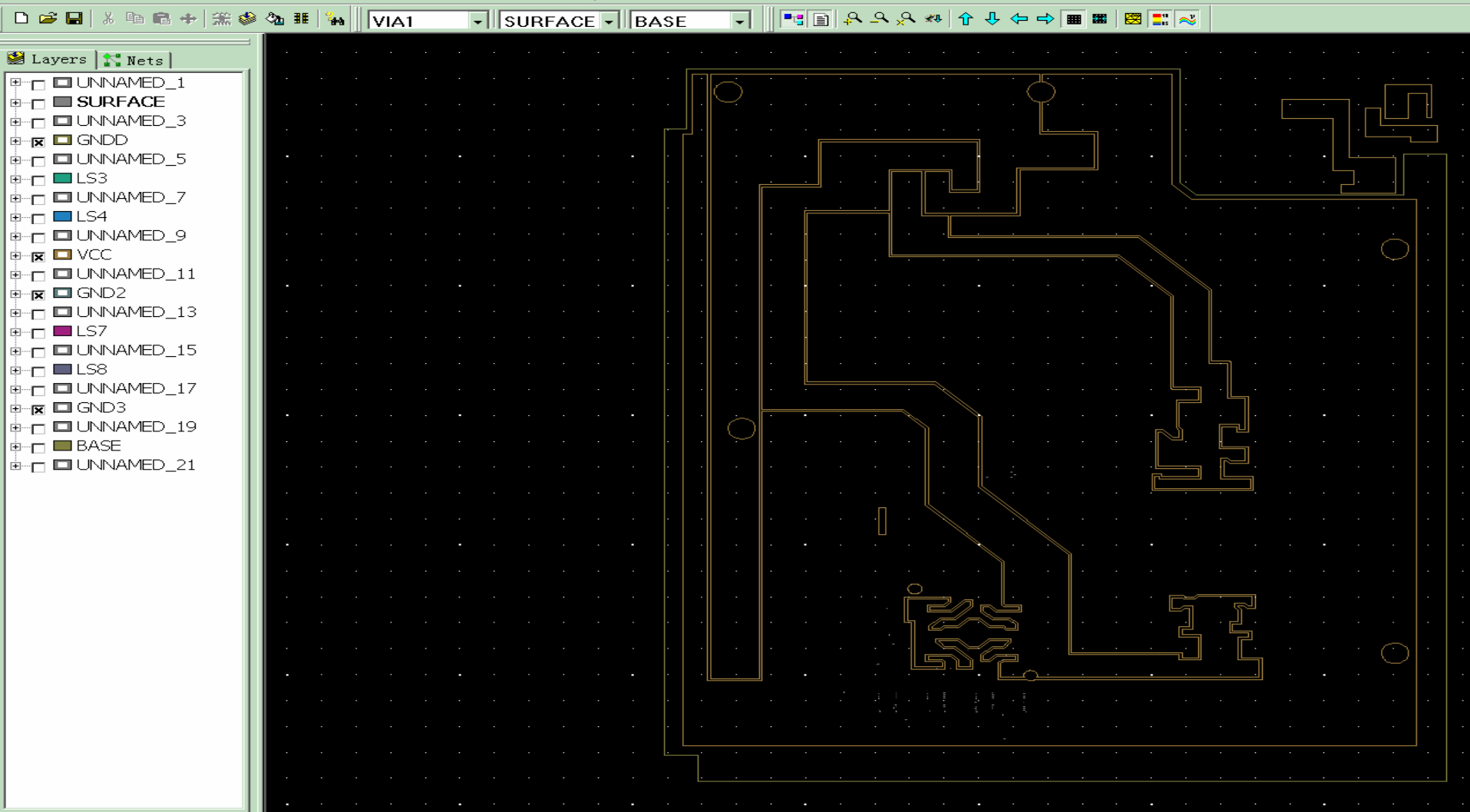
- Power is sensitive to both physical and circuit elements. Physical solvers and circuit simulator must work tightly together in one environment

# SIwave for Power Integrity

- SIwave combines Physical and Circuit Simulations
- SIwave distinguishes itself by using FEM mesh.

# Incorporate PI in high speed PCB Flow



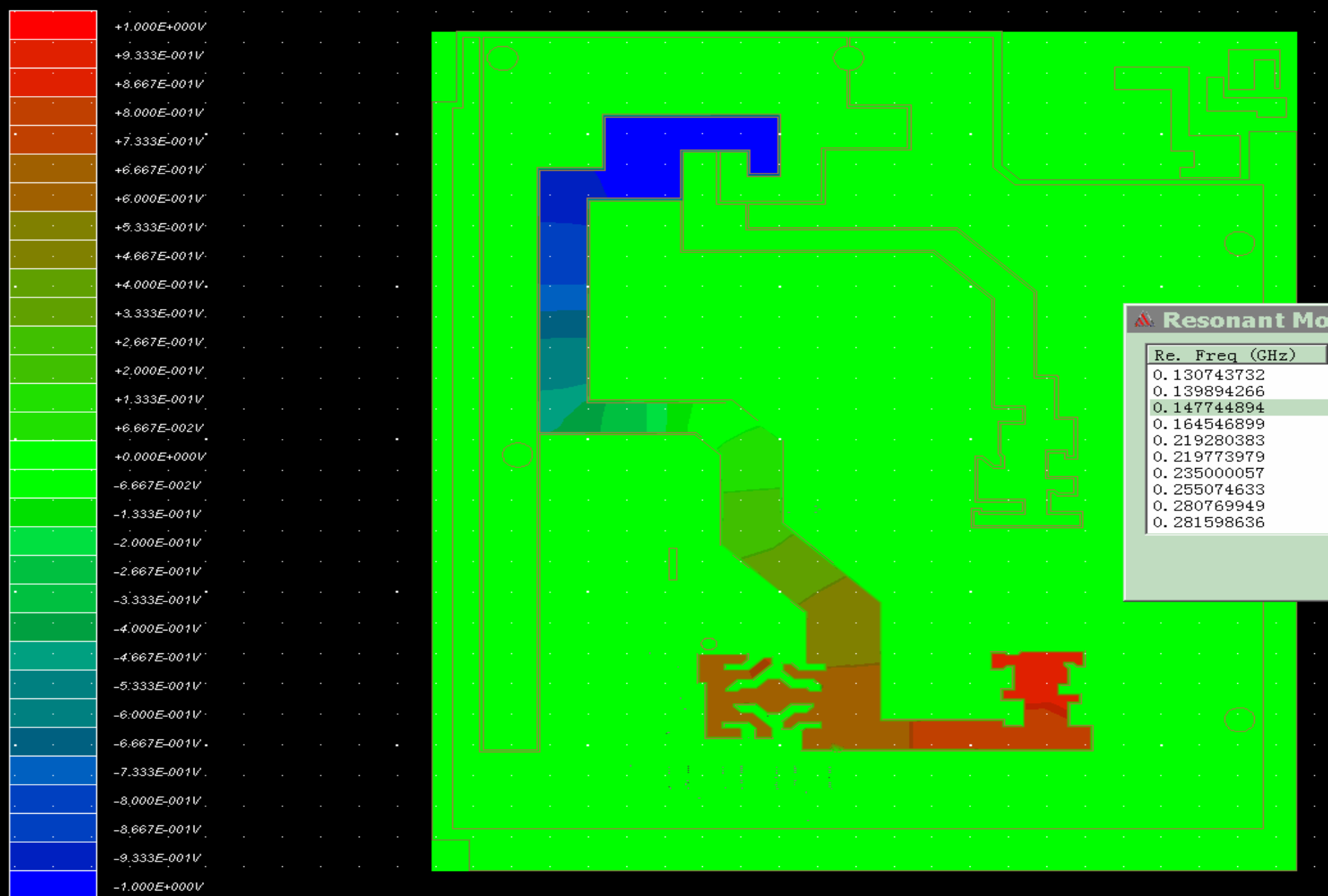


x: 11407. y: -220.42 lx: ly: units: mils Enter C L R V I %P %pP

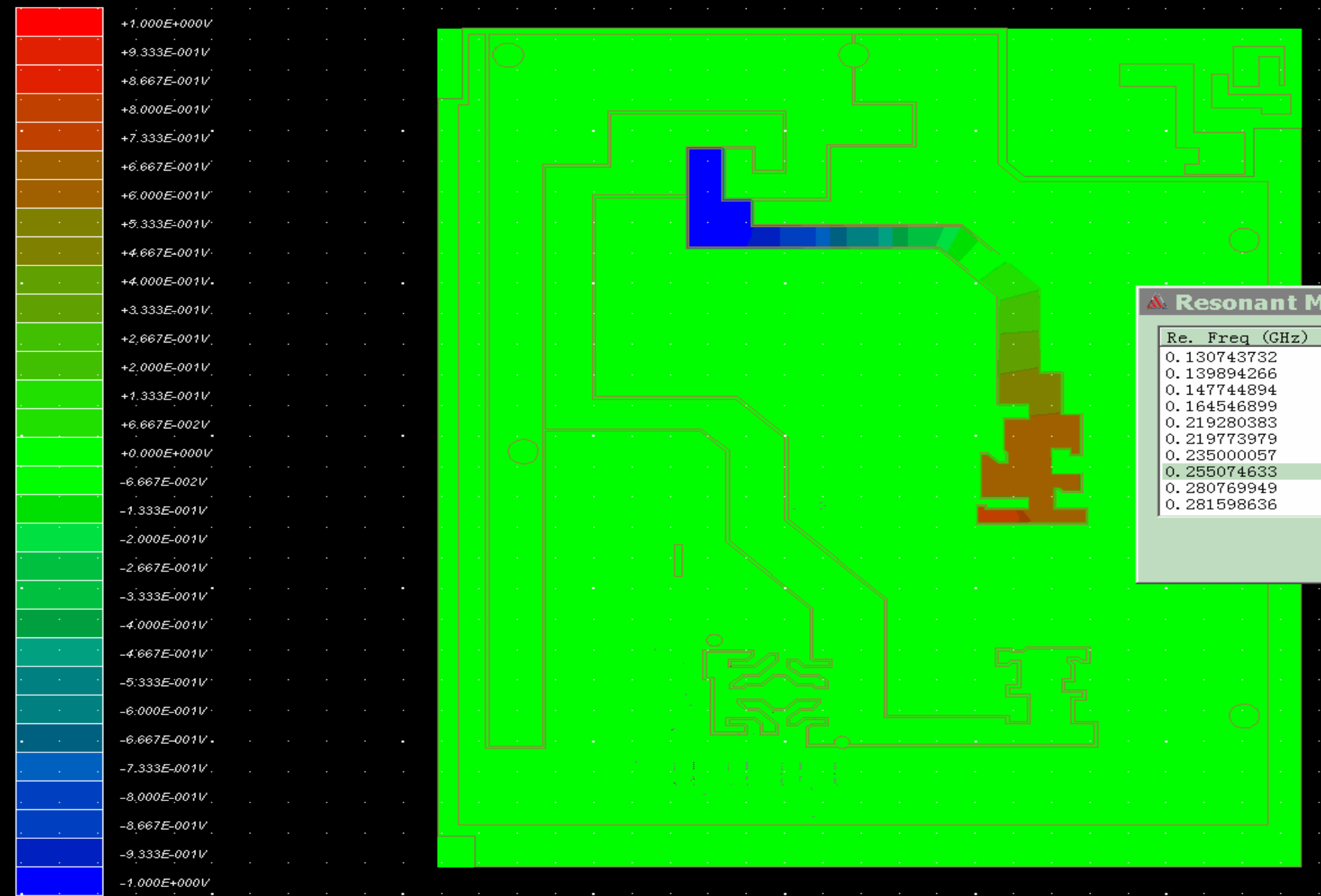
```
Generating solver input files...  
Solving for SYZ-parameters...  
Reading SYZ-parameter data...  
Saving design, simulation options and all solutions...  
Simulation completed on Tue Sep 17 23:08:19 2002
```

```
Deleting S-,Y-,Z-parameter solutions...
```

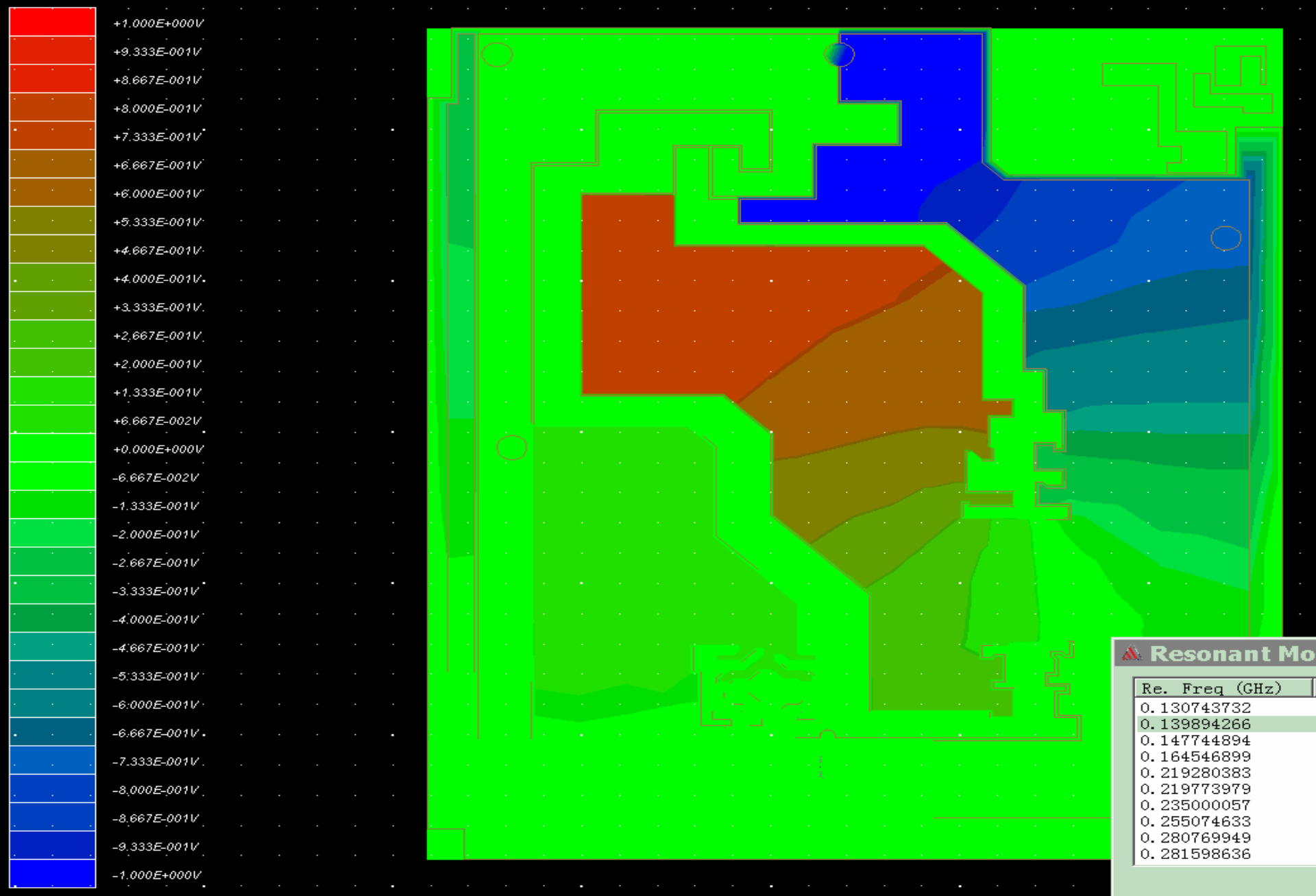
# A ten-layer PCB with split power planes



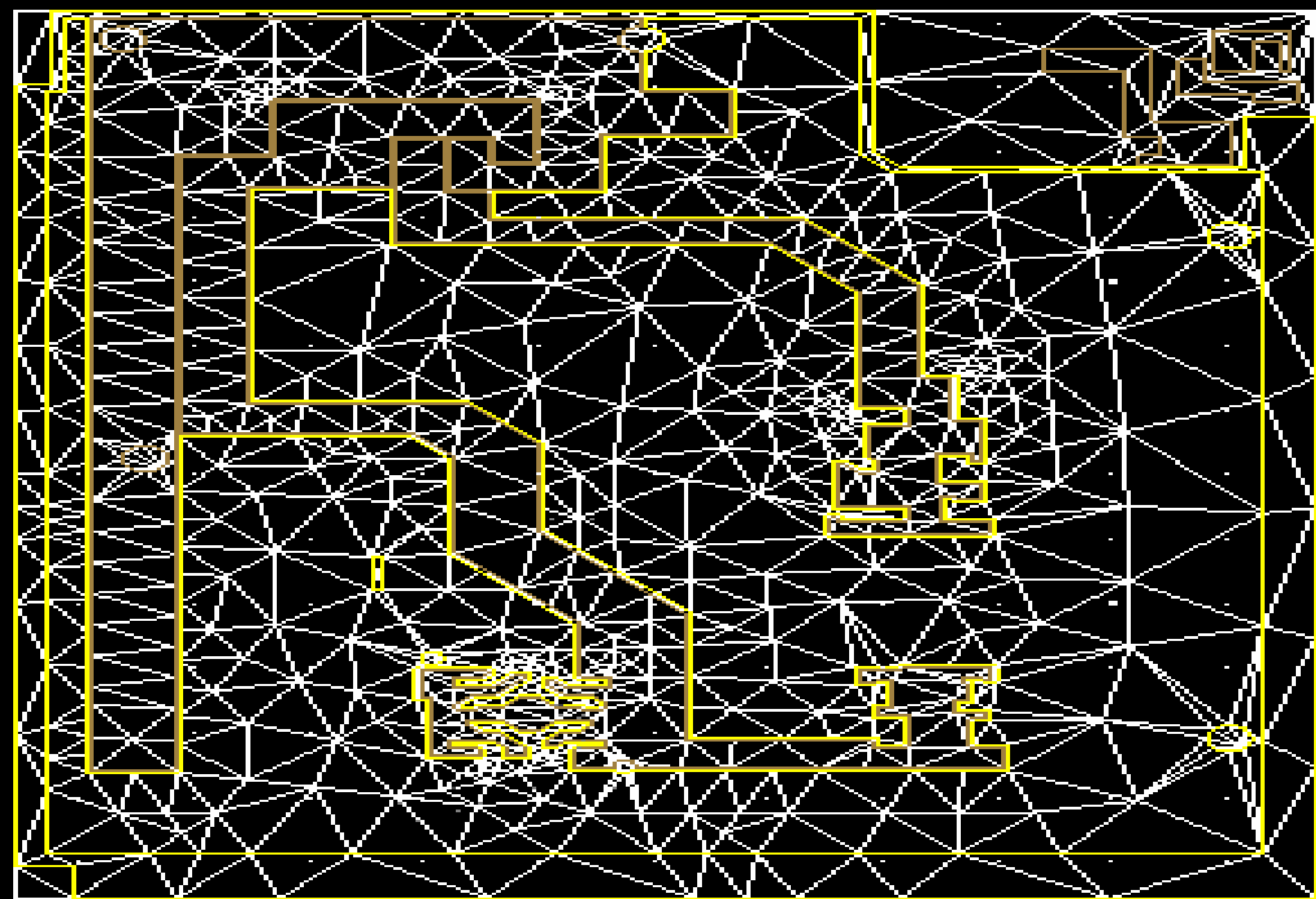
● Bare 1.8v split plane resonance



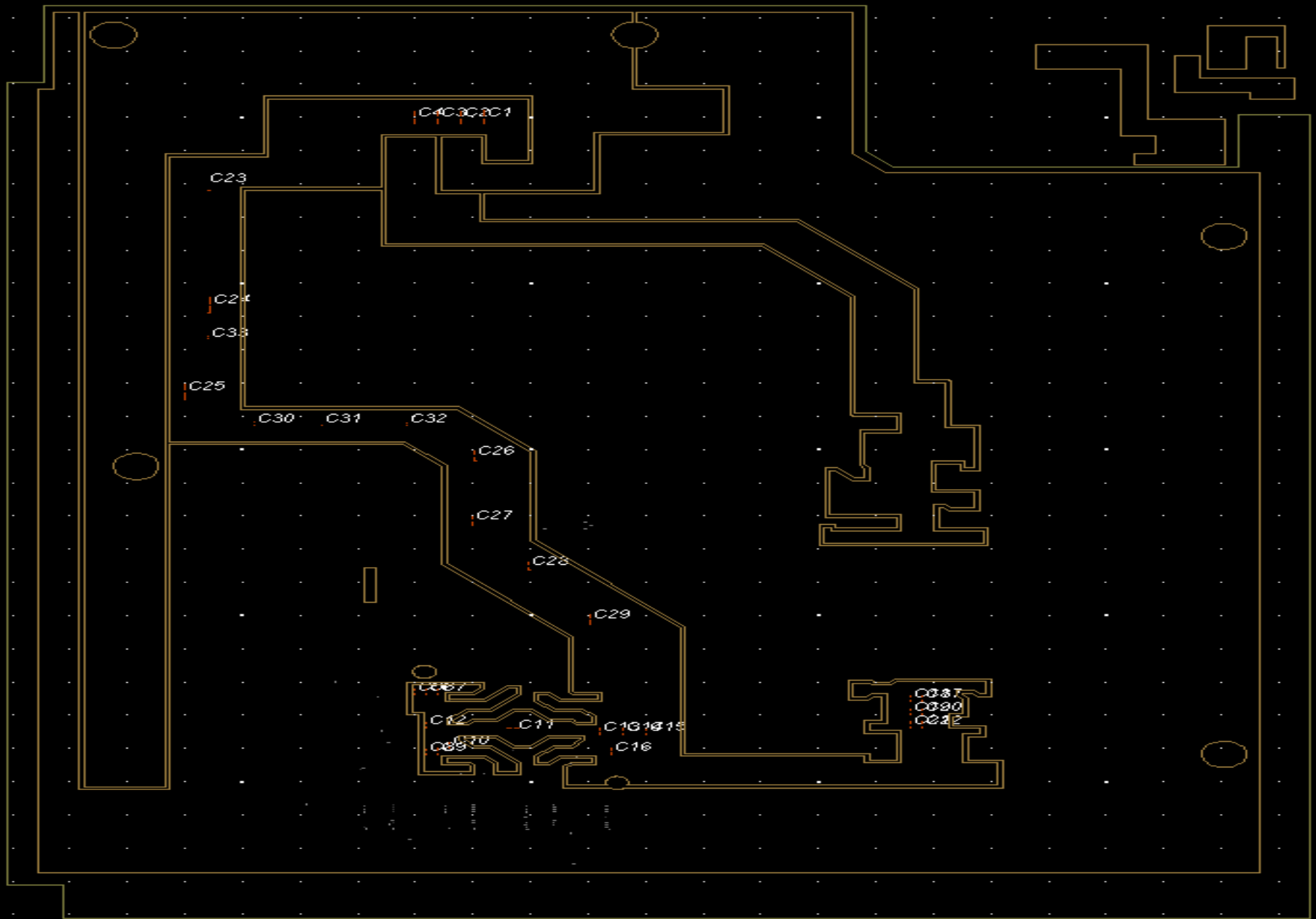
● Bare 2.5v split plane resonance



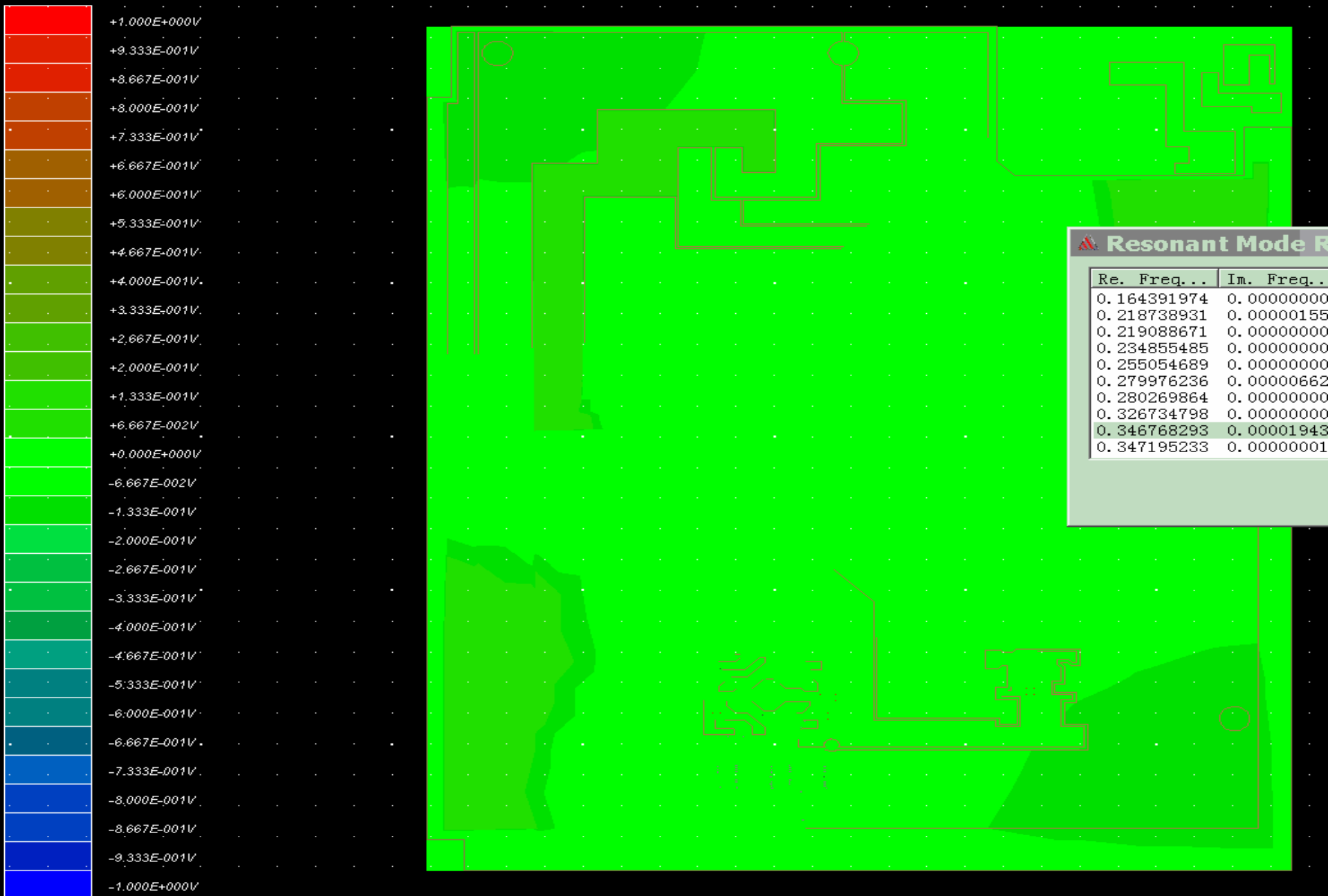
● Bare 3.3v split plane resonance



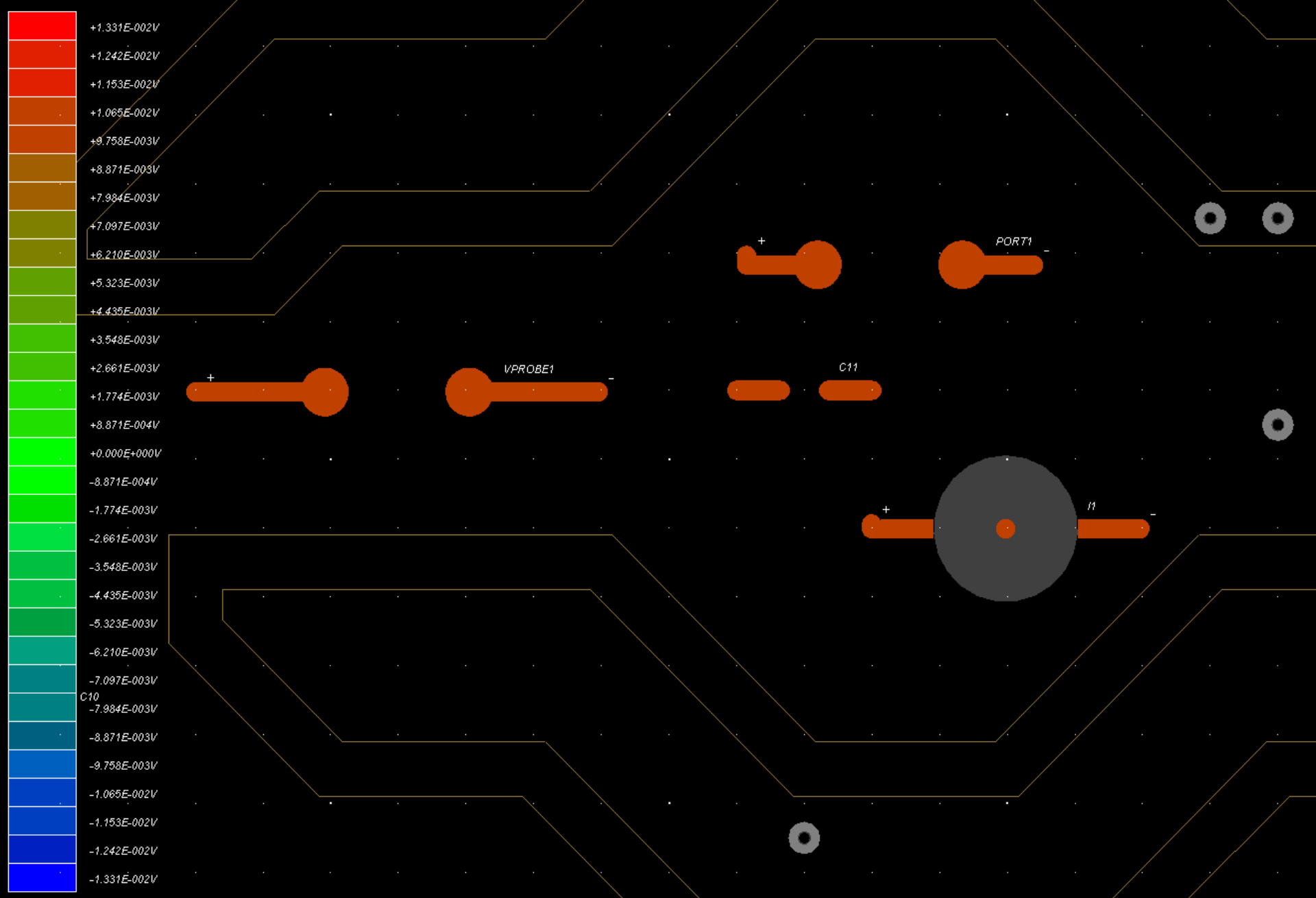
- Mesh is dense in sensitive areas



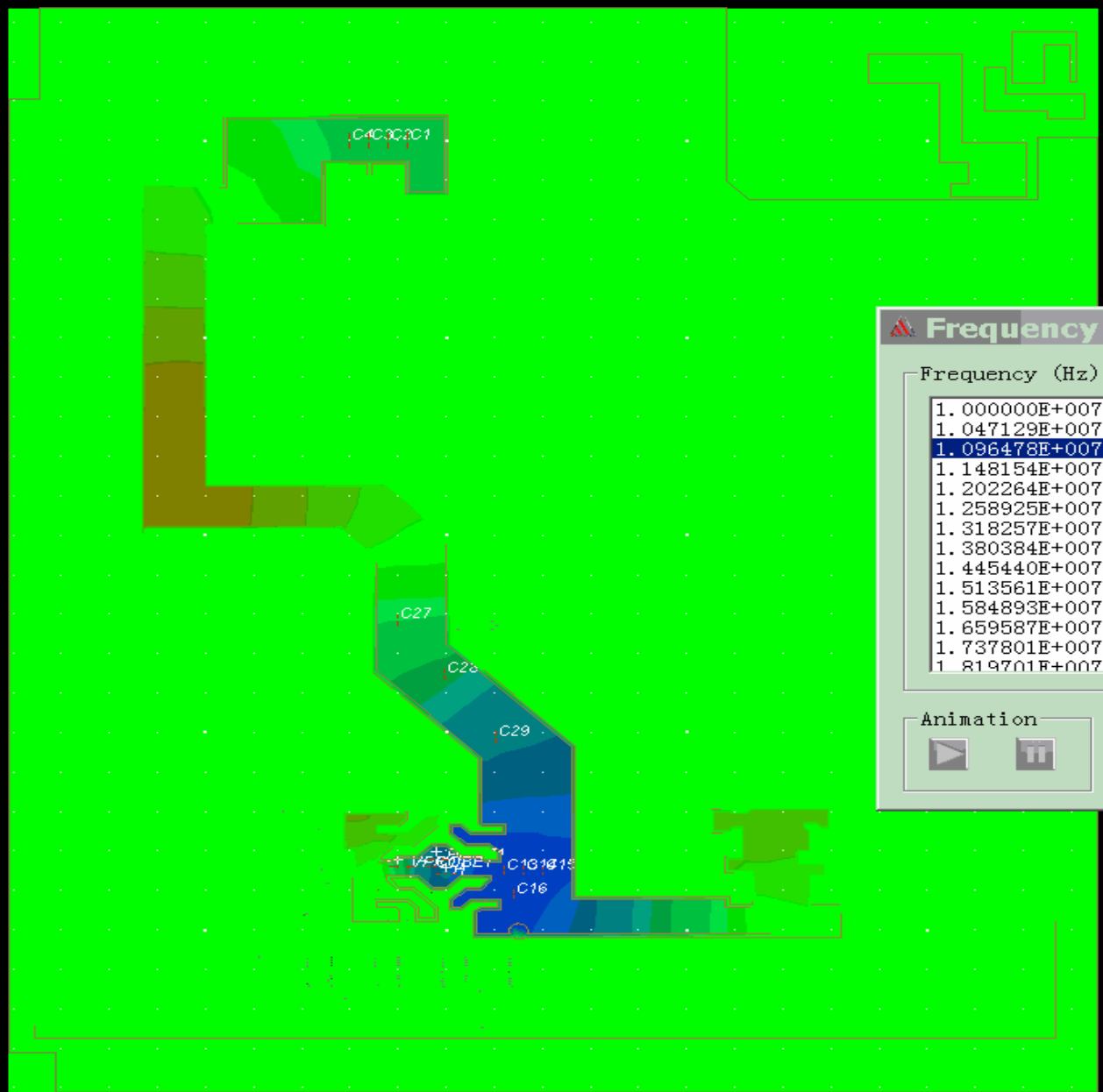
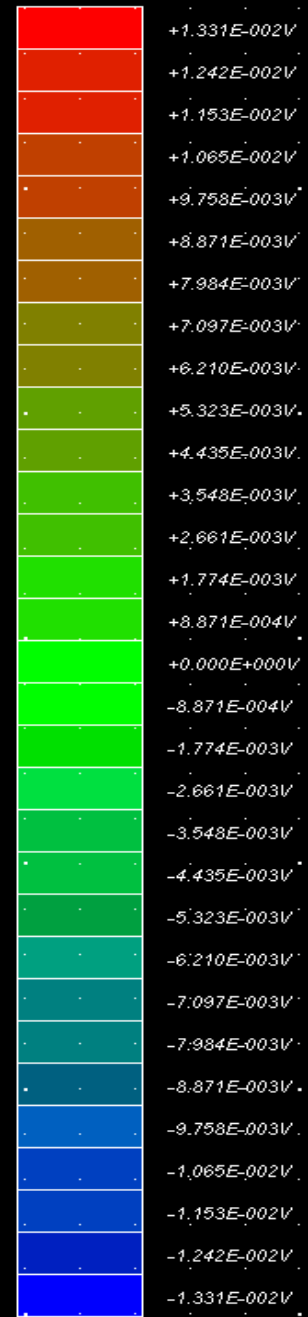
● Add 0.01uf caps for 1.8v split plane



● No resonance observed up to 350Mhz



● An 1A current source & voltage probe added



**Frequency Sw**

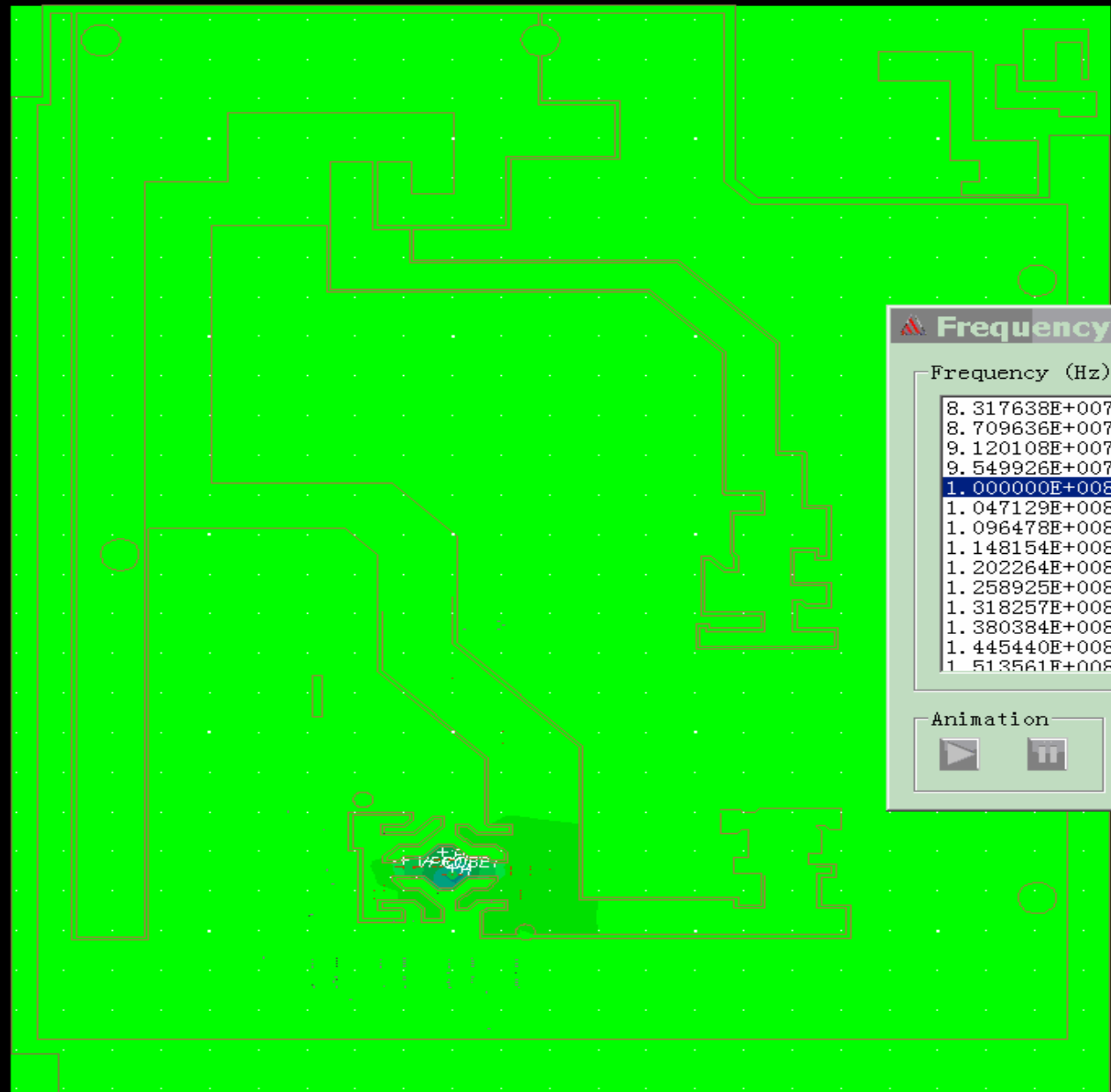
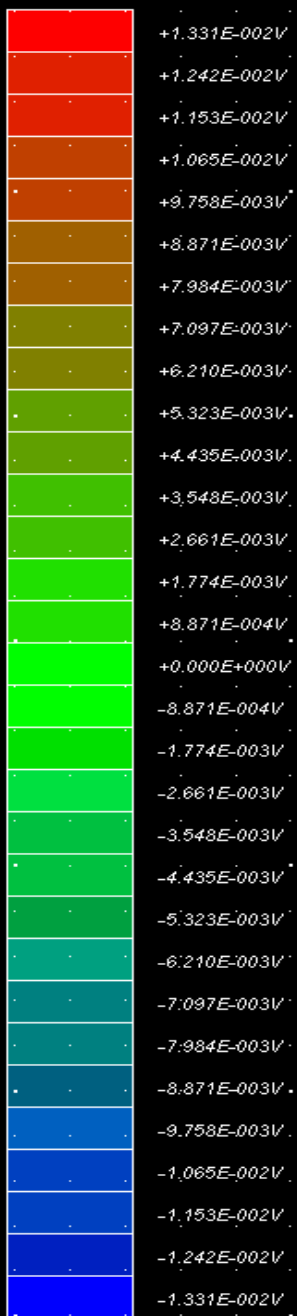
Frequency (Hz)

1.000000E+007
1.047129E+007
<b>1.096478E+007</b>
1.148154E+007
1.202264E+007
1.258925E+007
1.318257E+007
1.380384E+007
1.445440E+007
1.513561E+007
1.584893E+007
1.659587E+007
1.737801E+007
1.819701E+007

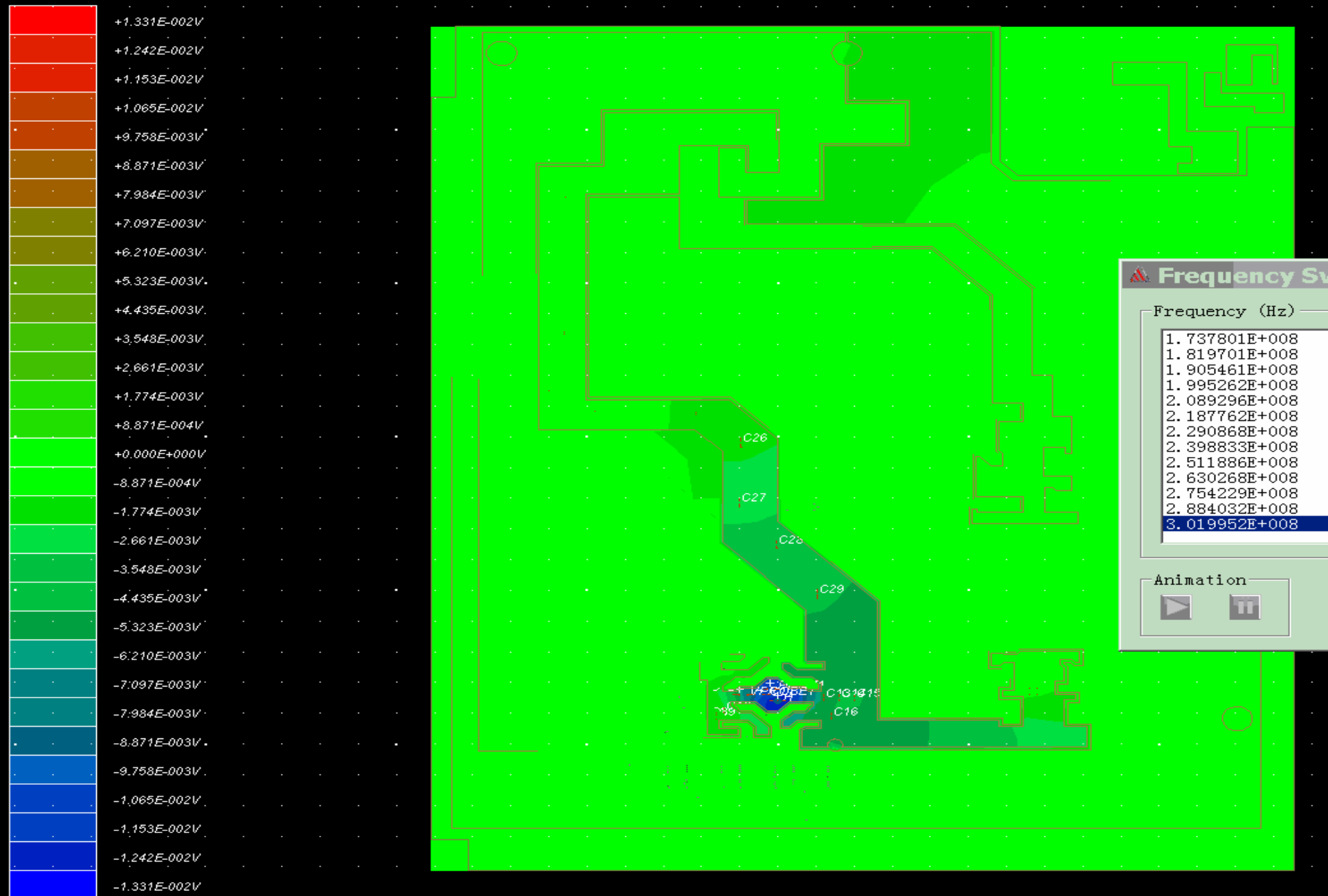
Animation

▶ ⏸

Small voltage fluctuation in 10MHz

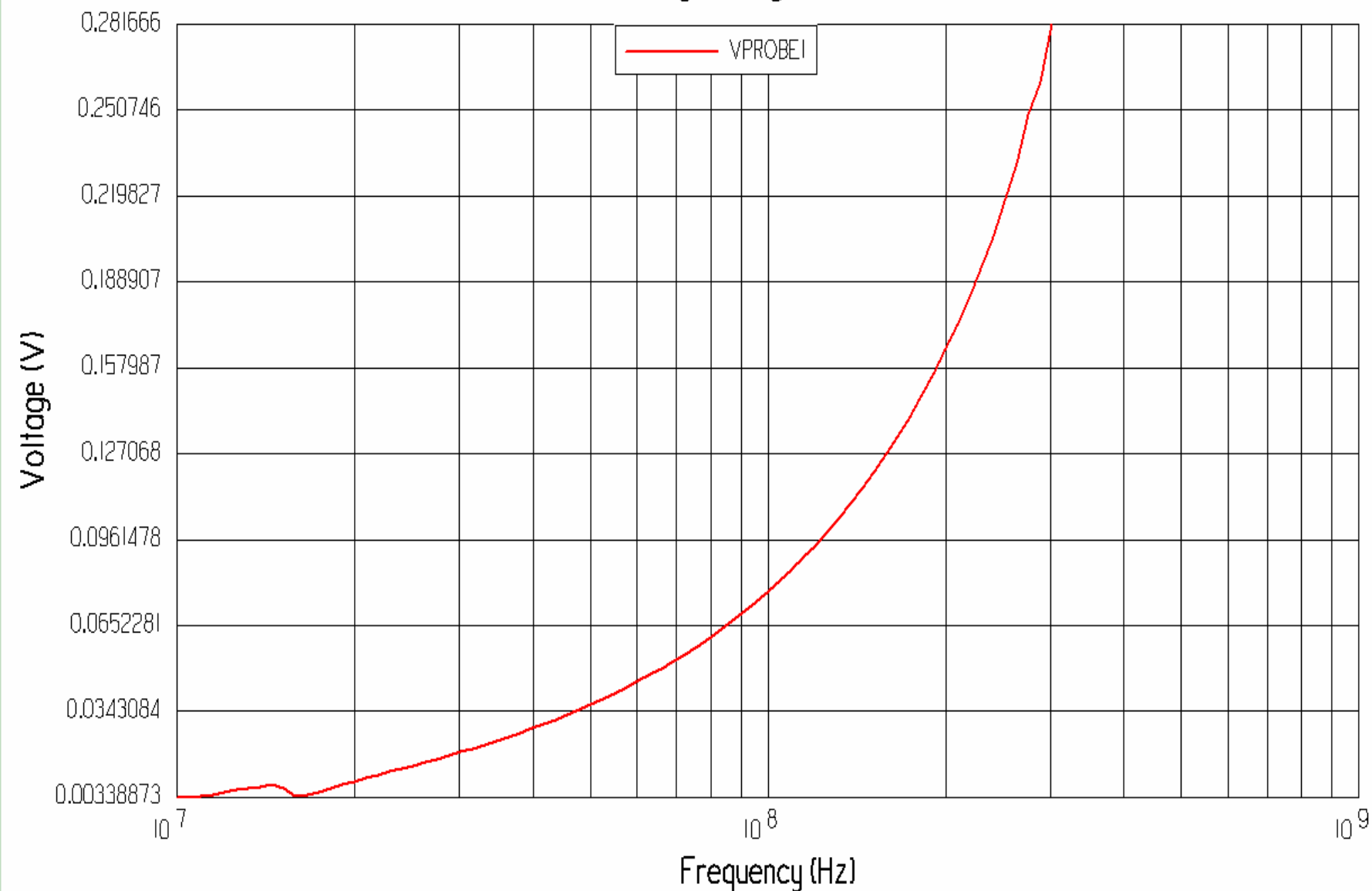


● Little voltage fluctuation in 100MHz

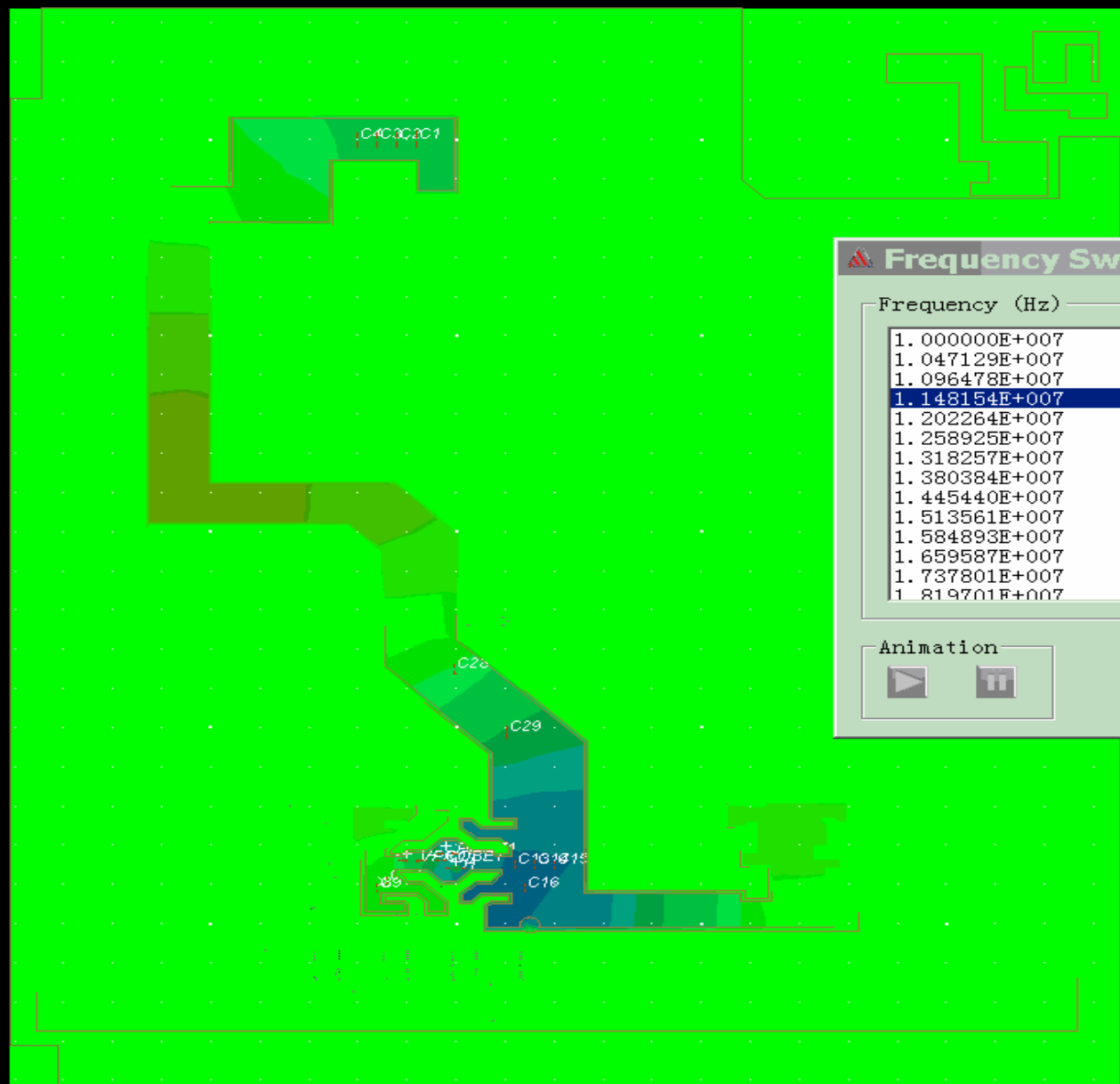
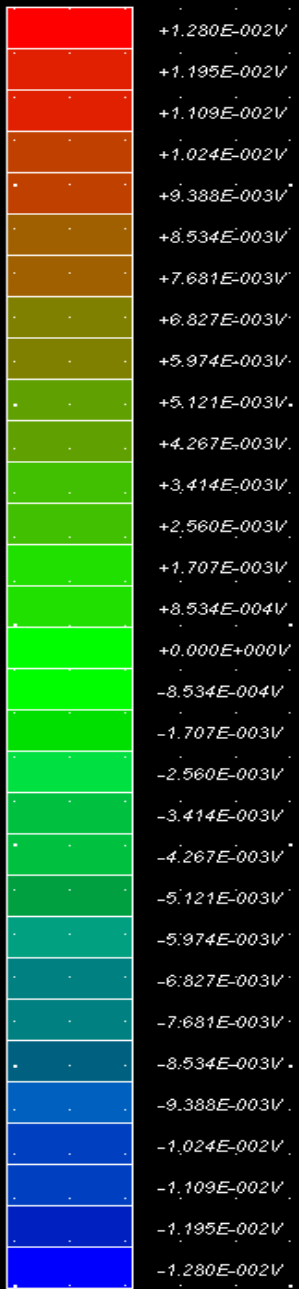


Some local voltage fluctuation in 300MHz

### Voltage Magnitude Plot



● Voltage vs. frequency at voltage probe point



**Frequency Sweep**

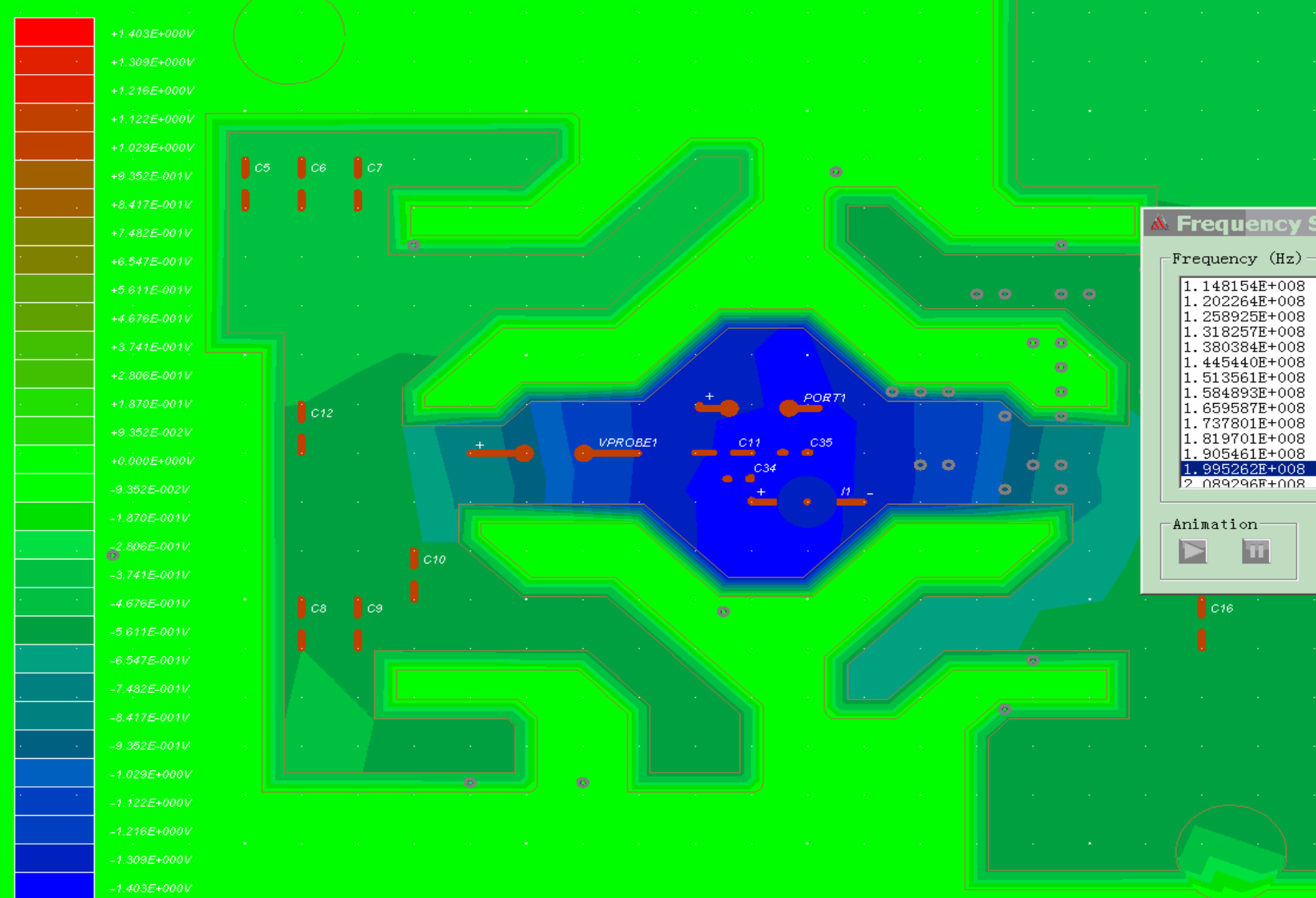
Frequency (Hz)

- 1.000000E+007
- 1.047129E+007
- 1.096478E+007
- 1.148154E+007
- 1.202264E+007
- 1.258925E+007
- 1.318257E+007
- 1.380384E+007
- 1.445440E+007
- 1.513561E+007
- 1.584893E+007
- 1.659587E+007
- 1.737801E+007
- 1.819701E+007

Animation

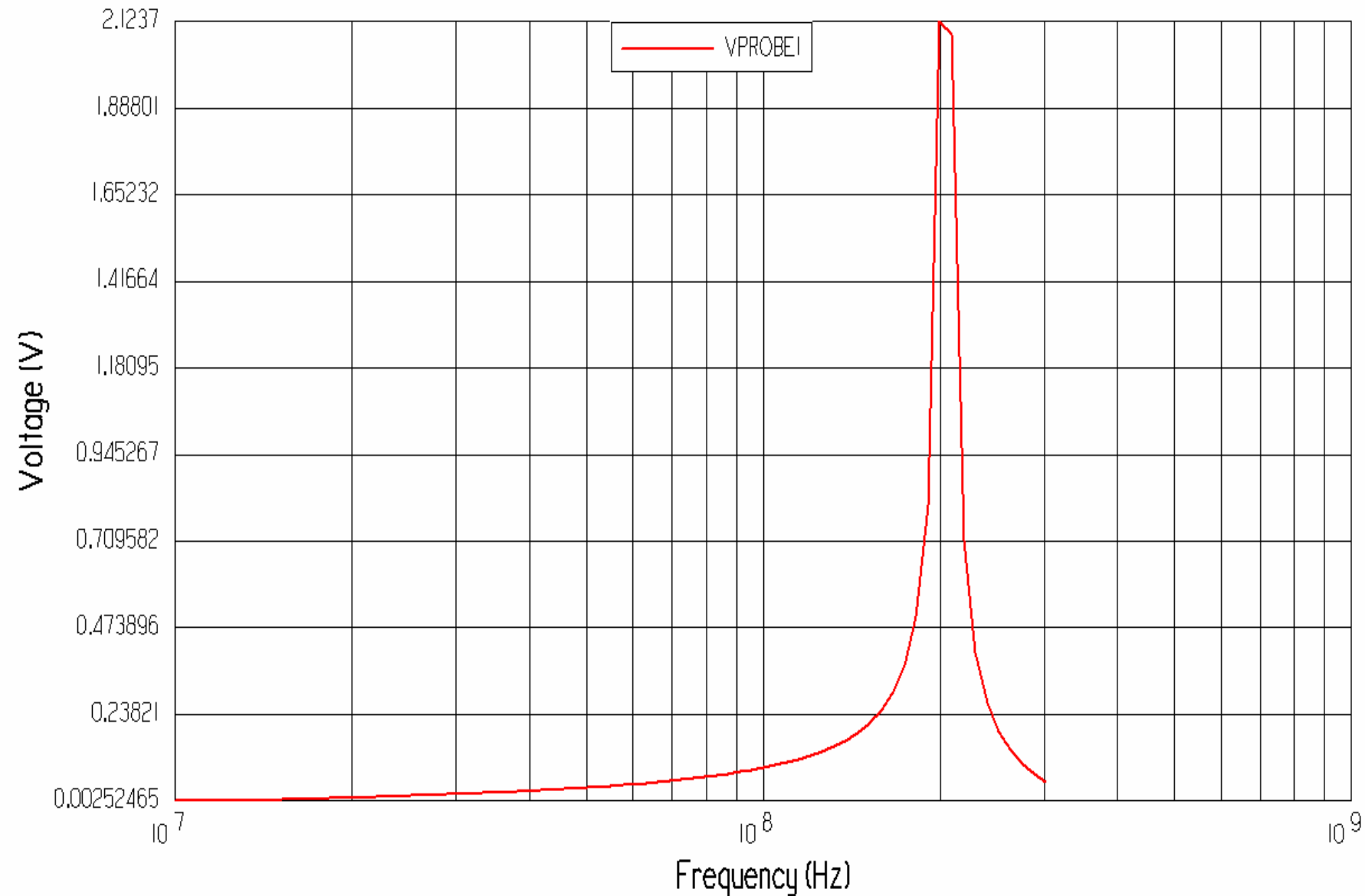
▶ ⏸

● Three 100uf caps added to reduce fluctuation

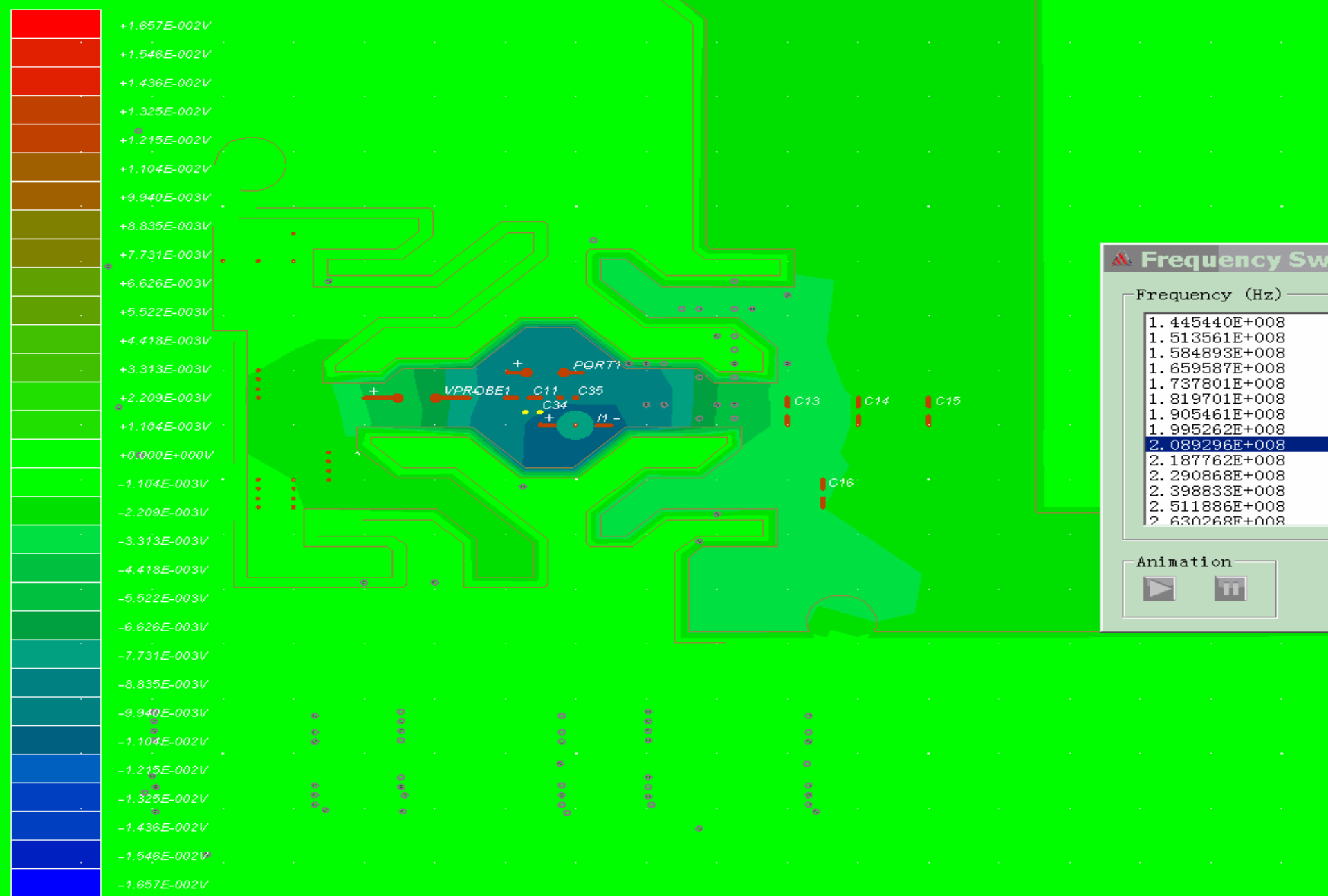


1nf local caps for high frequency decouple, but

# Voltage Magnitude Plot

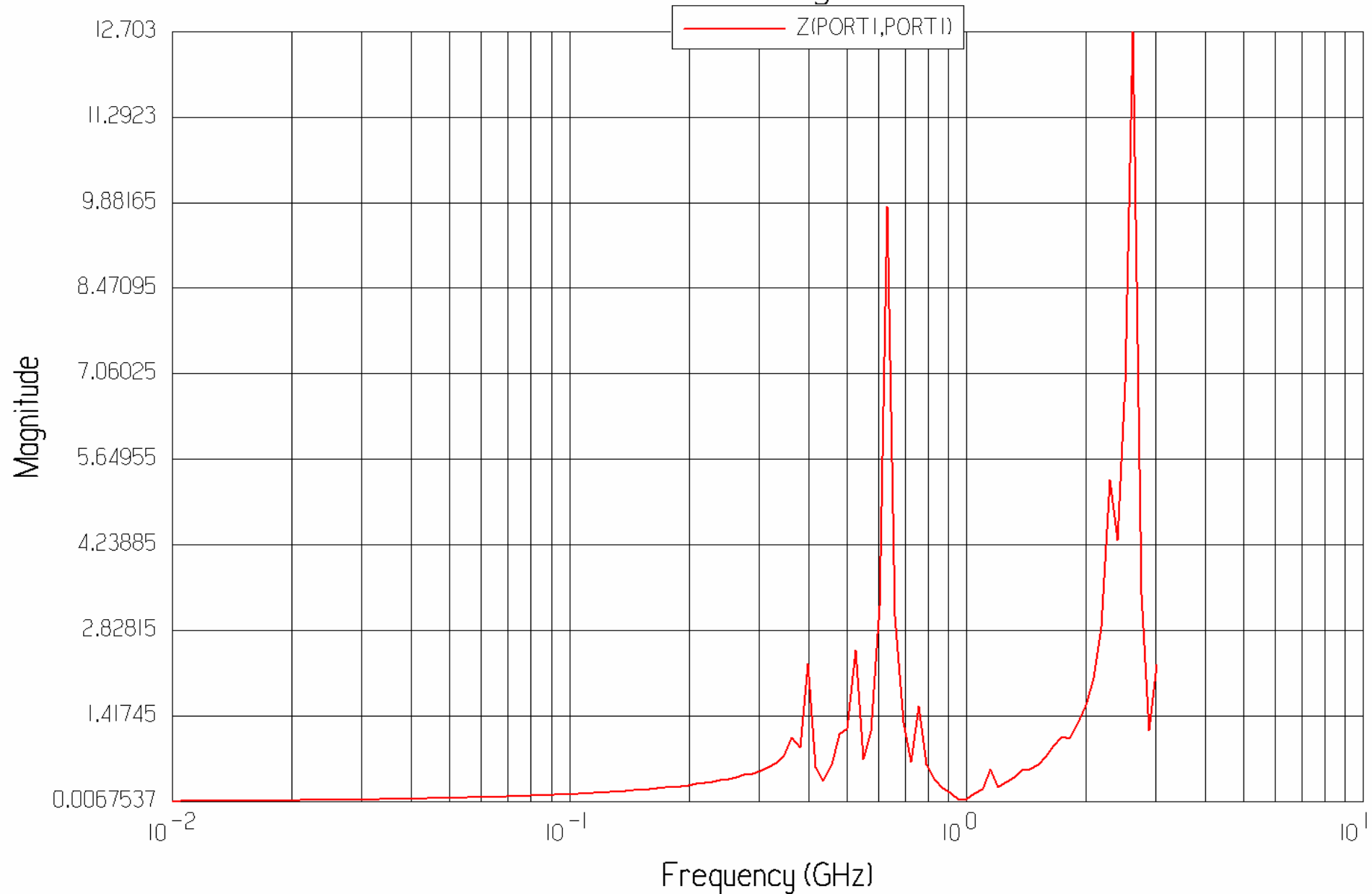


 Resonance induced



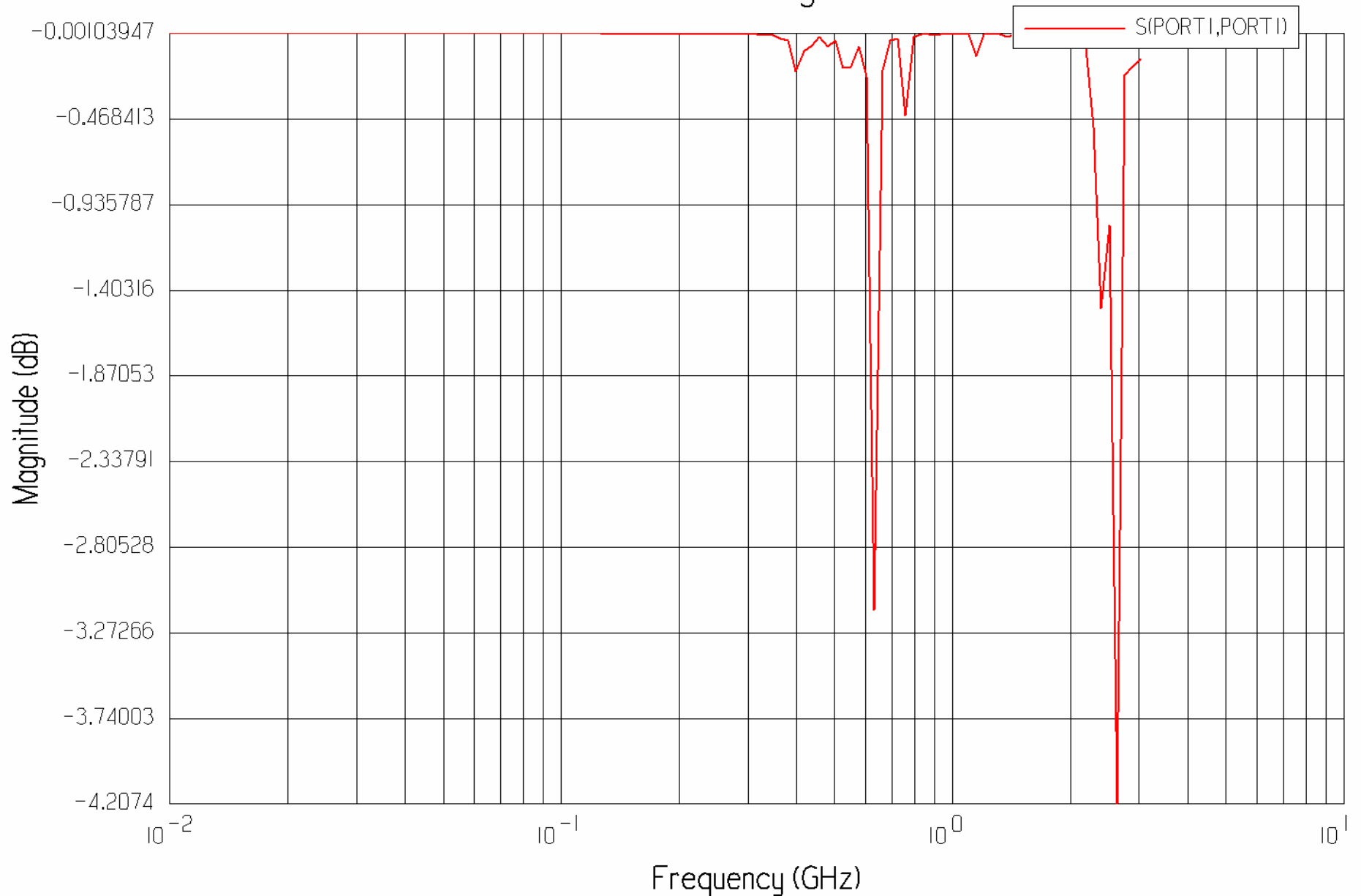
Adjust caps to avoid resonance

# Z-Parameter Magnitude Plot

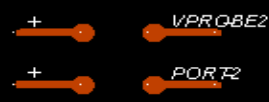
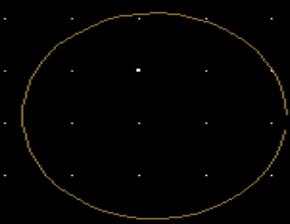
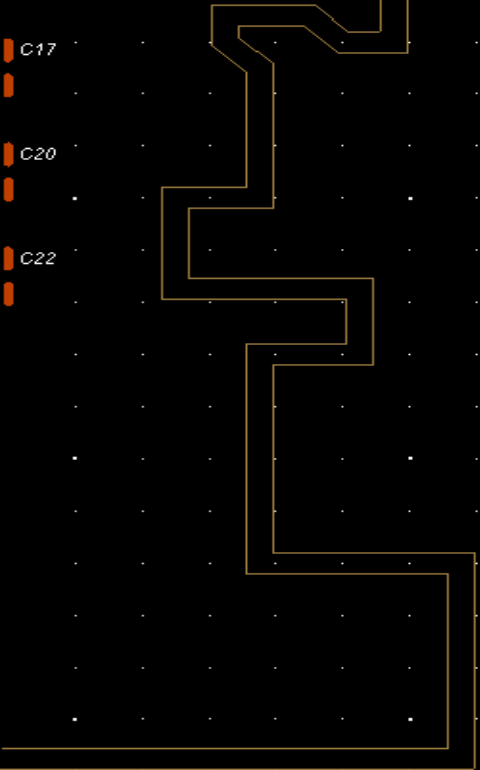


● Z parameter vs. frequency at probe point

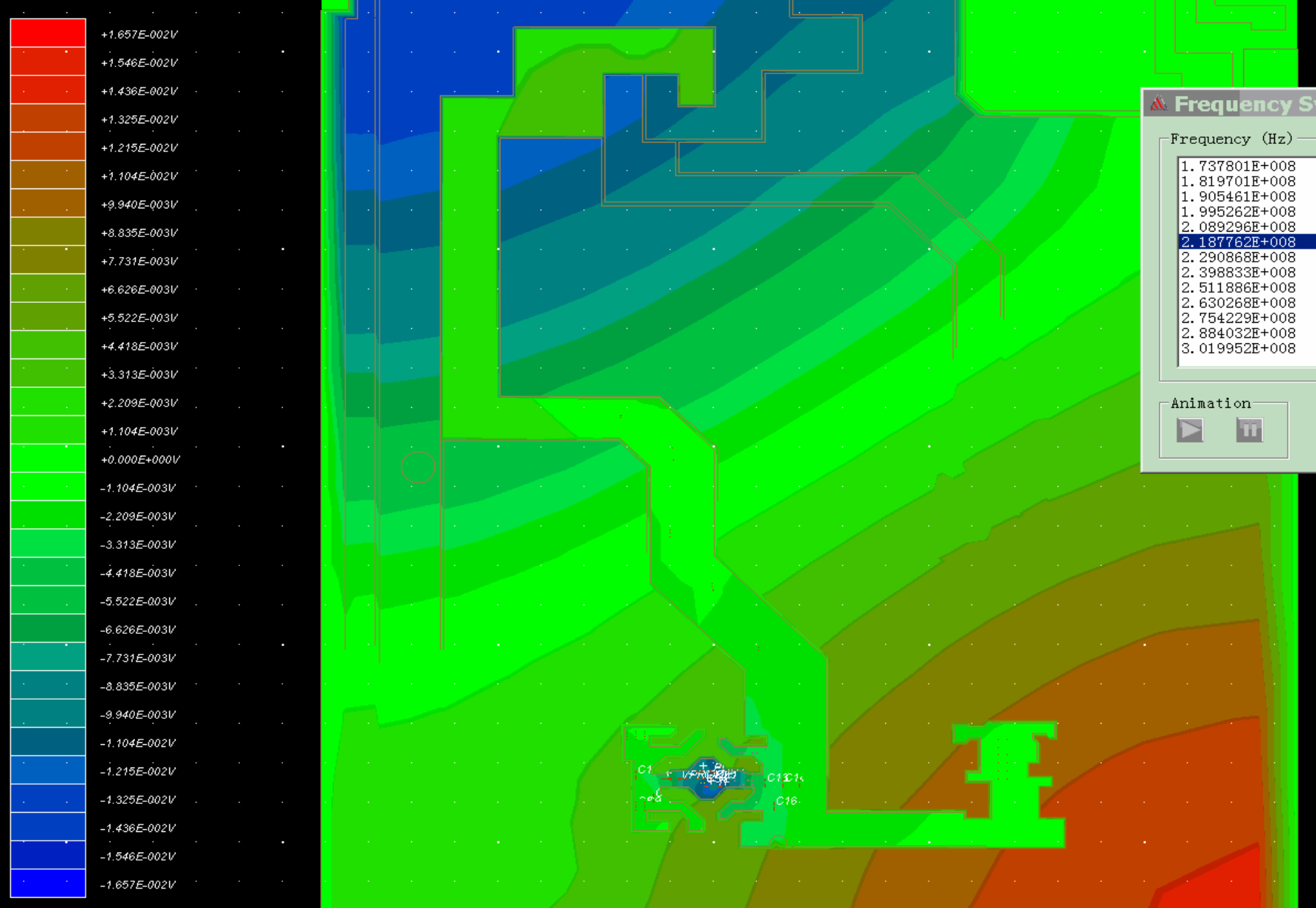
# S-Parameter Magnitude Plot



● S parameter vs. frequency at probe point

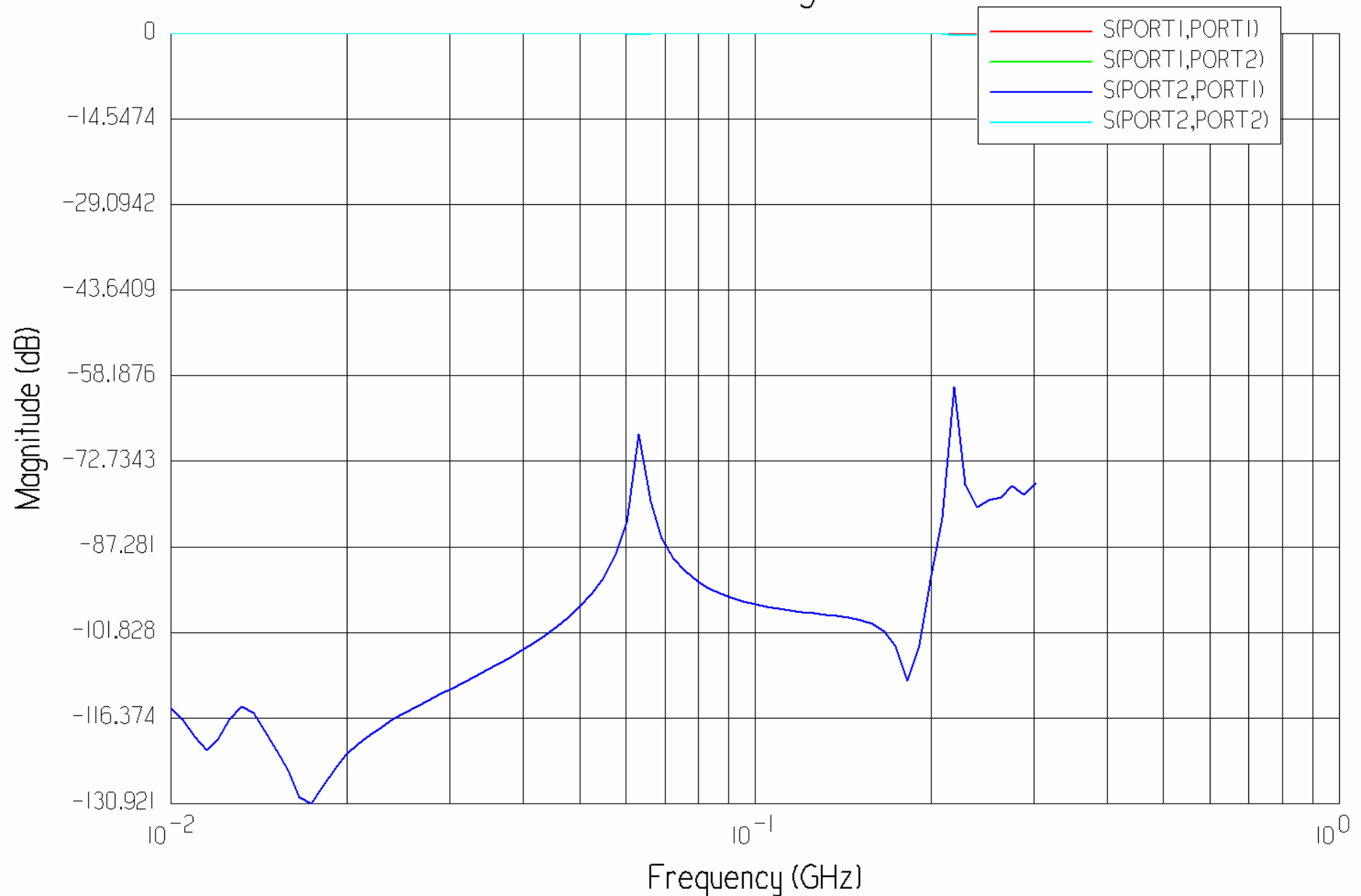


● Add probe and port for plane crosstalk analysis



# Crosstalk between split planes

# S-Parameter Magnitude Plot



● S parameter for split plane crosstalk

- Solve power and ground related problems BY DESIGN with SIwave.

The background is a dark blue gradient. It features several black lines of varying thickness and orientation, some crossing each other. A prominent, thick black diagonal shape runs from the top center towards the bottom right. The text 'Thanks a lot!' is centered in the upper half of the image in a bright yellow font.

Thanks a lot!