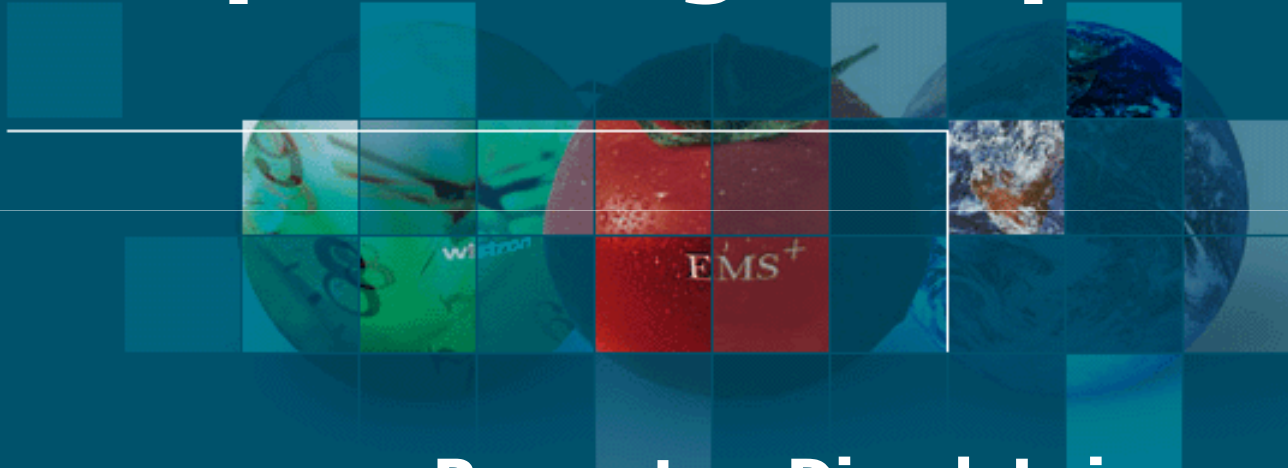


“Achieve optimized power delivery using Adaptive target impedance”



Presenter: Dirack Lai

2007/10/04

Wistron Corporation

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Vision of Wistron Corp.



“To be the leading provider of Design, Manufacturing and After-sales Service support for ICT products.”

WISTRON Corp. Products



Mobile PC



Personal communication devices



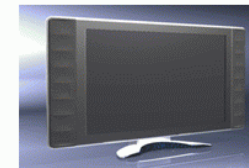
Server System
Storage System
VoIP phone
IPC/Monitor



Desktop PC,
CLD PC



Broadband Streaming



LCD-TV



Game Console

- **EBG (Enterprise Business Group)**
Server System/Motherboards, Storage System
IP Phone, Video Phone, PoE Accessory
Industry application computers
- **MBG (Mobile Business Group)**
Mobile PC/Notebook/Laptop
PDA/Smart Phone/GPS Handheld
- **DBG (Digital Business Group)**
Desktop PC, LCD TV, Game Console



Agenda

- ◆ Design Overview
- ◆ How to define Adaptive Target impedance ?
- ◆ Power/Ground geometry
- ◆ Decoupling capacitors placement

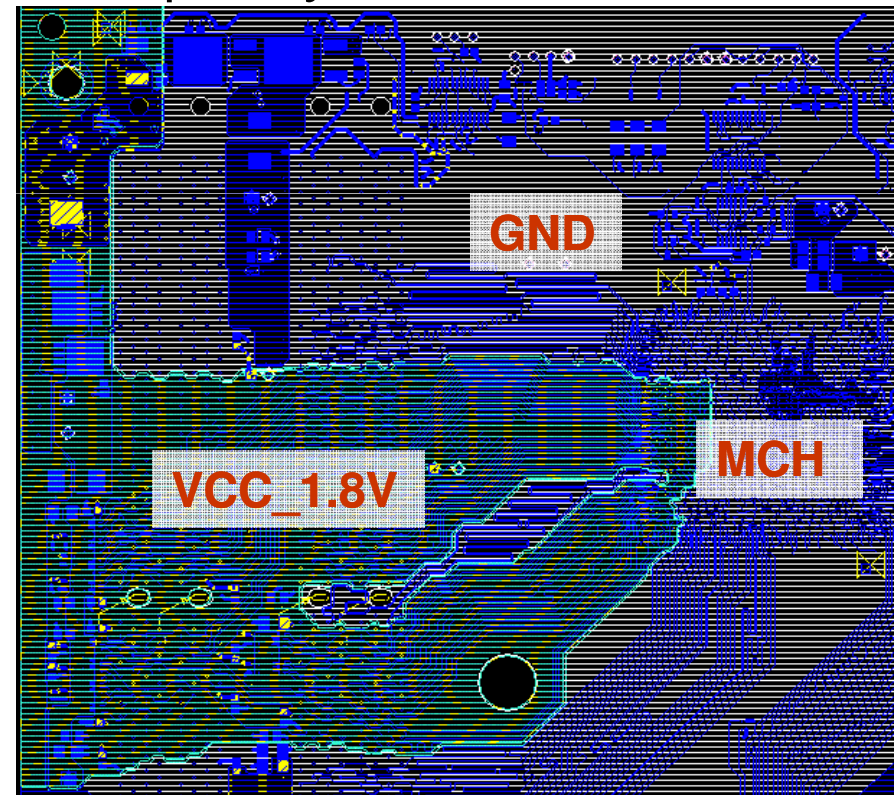
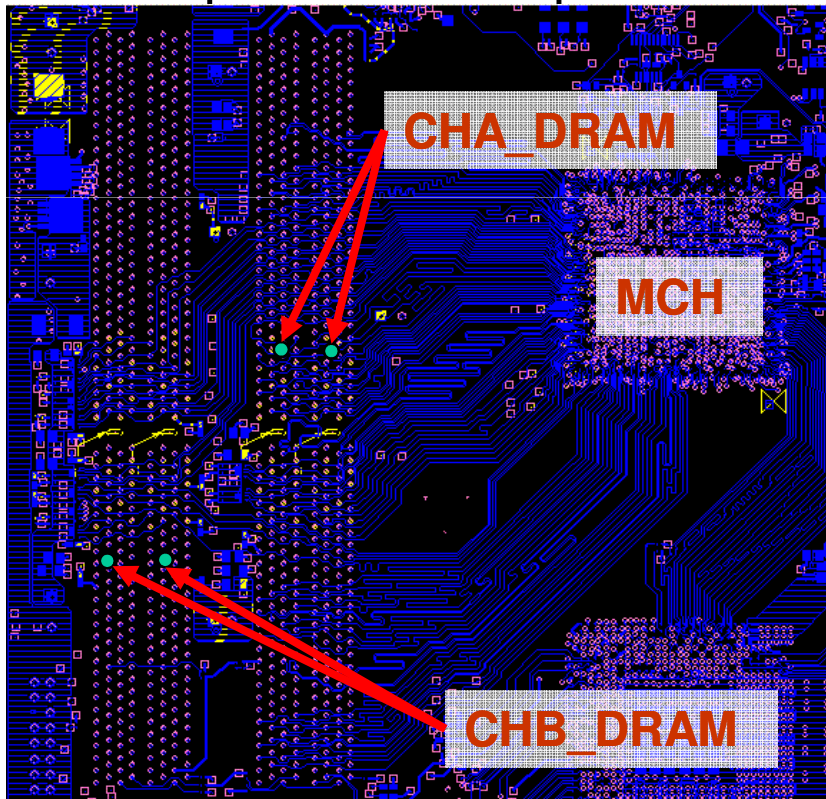


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PCB Layout Structure

- ◆ High-speed signals are routed between MCH and DIMM.
 - ◆ Minimize noise voltage distribution on the VCC/GND plane pair
 - ◆ Design of this Pwr/Gnd plane is the most important aspect of design
 - ◆ Low power bus impedance over frequency



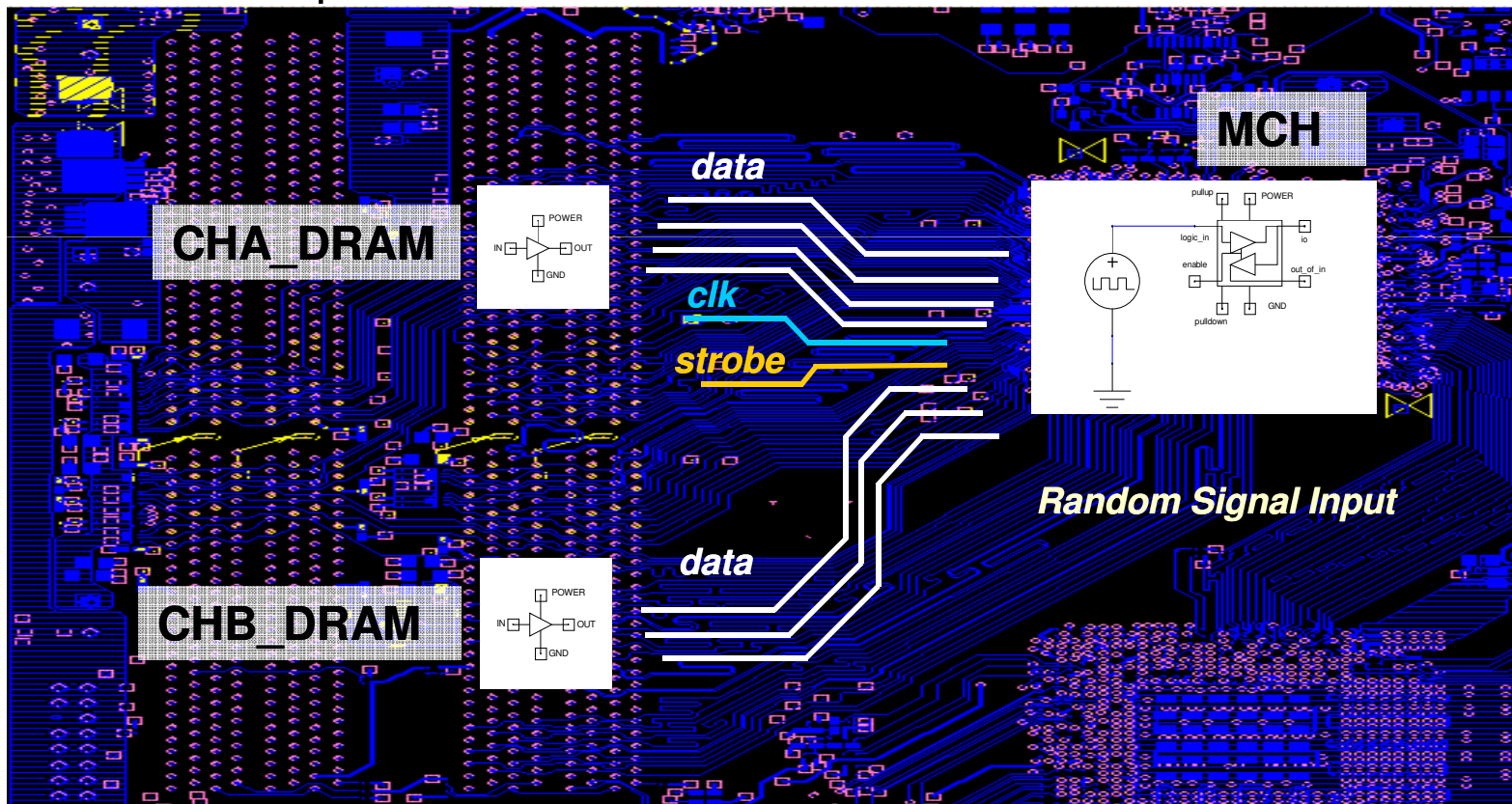


Agenda

- ◆ Design Overview
- ◆ How to define Adaptive Target impedance ?
- ◆ Power/Ground geometry
- ◆ Decoupling capacitors placement

Define Target Impedance

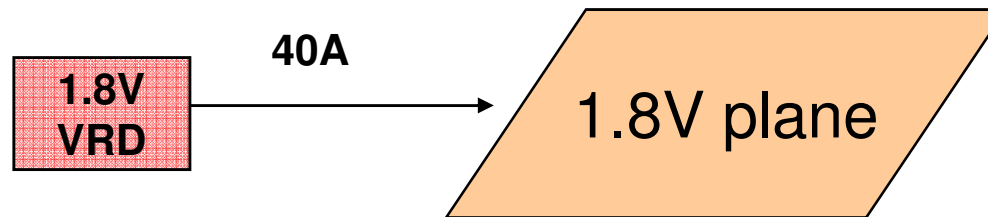
- ◆ Target Impedance
 - ◆ Get TX/Rx IBIS models for MCH and DRAM modules
 - ◆ Use Random Signal Input from MCH
 - ◆ Get current profile



Target Impedance Calculation

$$Z_{\text{Target}} = \frac{(\text{Power_Supply_Voltage}) \times (\text{Allowed_Ripple})}{\text{Current}}$$

Example:



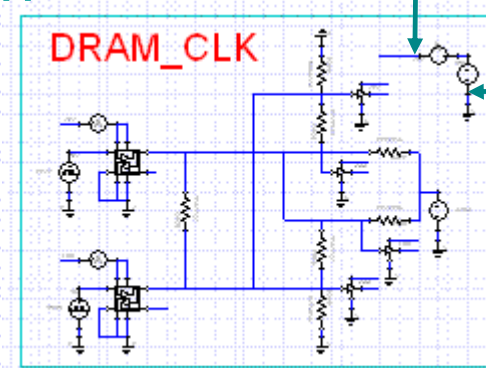
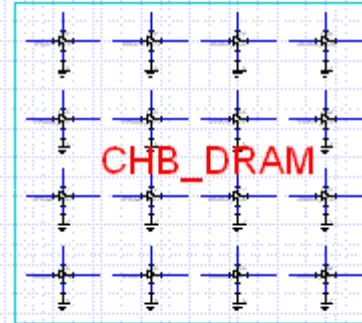
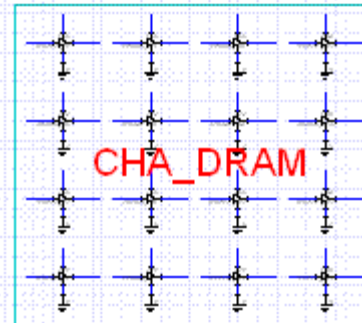
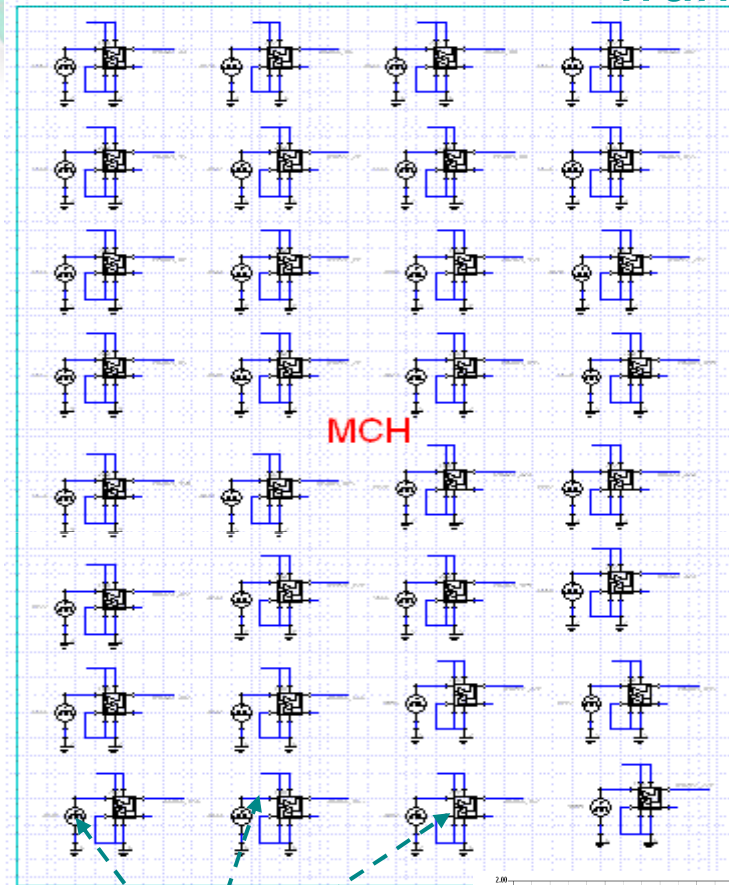
$$Z_{\text{Target}(1.8\text{V})} = \frac{(1.8\text{V}) \times (5\%)}{40\text{A}} = 2.25\text{m}\Omega$$

Target Impedance is the goal that designer should hit !!!

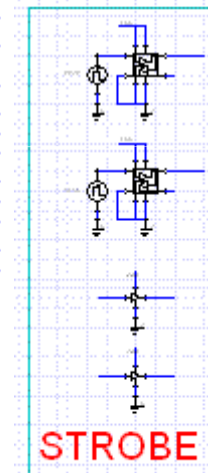
Real Current Profile

Transient simulation

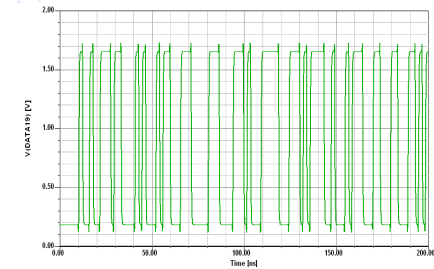
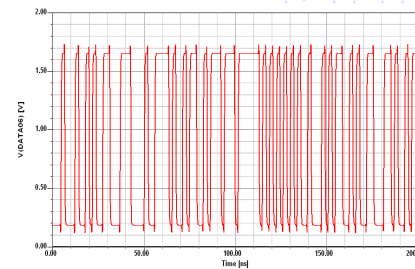
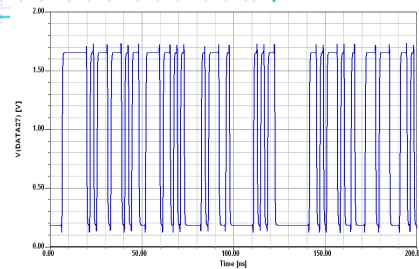
Current Probe



DC +1.8V

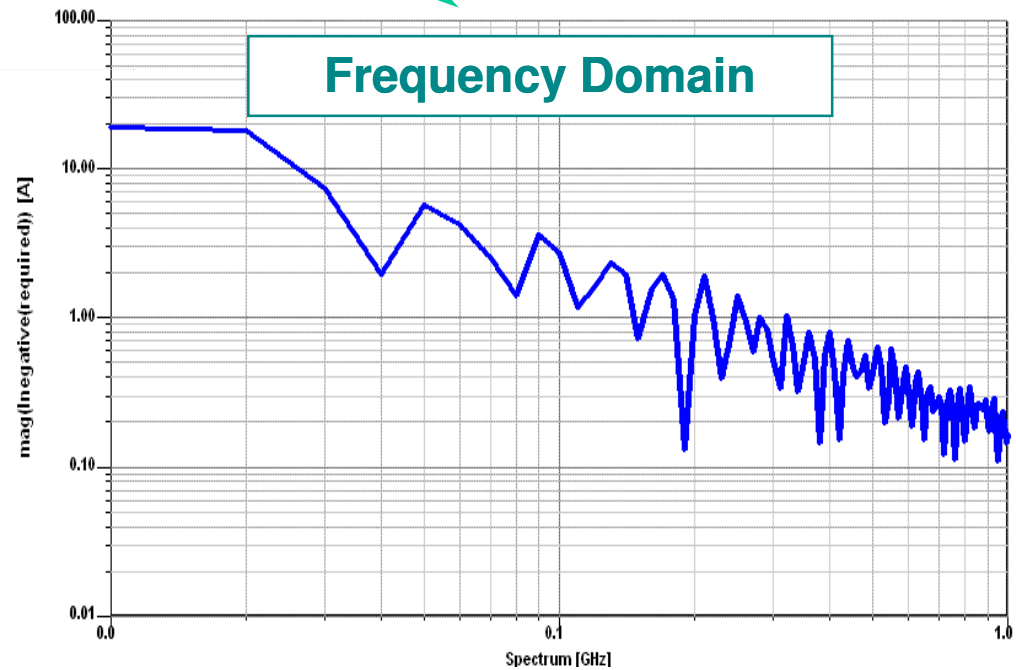
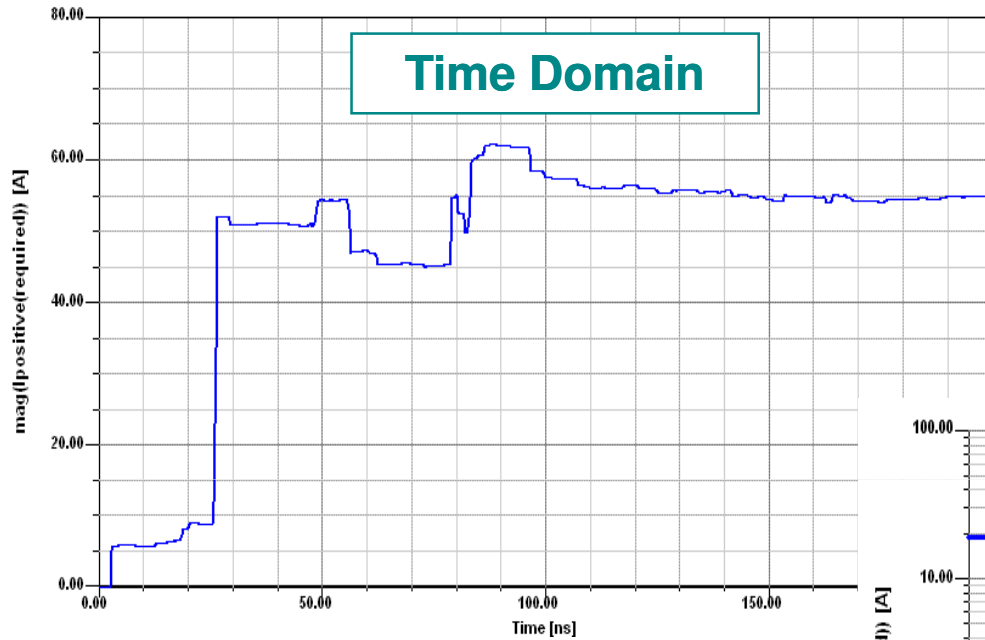


Random signal input from MCH





Getting Real Current Profile

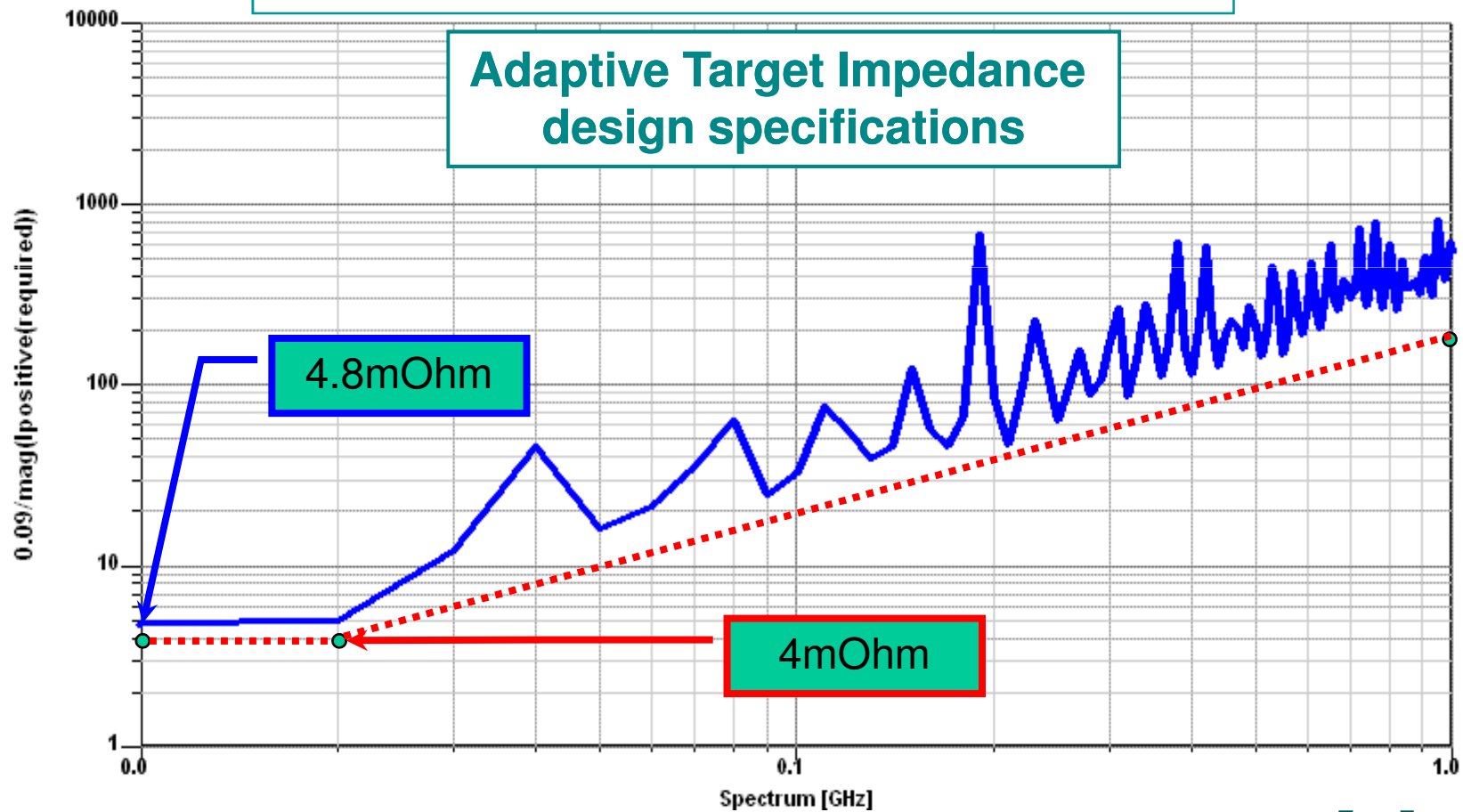




Define Target Impedance

- +1.8V with 5% voltage variation = 0.09V

$$Z_{\text{Target}} = \frac{(\text{Power_Supply_Voltage}) \times (\text{Allowed_Ripple})}{\text{Current}}$$



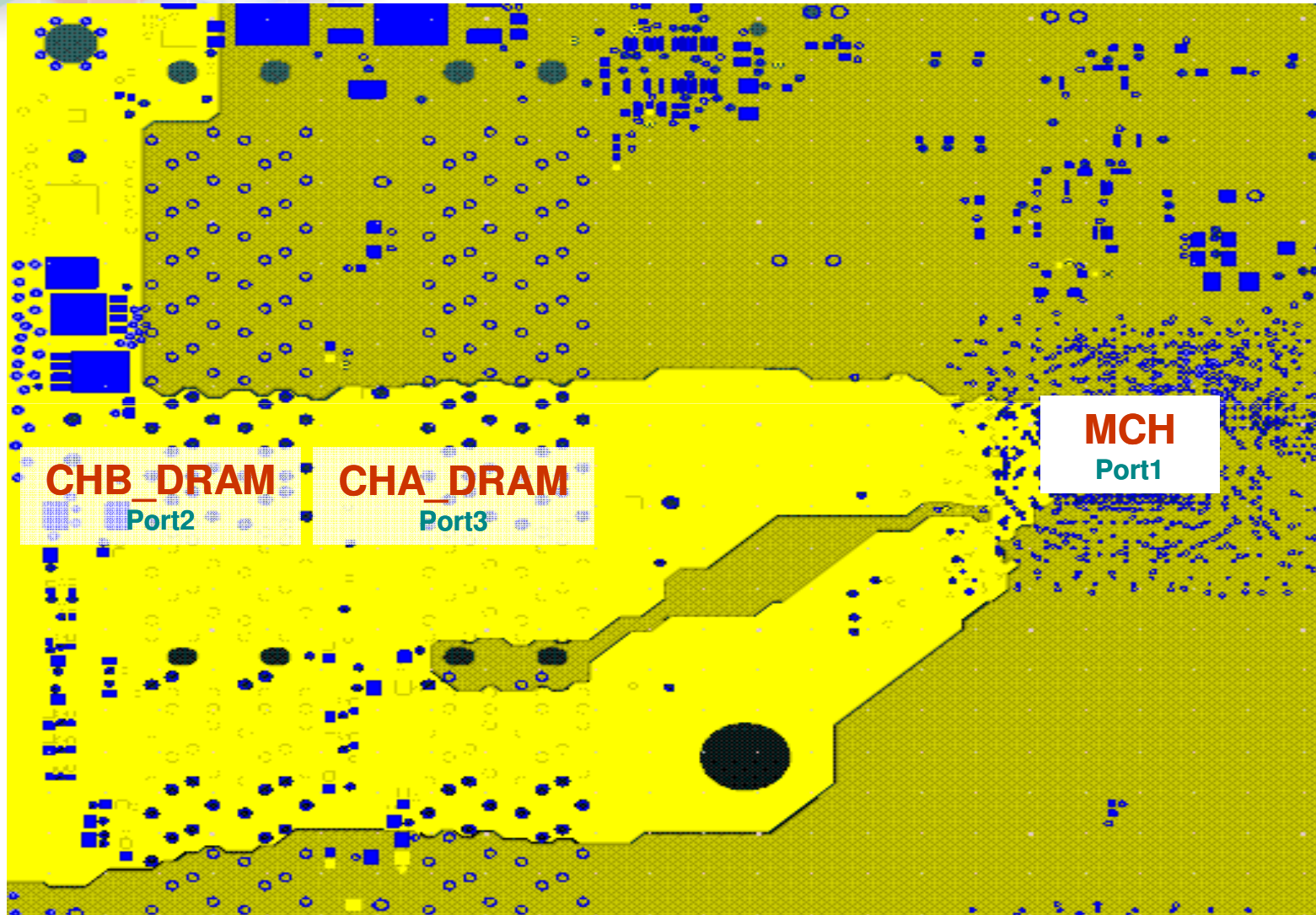


Agenda

- ◆ Design Purpose
- ◆ How to define Adaptive Target impedance ?
- ◆ **Power/Ground geometry**
- ◆ Decoupling capacitors placement

Target Impedance Simulations

- Place ports on pwr/gnd pins of CHA_DRAM, CHB_DRAM and MCH.

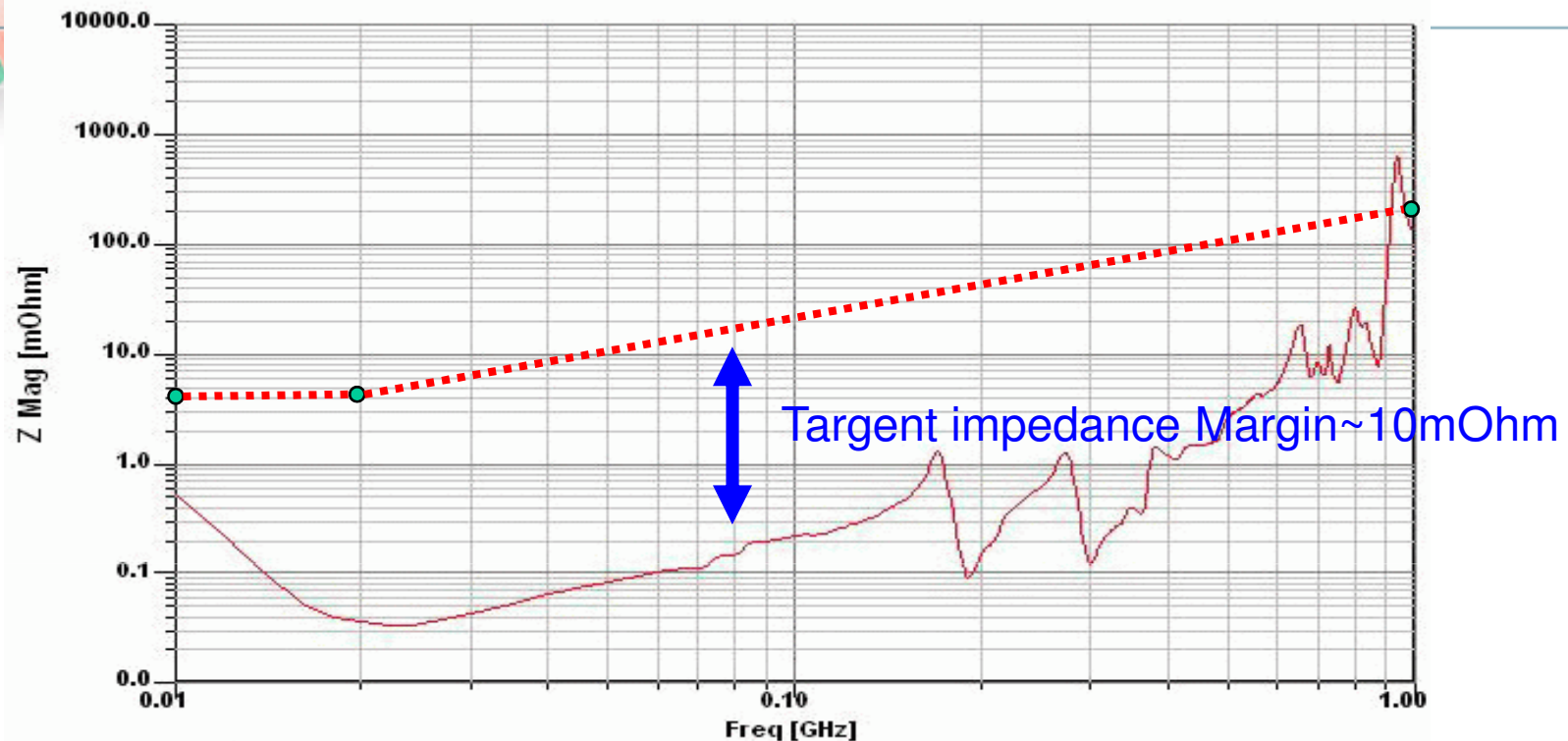




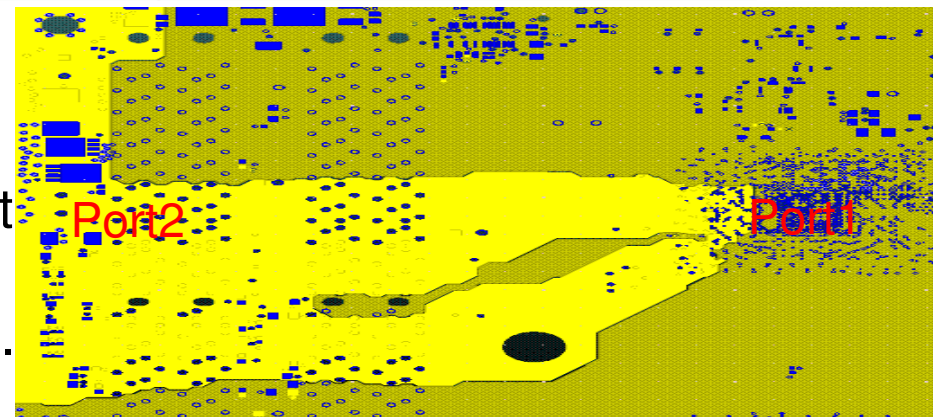
Agenda

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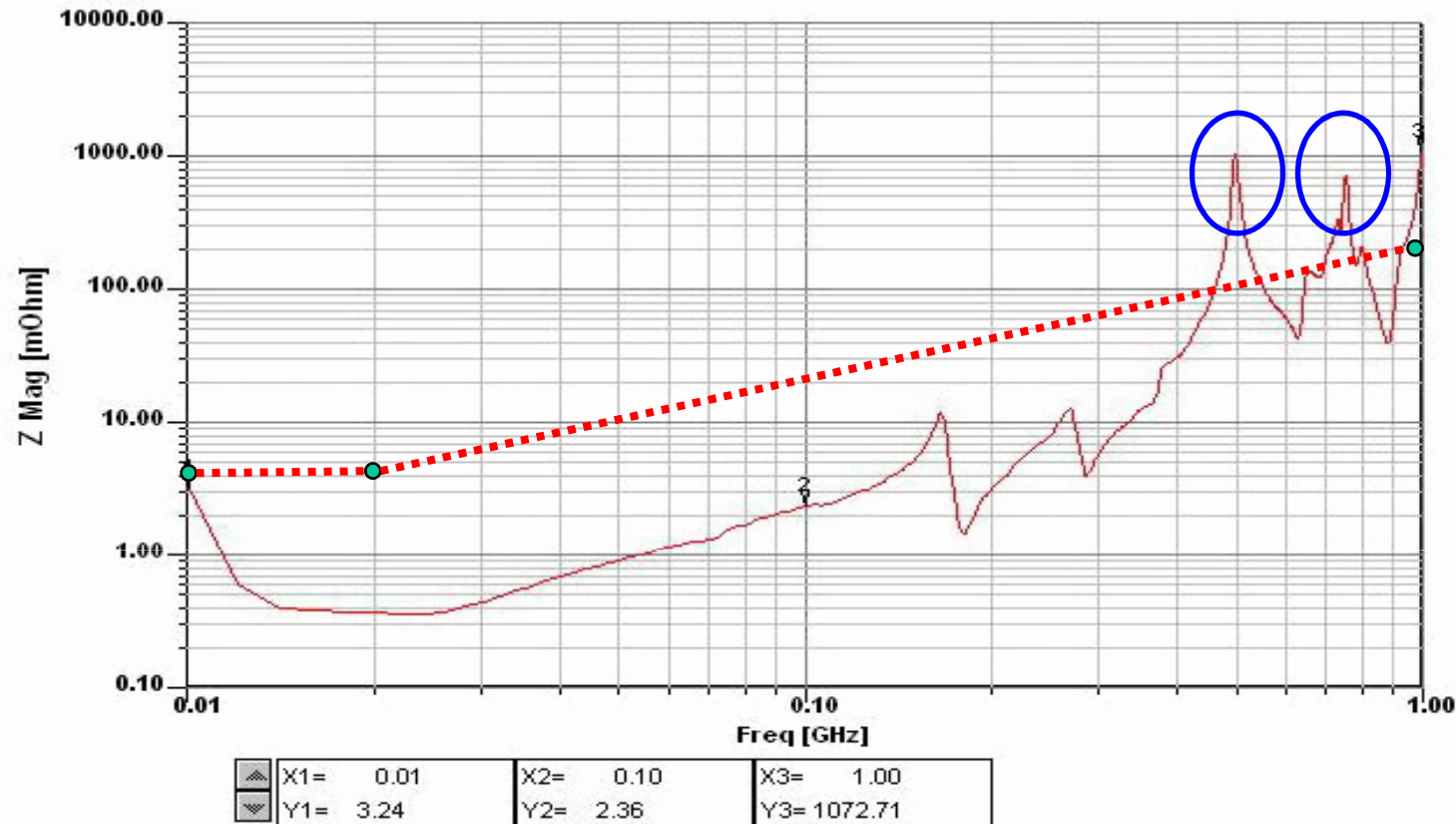
Decoupling Capacitors Strategy - step 1



- ◆ Adding all 46 *de-caps* near IC pwr/gnd pins (*PI and SI caps*)
- ◆ Compare SIwave simulation result to the target impedance limit line for next step *de-caps* optimization.
- ◆ The target impedance is too low.



Decoupling Capacitors Strategy - step 2



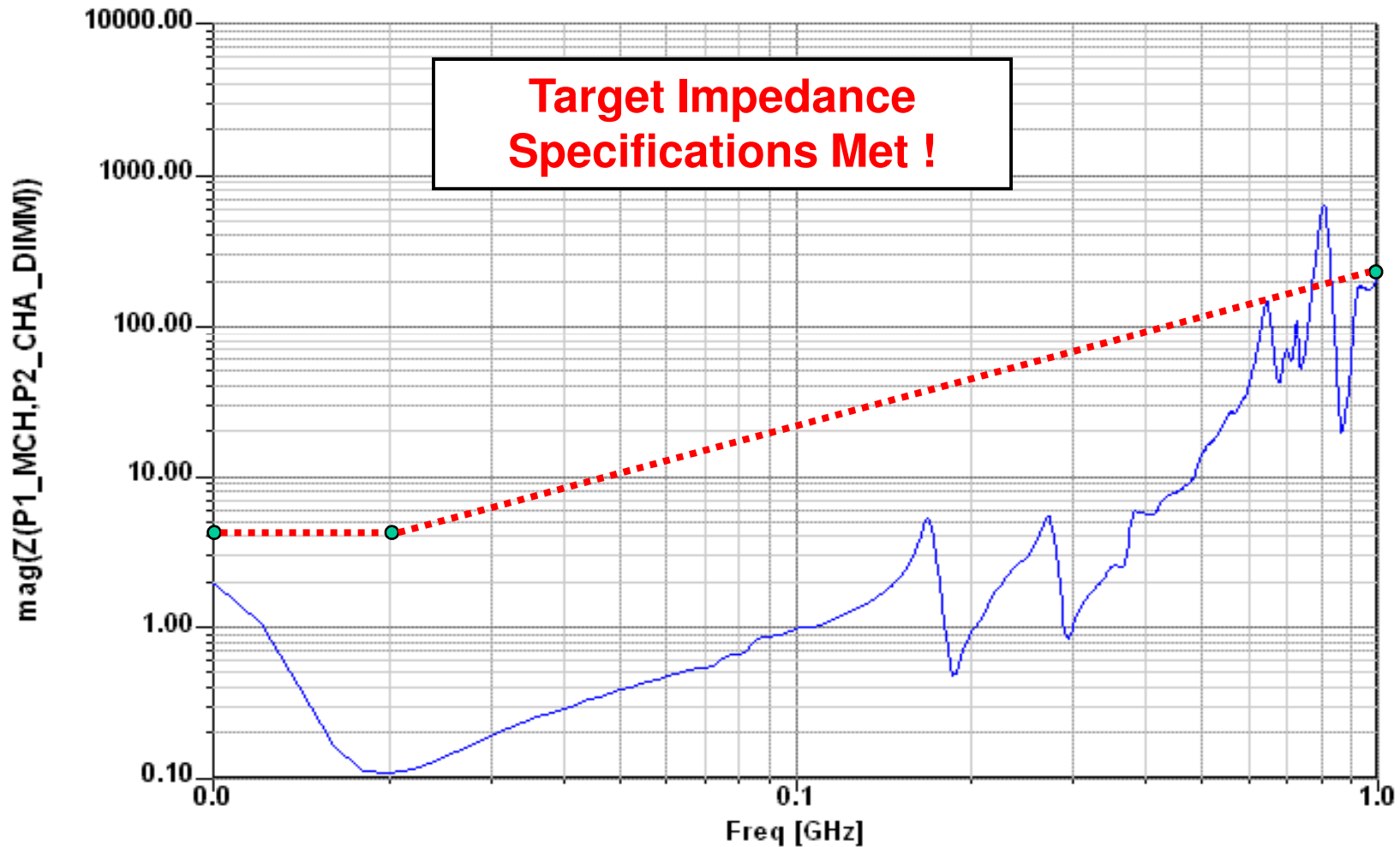
- ◆ Remove 21 *de-caps* near IC pwr/gnd pins (*PI and SI caps*)
- ◆ The target impedance reduce to ~ 5mOhm.
- ◆ There're two peaks near 500MHz and 650MHz.
- ◆ This result leads to resonant mode analysis at these two frequency and add some 0.1uF de-caps back as next step.



Decoupling Capacitors Strategy

Final Design

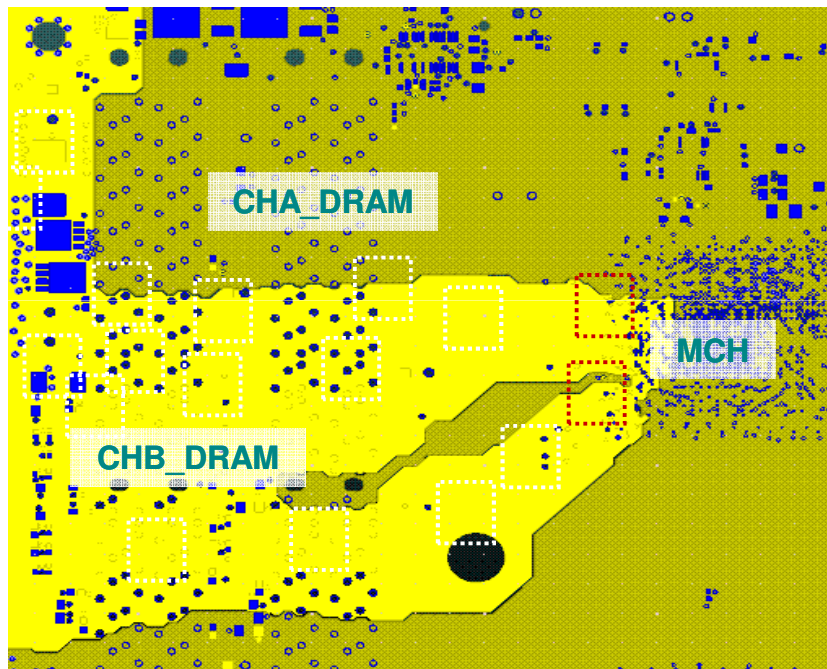
- ◆ Target Impedance Simulations





Design Comparison

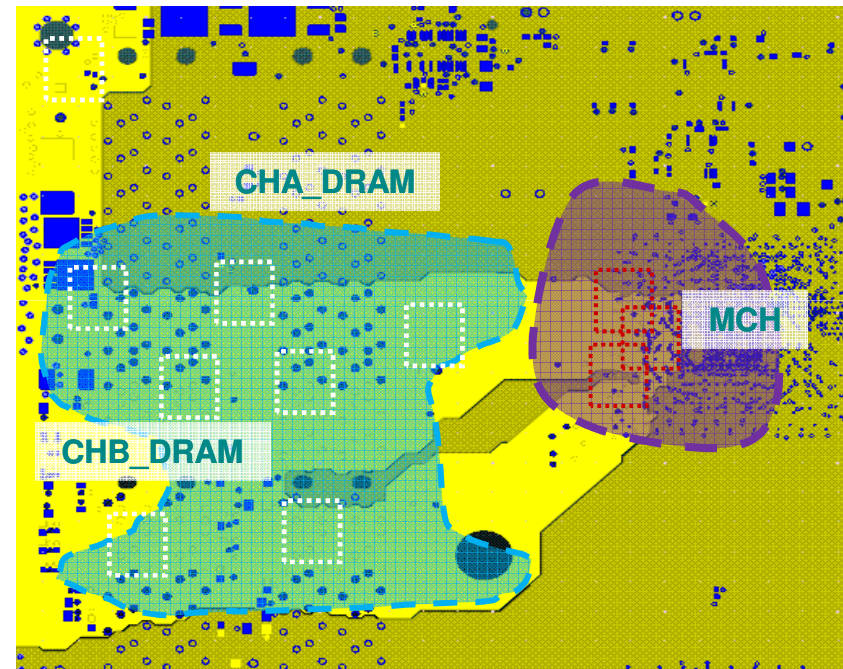
- ◆ Modified design overview
 - ◆ Reduced number of capacitors
 - ◆ Reduced system cost



Original Design - Total 46 Caps

PI & SI Caps

C1,C2,C3 PI Caps



Modified Design - Total 29 Caps

Total Quantity Savings $(46-29) / 46 = 36.9\%$



Summary

- Achieving *Adaptive Target Impedance* Specifications is critical for overall system performance
- Specific design approaches for achieving *Adaptive Target Impedance* were shown here.
 - Decoupling capacitor strategy
 - Location, Value
- *Adaptive Target Impedance* analysis and “What-if...” type analysis is utilized using:

SIWAVE™
NEXXIM®
DESIGNERSI™



Thank You!