



Ansoft Workshop 2007

# Chip-Level Power Integrity

## :Trend and Challenge for On-chip PDN Design

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**Hynix Semiconductor Inc.**  
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9 October 2007



## Outline

- Trend and Challenge
- PDN Design Issues
- On-chip PDN ( $\Delta V$ , Current Flow)
- A Design Example
- Things To Need To be Prepared

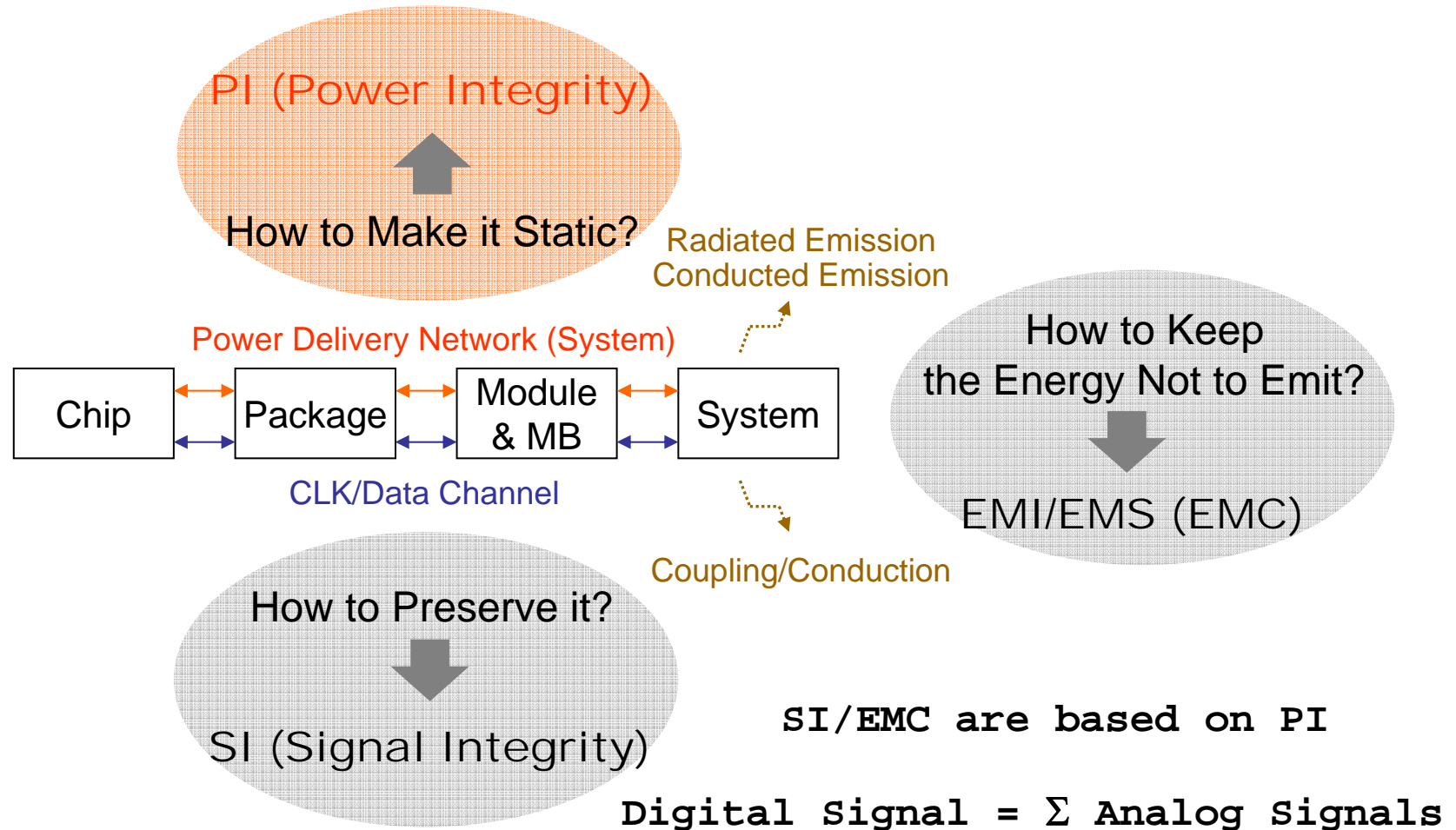


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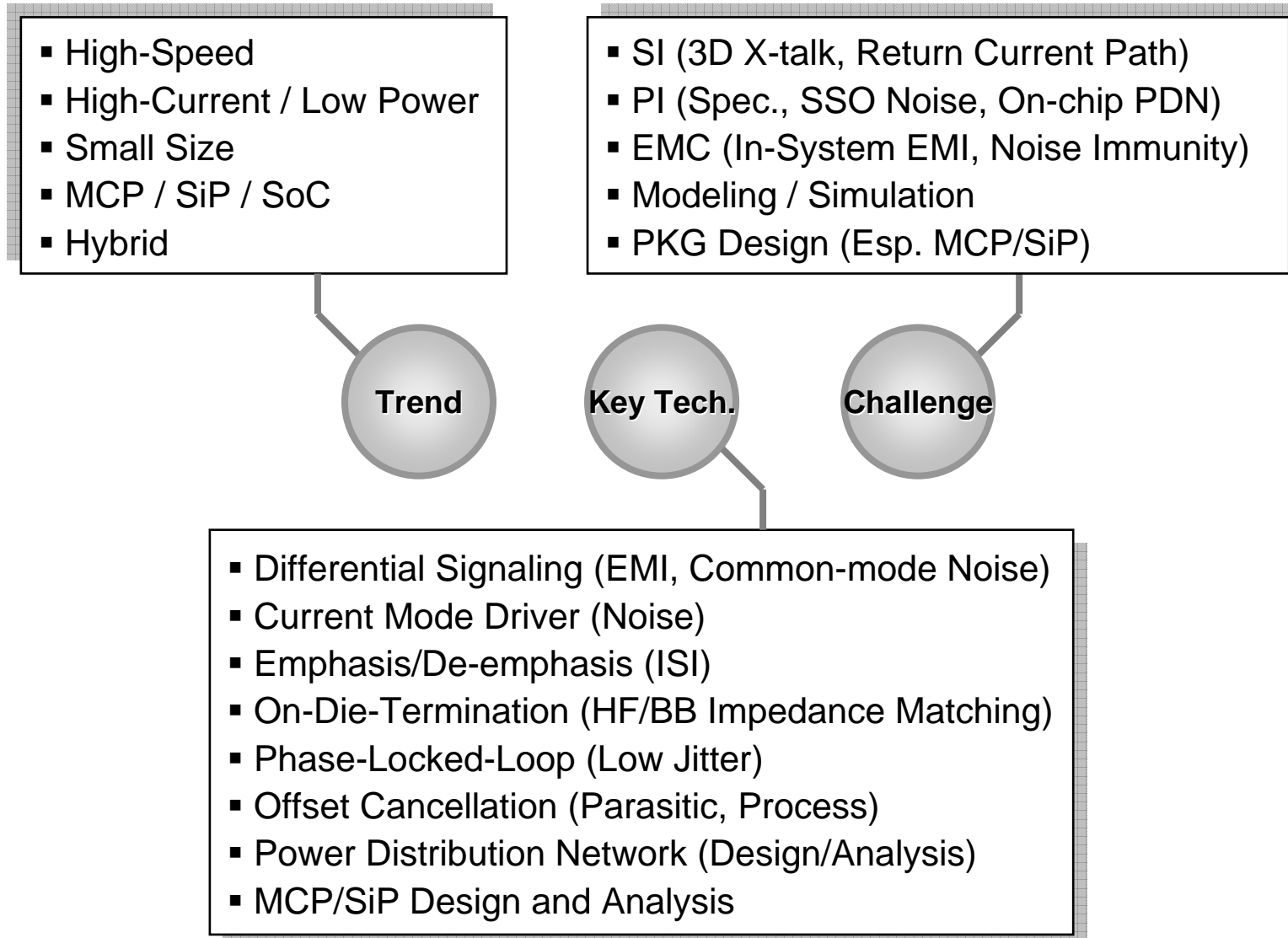


# Three Key Elements of Digital System Integrity



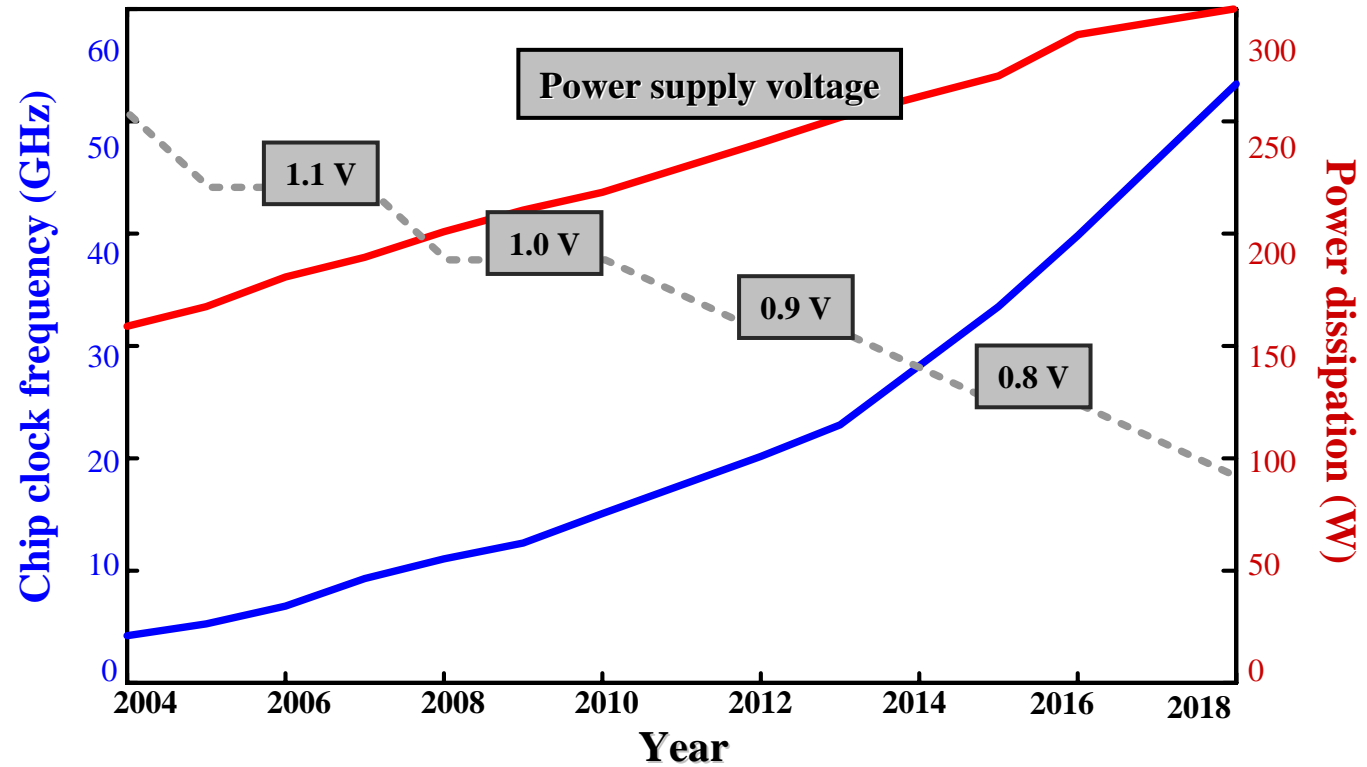


## Trend and Challenge – (1)





# Trend and Challenge – (2)



\* ITRS (International Technology Roadmap for Semiconductors)2003

Increase of SSN  
Decrease of Noise Margin

$$\uparrow \Delta V = Z \times \Delta I \uparrow$$

Increase of Current  
Increase of Clock Frequency

**Z (PDN Impedance): the only controllable parameter**

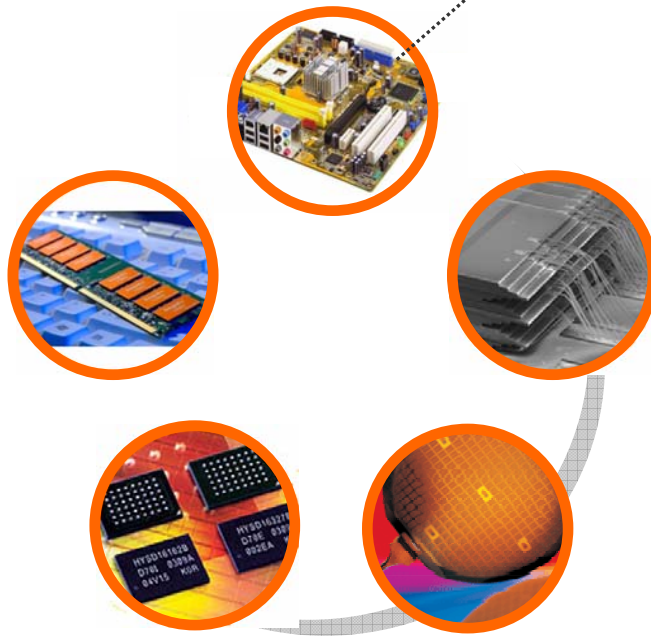


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# PDN Design Issues



## MCP/SiP

- ❑ More Serious PKG Issues
- ❑ Noise Coupling  
(C2C Direct Coupling, CE)
- ❑ EMS (In-system EMI)



# On-chip PDN Design

**Issues:** Voltage Drops (Static, Dynamic), SSO Noise, Power Domain Crossing, EMI/EMS

**Target:** Impedance ( $Z_{11}$ ,  $Z_{21}$ ), Return Current Path

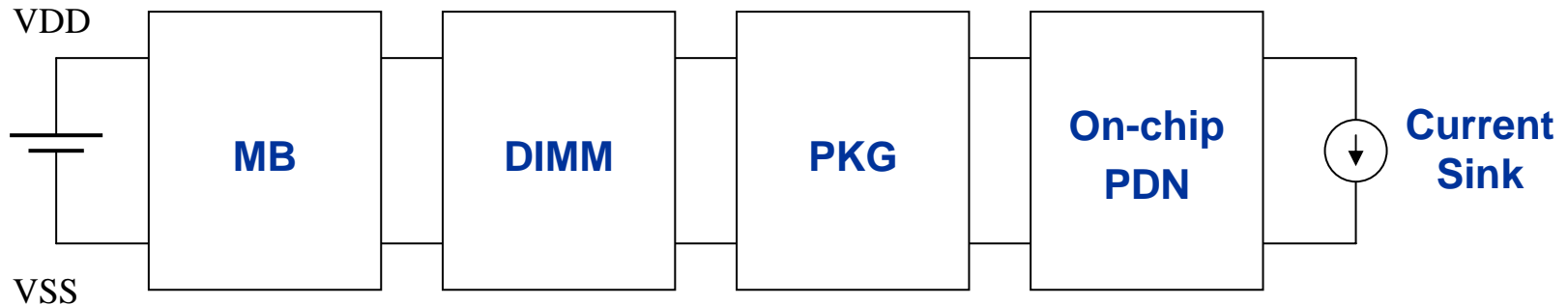
**Key Elements:** Pad (Location, Number), PKG, Power Mesh (Material, Width, Number), De-cap. (Size, Location, Frequency), Floor Plan

**Challenge:** Cost vs. Performance, Accuracy vs. Time (Modeling)

**Tool:** Excellent Tools are Available for Off-chip. However, **Not a Right One yet for On-chip** (only available for ASIC)



# PDN Modeling Challenges



## Modeling Scheme

**MB:** MHz 이하 Model, Cavity Resonance (수십MHz이상)

**DIMM:** 수십MHz 이하 Model, Cavity Resonance (수백MHz이상)

**PKG:** 수십MHz 이하 Model, Broadband Model (Off-chip Driving), 수백 개 이하의 Ports

**On-chip PDN:** Broadband Model, 수십만 개 이상의 Ports

**Current Sink:** Current Profile vs. MOS Model, 수십만 개 이상의 Ports

## Choose the Right Model to meet the Purpose

**Purpose:** PI, SI

**Target Frequency:** Current Sink Spectrum, Signal Spectrum

**Interest:** On-chip, PKG, DIMM



# Choose the Right Modeling Tool: Off-chip

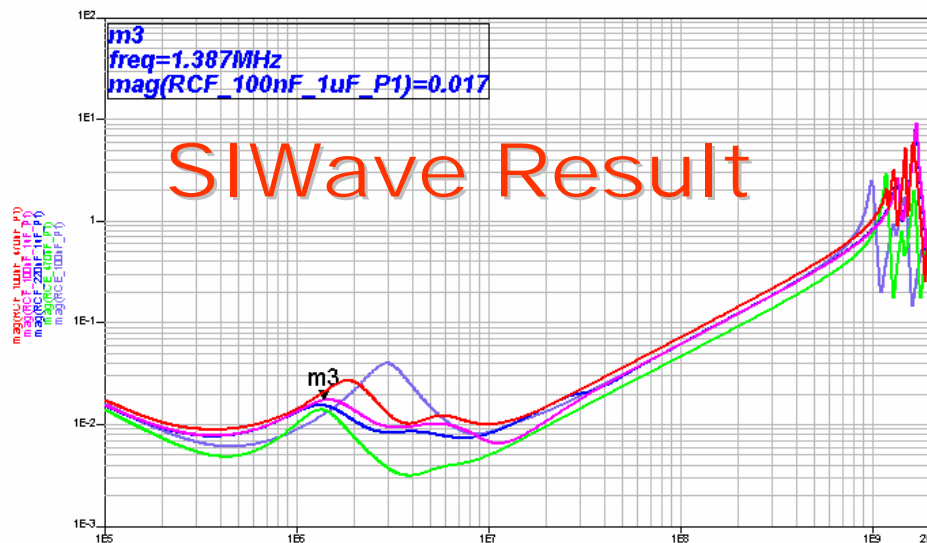
**Modeling:** Analysis + Model Generation

**Analysis:** Dimensions (2D, 2.5D, 3D), Domain (Frequency, Time)

**Model Generation:** Lumped , S-parameters, Macro, Analytical, Scalable

**Tool Requirement:** Speed, Accurate for Complex Structures,  
Several Hundreds of Ports

**Model Requirement:** Not Heavy, Broadband



## DDR2 Module PDN Analysis

Why SIWave in Mudule Analysis?  
: To Require Broadband, Speed,  
Multi-layer (Cavity Resonance),  
Frequency-dependant, Accurate



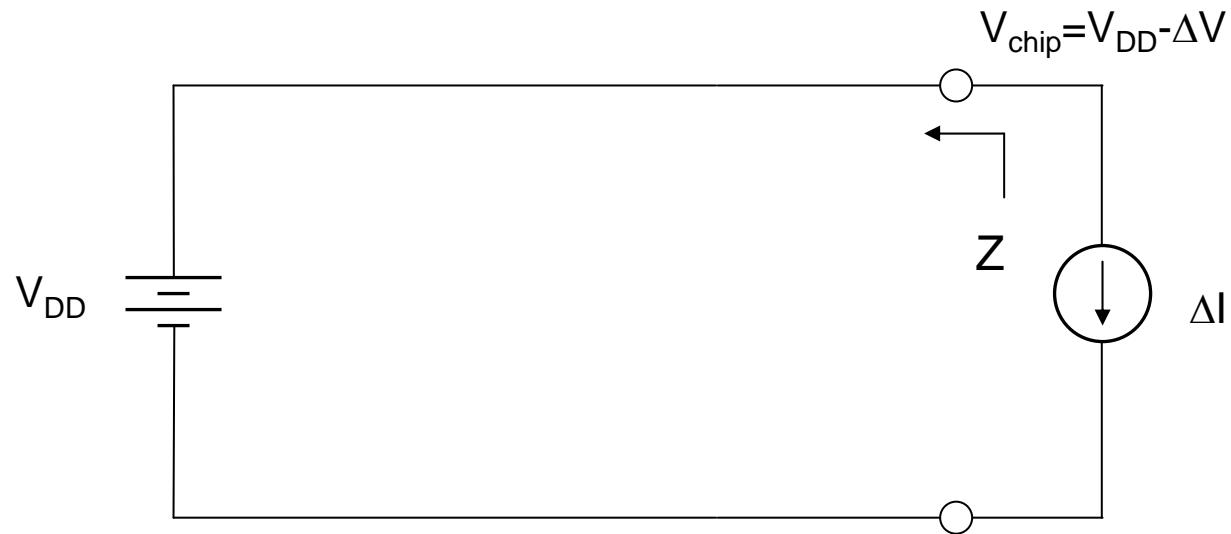
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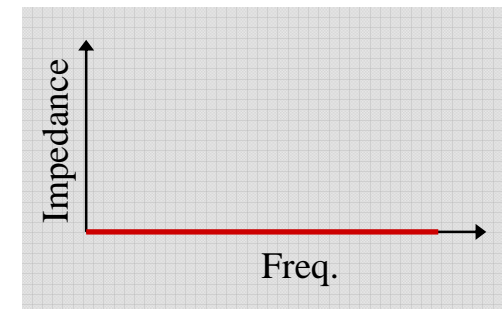


# Generation and Reduction of Power Noise – (1)

Ideal PDN



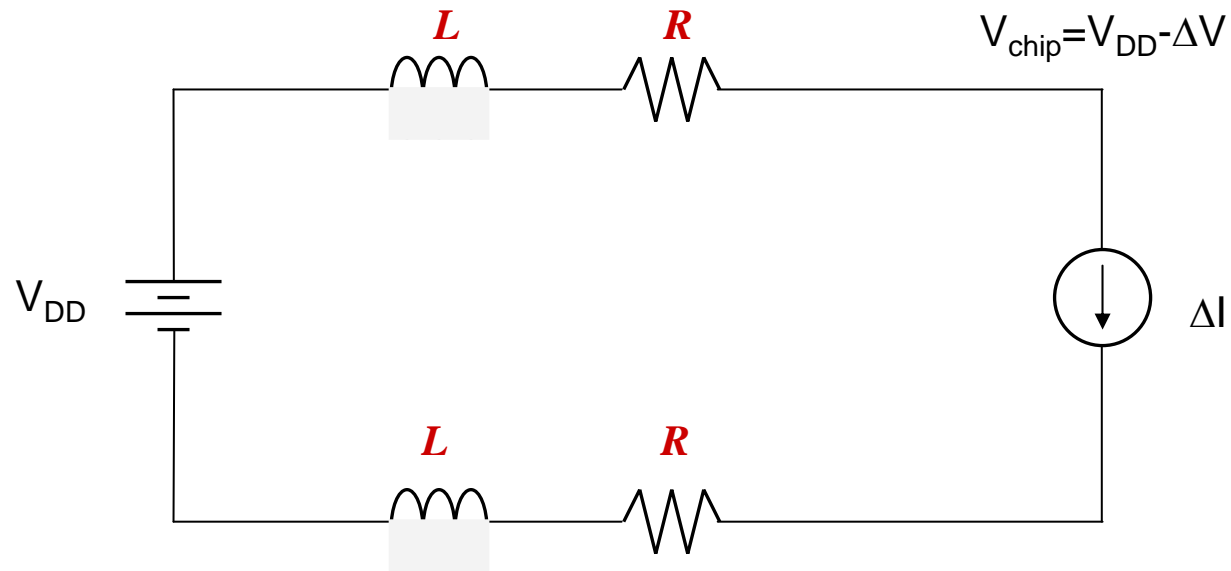
$$\Delta V = \Delta I \times Z = 0$$



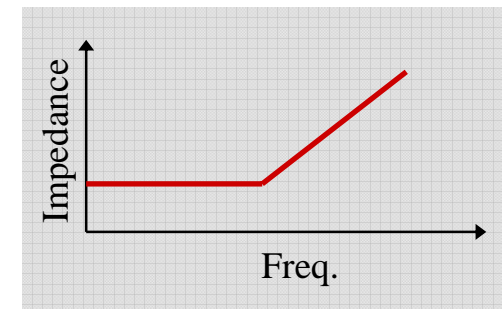


# Generation and Reduction of Power Noise – (2)

Non-Ideal PDN w/ R and L



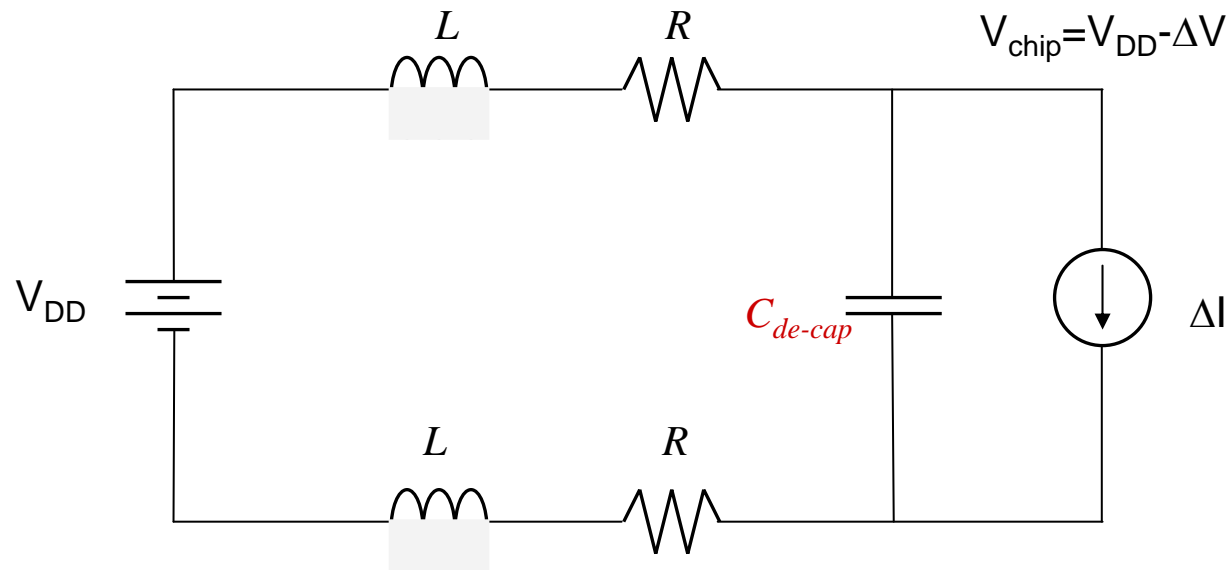
$$\Delta V = \Delta I \times (2R + 2j\omega L)$$





# Generation and Reduction of Power Noise – (3)

Non-Ideal PDN w/ Ideal De-cap.



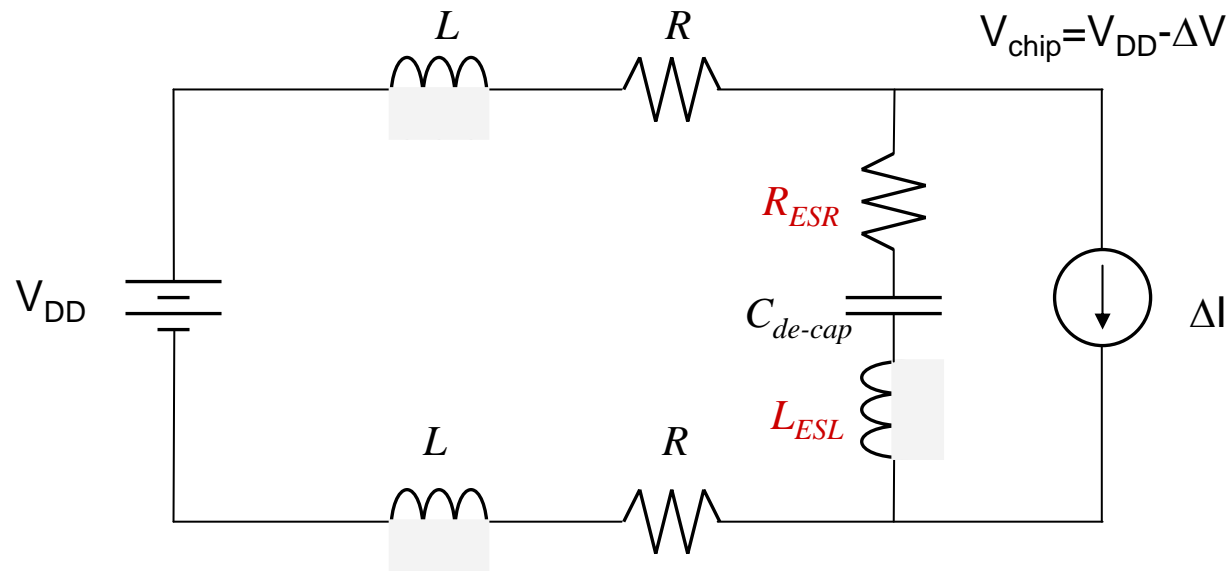
$$\Delta V = \Delta I \times (2R + 2j\omega L) // (1/j\omega C)$$



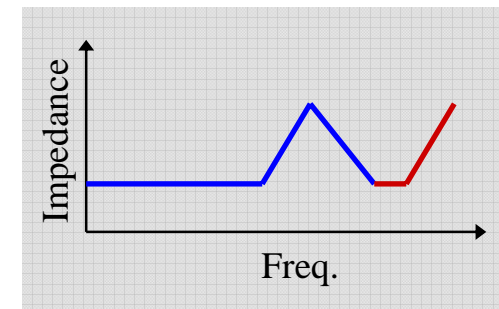


# Generation and Reduction of Power Noise – (4)

Non-Ideal PDN w/ Non-Ideal De-cap.



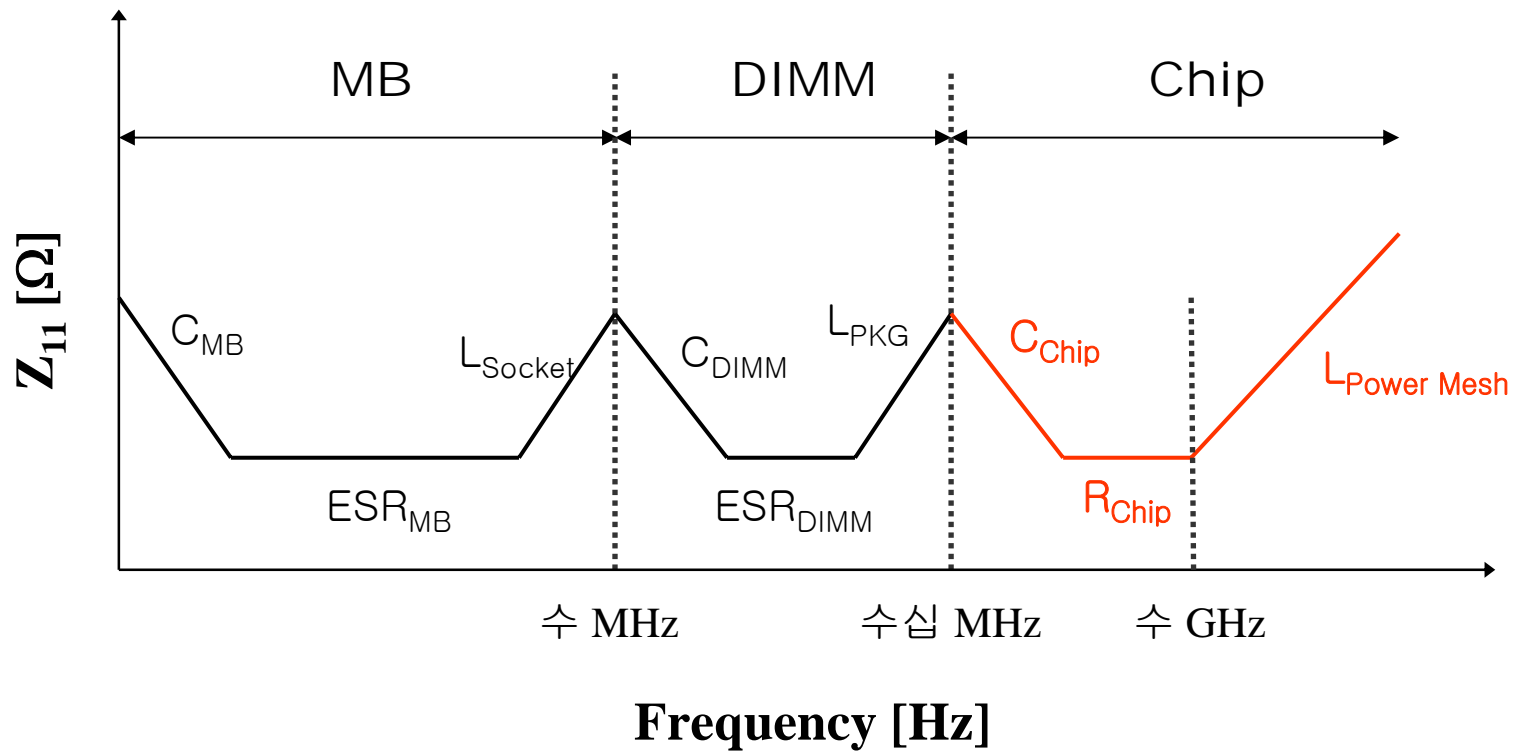
$$\Delta V = \Delta I \times (2R + 2j\omega L) // (R_{ESR} + j\omega L_{ESL} + 1/j\omega C)$$





# Typical On-chip PDN Impedance

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# On-chip Voltage Drops

**Frequency:** Static, Dynamic (DvD)

**Periodicity:** SSN, SSO Noise

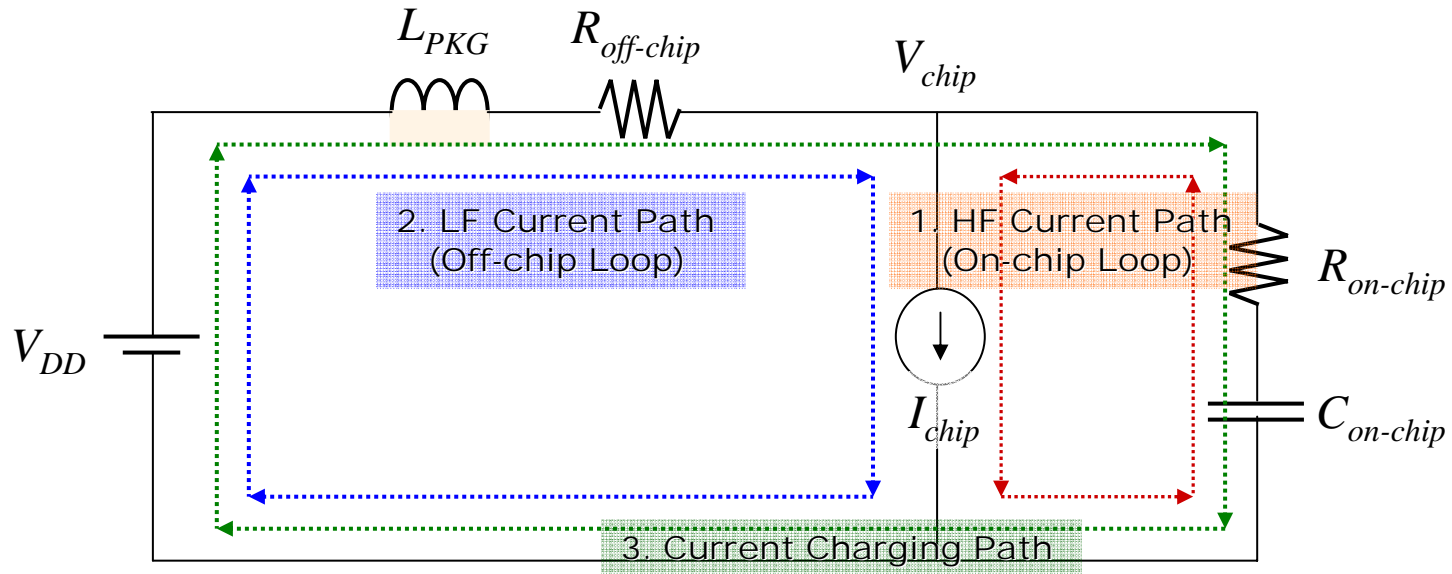
**Current Driving:** On-chip, Off-chip

**PWR/GND Noise Phase:** In-phase, Out-of-Phase

**Current Sink Time:** Resonance (if unsynchronized and periodic)



# Simple PDN Model and Current Flow: On-chip Driving



$L_{PKG}$ : Package Inductance

$R_{off-chip}$ : Current Sink로부터 Off-chip Current Loop의 저항 ( $R_{mesh} + R_{PKG} + \dots$ )

$R_{on-chip}$ : Current Sink로부터 On-chip Current Loop의 저항 ( $R_{mesh} + ESR$ )

$C_{on-chip}$ : On-chip De-coupling Capacitor

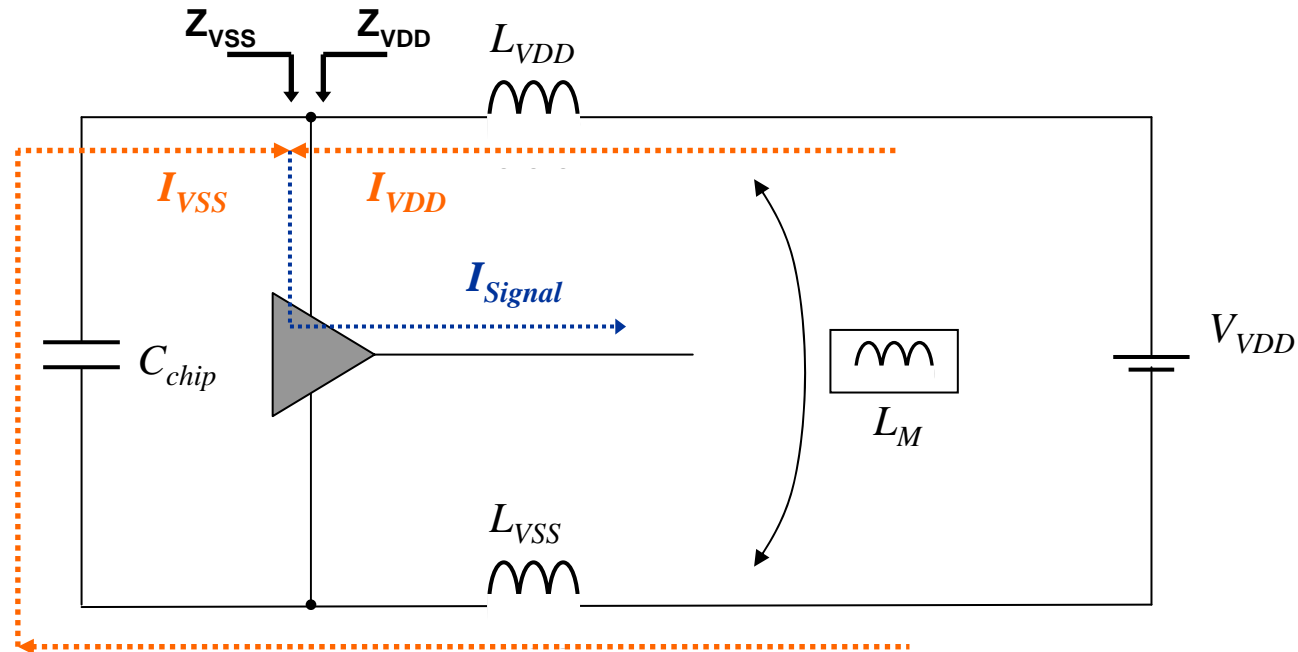
$I_{chip}$ : On-chip Current Consumption

$V_{DD}$ : External Supply Voltage

$V_{chip}$ : Voltage Level at Current Sink Location



## Simple PDN Model and Current Flow: Off-chip Driving



$$\Delta I_{VDD} = \Delta I_{Signal} \cdot Z_{VSS} / (Z_{VDD} + Z_{VSS})$$

$$\Delta I_{VSS} = \Delta I_{Signal} \cdot Z_{VDD} / (Z_{VDD} + Z_{VSS})$$

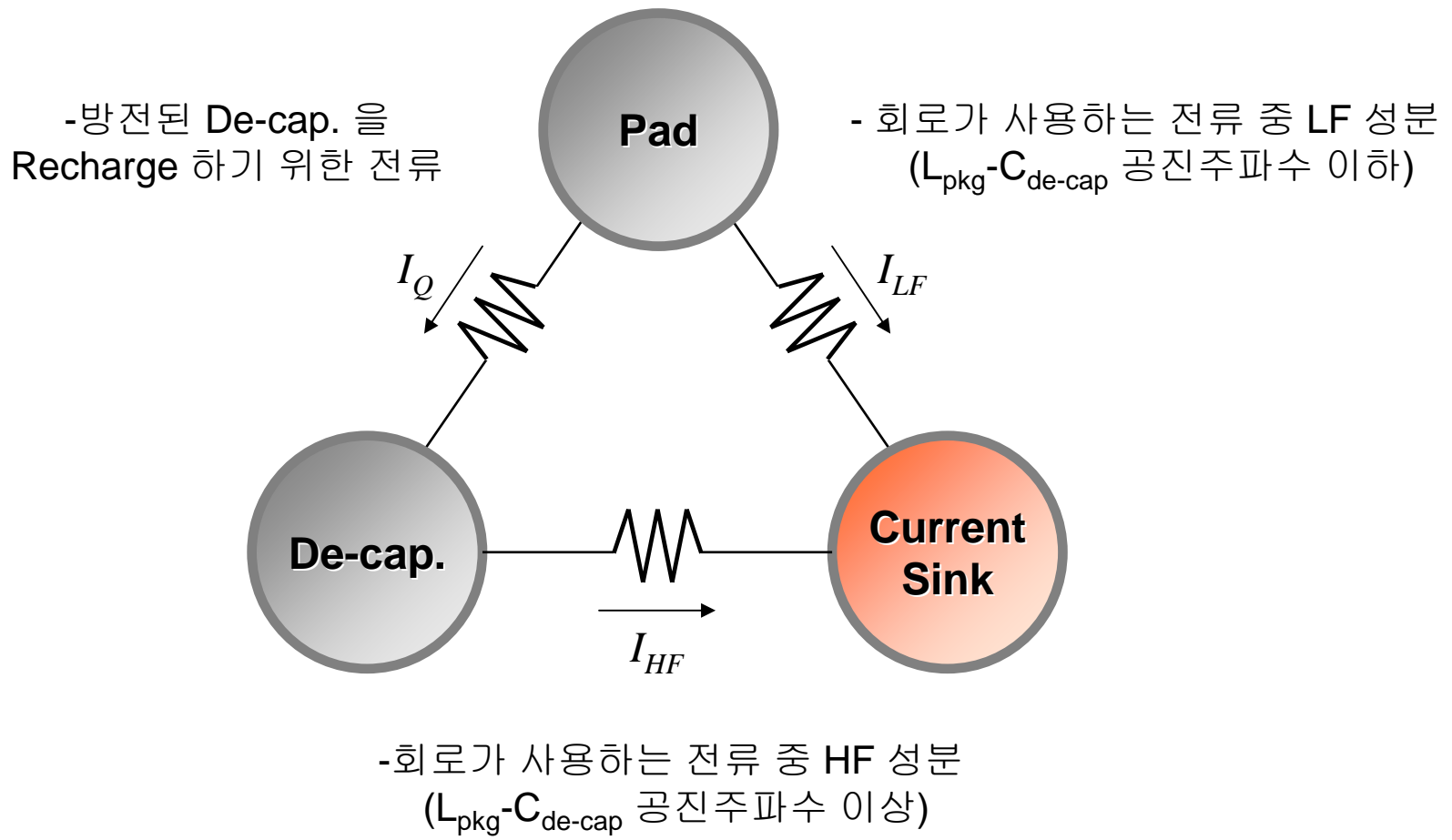
$$\Delta V_{VDD} = \Delta I_{VDD} \cdot j\omega L_{VDD} + \Delta I_{VSS} \cdot j\omega L_M$$

$$\Delta V_{VSS} = \Delta I_{VSS} \cdot j\omega L_{VSS} + \Delta I_{VDD} \cdot j\omega L_M$$

In-phase



# Classification of Power Mesh by Current Flow



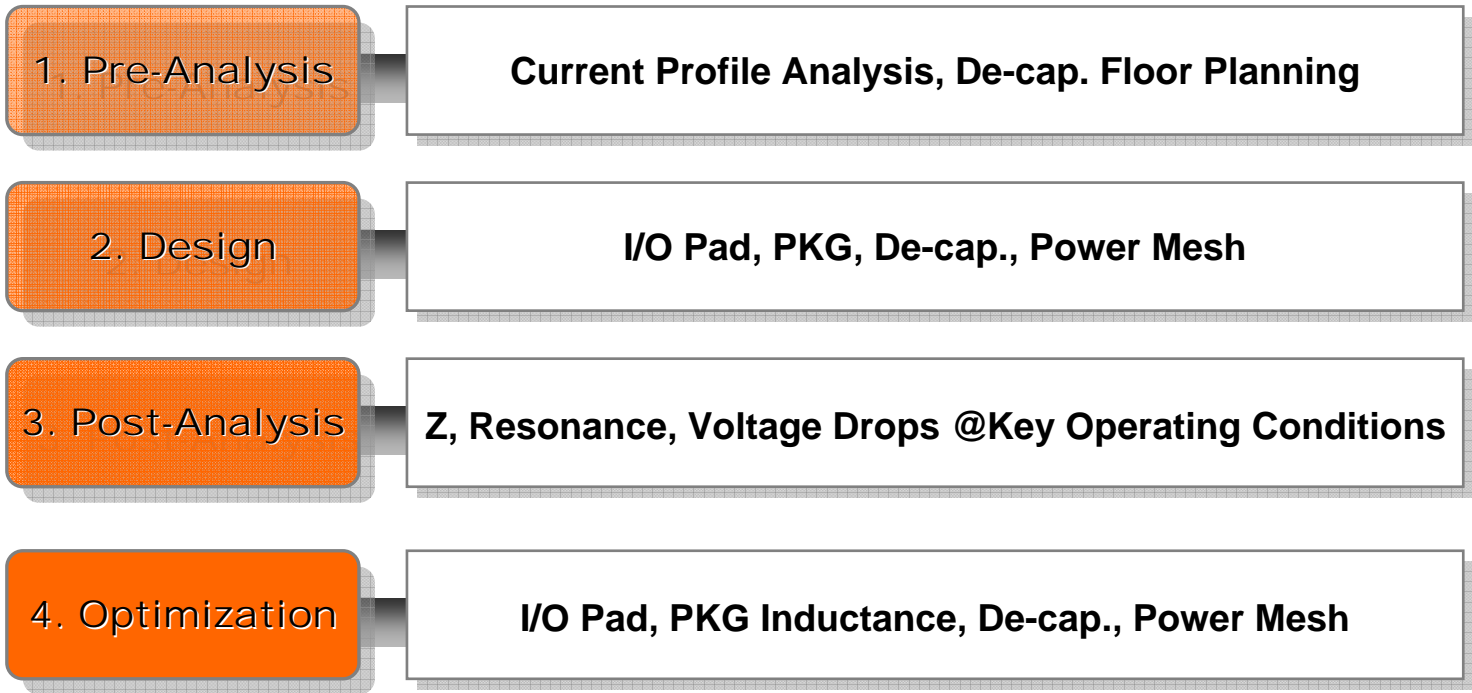


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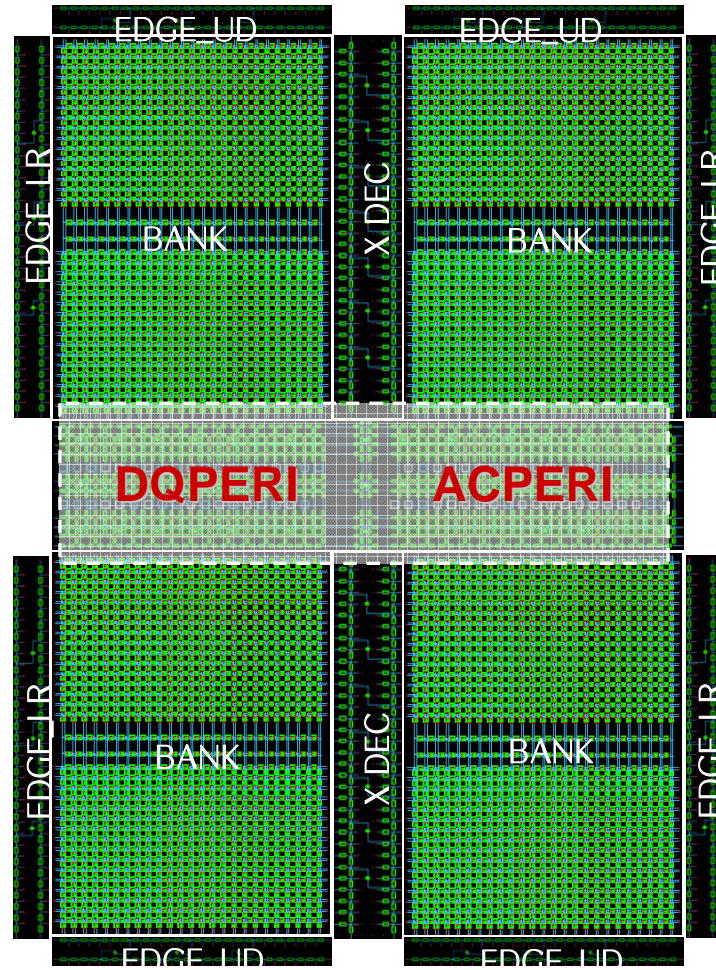


# Four Steps of On-chip PDN Design



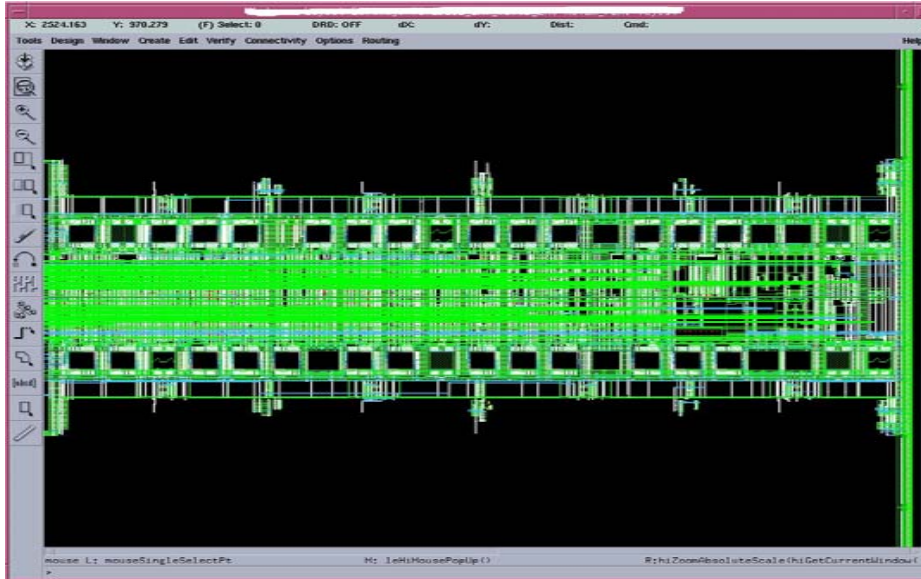


# DRAM Configuration



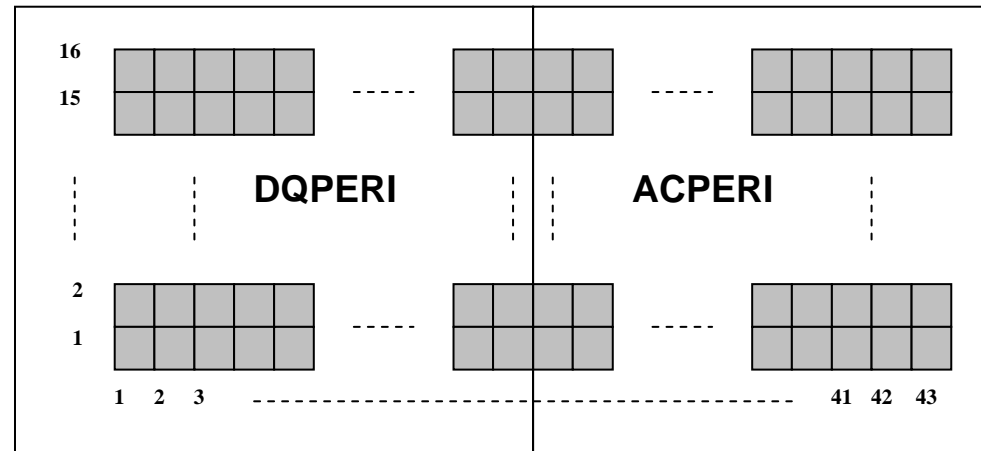


# Modeling Scheme for PERI



Power Mesh @ACPERI

Voltage Drop  
Display Cell Matrix



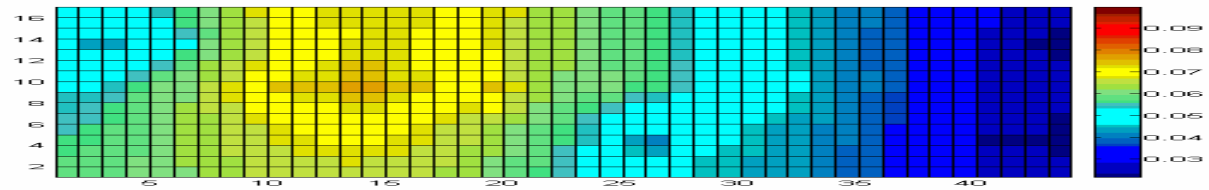


# Voltage Drop @PERI

## Target Voltage Drops @IDD4R

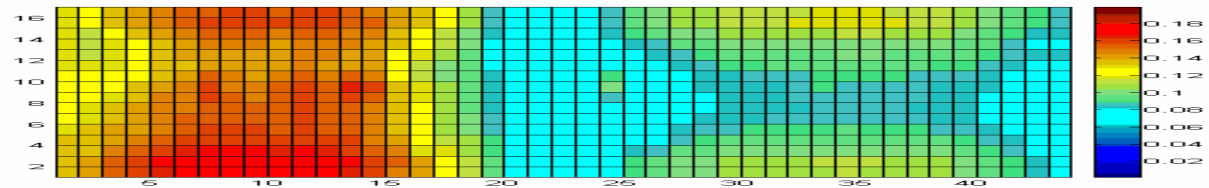
- Static: 60mV
- Dynamic: 150mV

**Max.: 76 mV**  
Min. : 21 mV  
Avg. (DQP): 64 mV  
Avg. (ACP): 40 mV



Static Voltage Drop

**Max.: 200 mV**  
Min. : 85 mV  
Avg. (DQP): 164 mV  
Avg. (ACP): 123 mV



Dynamic Voltage Drop



## How to Optimize On-chip PDN?

PKG Inductance: Ball Map-Pad Location Optimization, The Number of Pads, Optimized PKG Design

Chip-PKG Resonance: On-chip ESR, PKG L

Static Voltage Drop: Power Mesh, The Number of Pads,  
**Circuit-Pad Location Optimization**

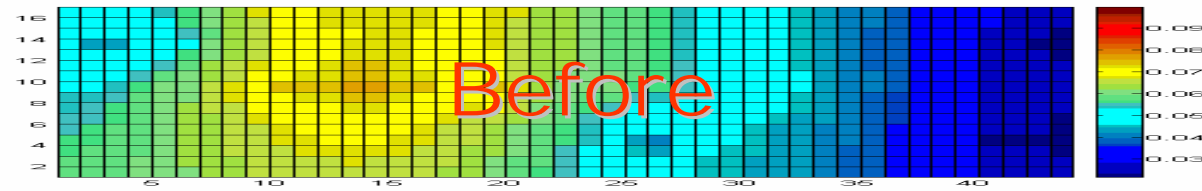
Dynamic Voltage Drop: Power Mesh R, On-chip ESR (De-cap. Size,  
**De-cap. W/L Ratio**)



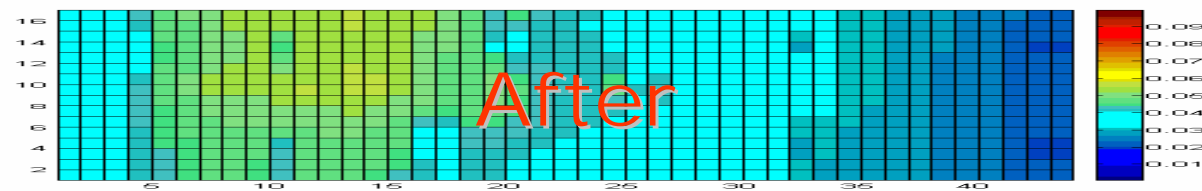
# Circuit-Pad Location Optimization – (1)

Inductance	Before	After
$L_{VDD}$	460 pH	440 pH
$L_{VSS}$	275 pH	266 pH
$L_m$	151 pH	162 pH

**Max.: 76 mV**  
Min. : 21 mV  
Avg. (DQP): 64 mV  
Avg. (ACP): 40 mV

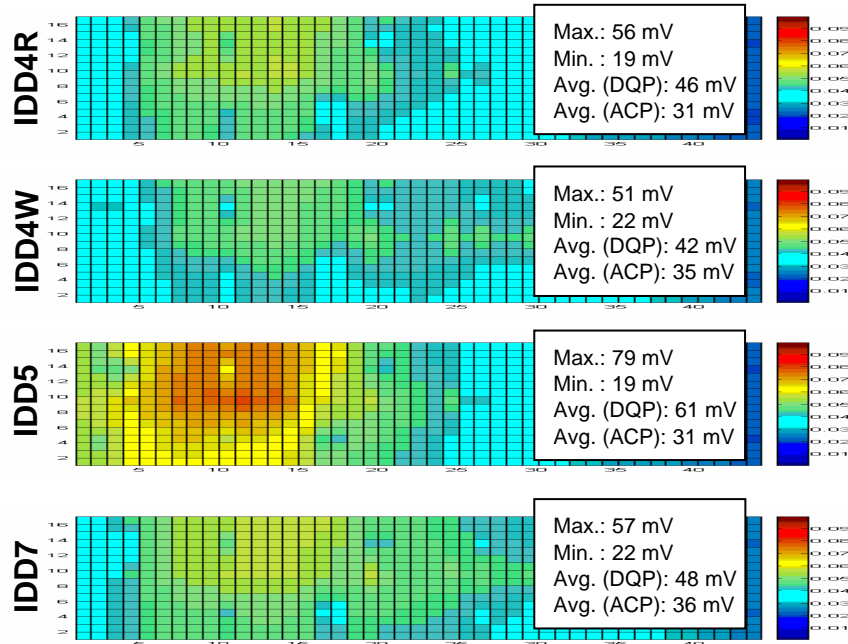


**Max.: 56 mV**  
Min. : 19 mV  
Avg. (DQP): 46 mV  
Avg. (ACP): 31 mV

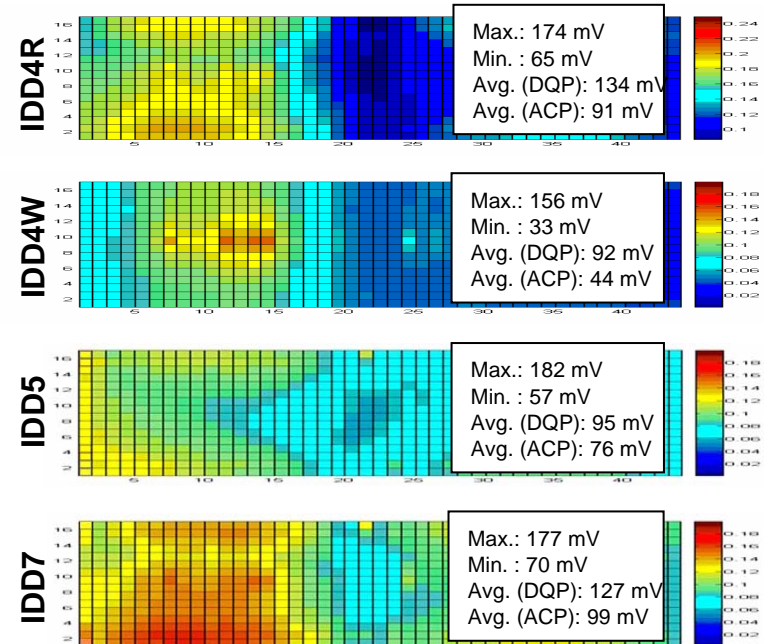




# Circuit-Pad Location Optimization – (2)



Static Voltage Drop

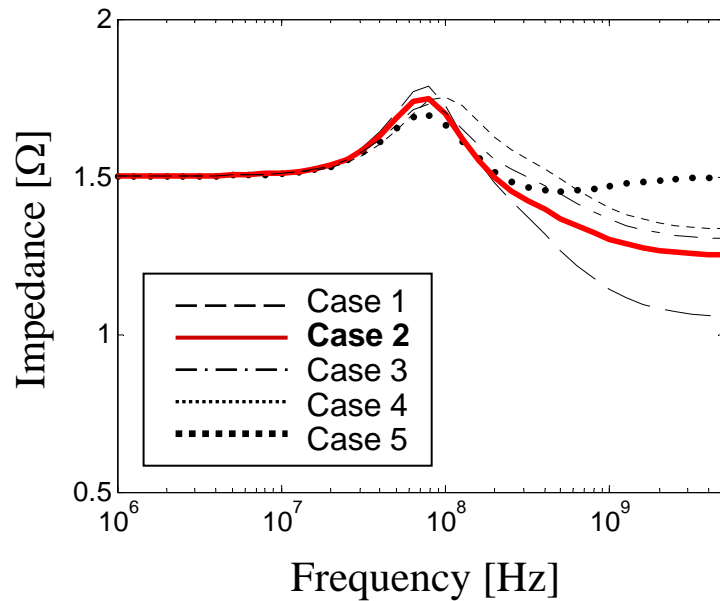


Dynamic Voltage Drop

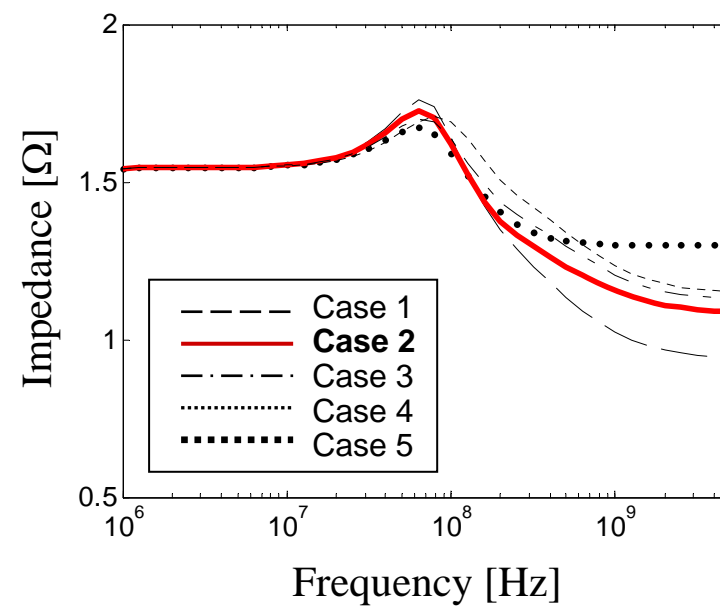


# De-cap. W/L Ratio Optimization – (1)

- Case 1: Fully Low ESR
- Case 2: Mixed ESR Opt.1**
- Case 3: Mixed ESR Opt.2
- Case 4: Mixed ESR Opt.3
- Case 5: Fully High ESR



**DQPERI**

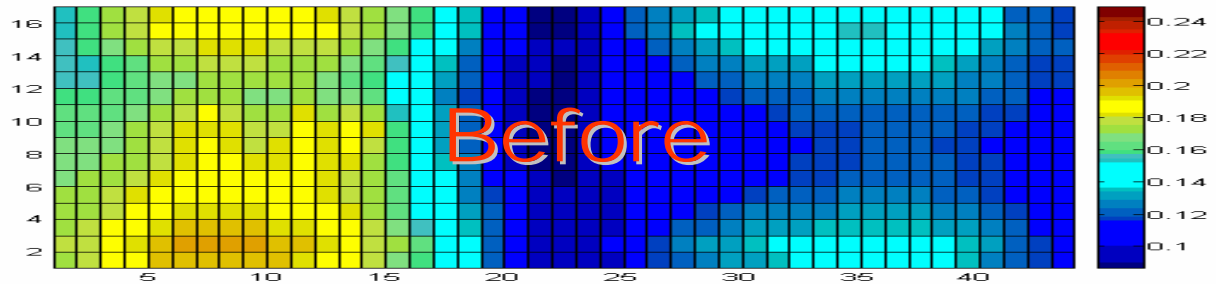


**Center PERI**

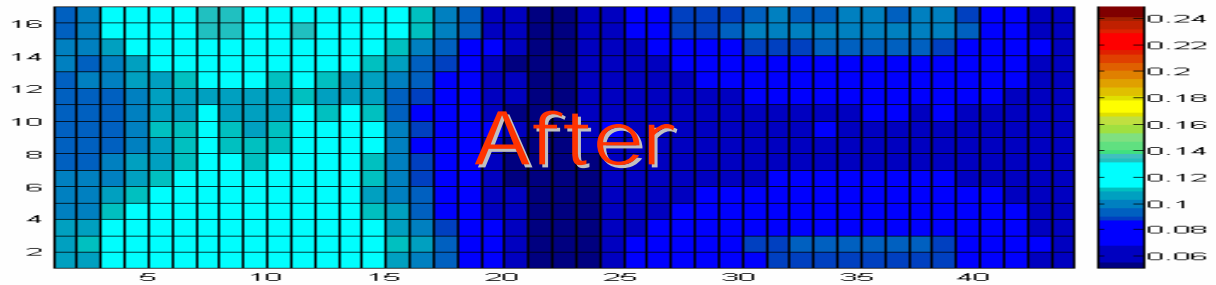


# De-cap. W/L Ratio Optimization – (2)

**Max.: 174 mV**  
Min. : 65 mV  
Avg. (DQP): 134 mV  
Avg. (ACP): 91 mV



**Max.: 133 mV**  
Min. : 49 mV  
Avg. (DQP): 104 mV  
Avg. (ACP): 40 mV





## Summary of Voltage Drops @IDD4R

<b>IDD4R (unit : mV)</b>	<b>Original</b>	<b>Pad Relocation</b>	<b>Pad Relocation + W/L Optimization</b>
<b>Static</b>	<b>76</b>	56	<b>56</b>
<b>Dynamic</b>	<b>200</b>	174	<b>133</b>



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# Things To Need To be Prepared

## Trend

- High-Speed
- High-Current/Low Power
- Small Size
- MCP / SiP / SoC
- Hybrid

## Target

- Power Specification
- Target Jitter/Timing
- Noise Sensitivity
- By Frequency

## Design Methodology

- Optimized De-cap.
- Low-L PKG
- Resonance
- Cost-Effective

## Modeling

- PKG/On-chip/PCB
- Accuracy/Efficiency
- MoR
- Broadband

## Analysis

- Simulation Tool
- Co-Simulation
- Multi-chip PI/SI/EMC

## Human Resource

- More SI/PI/EMC Engineer
- SI/PI/EMC All-rounded



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**Thank You!**