

Accurate HFSS Simulation of SMT Components in SiP and MCM Designs

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Skyworks Solutions

16 Oct 2007



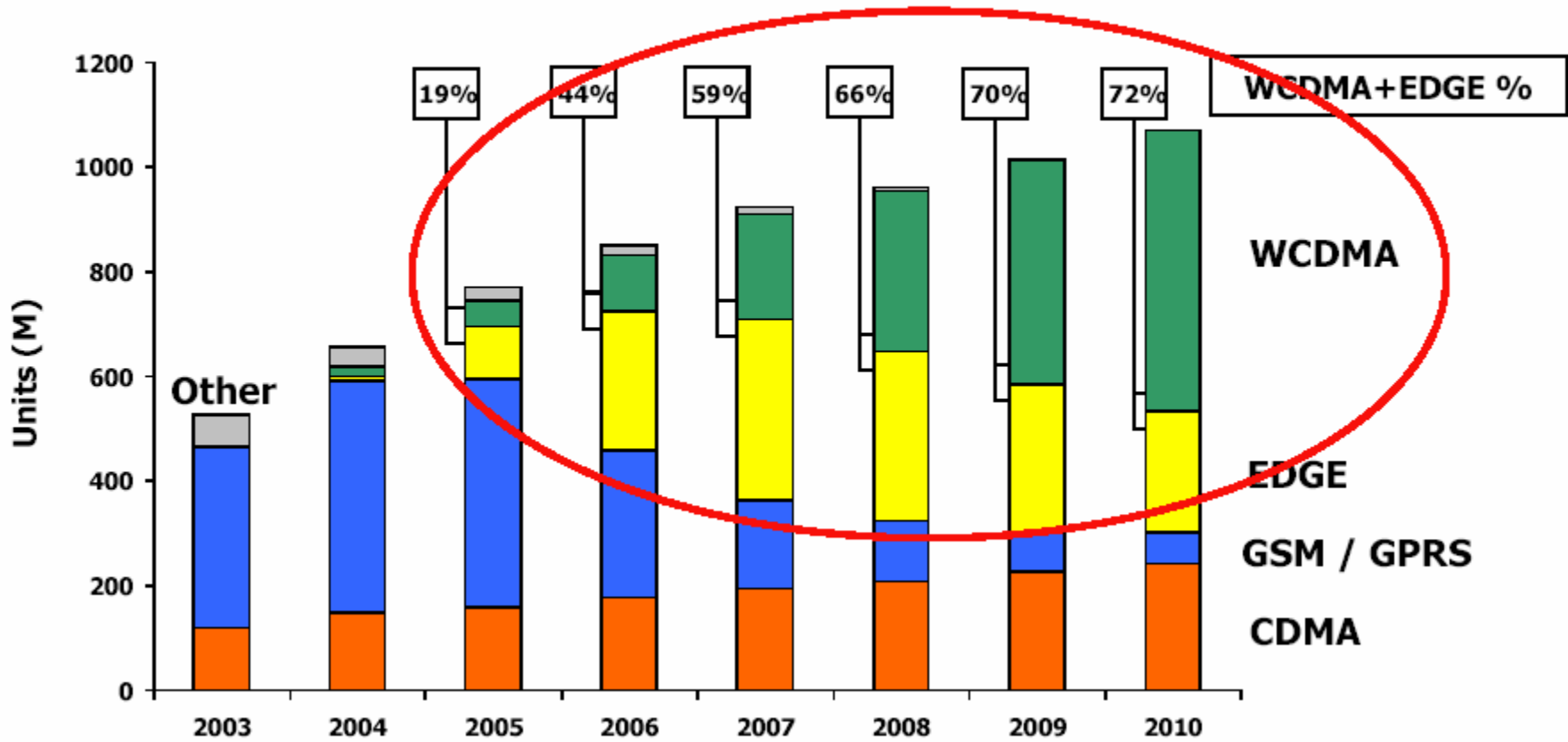
- **Wireless Market Evolution**
- **Why SMT Components?**
- **A Sample MCM Laminate Design**
- **HFSS Simulation Setups for a SMD**
- **Intrinsic Inductance of Lumped Port**
- **How to Split a Port with No GND Reference**
- **Recommendations**

Mobile Handset Evolution



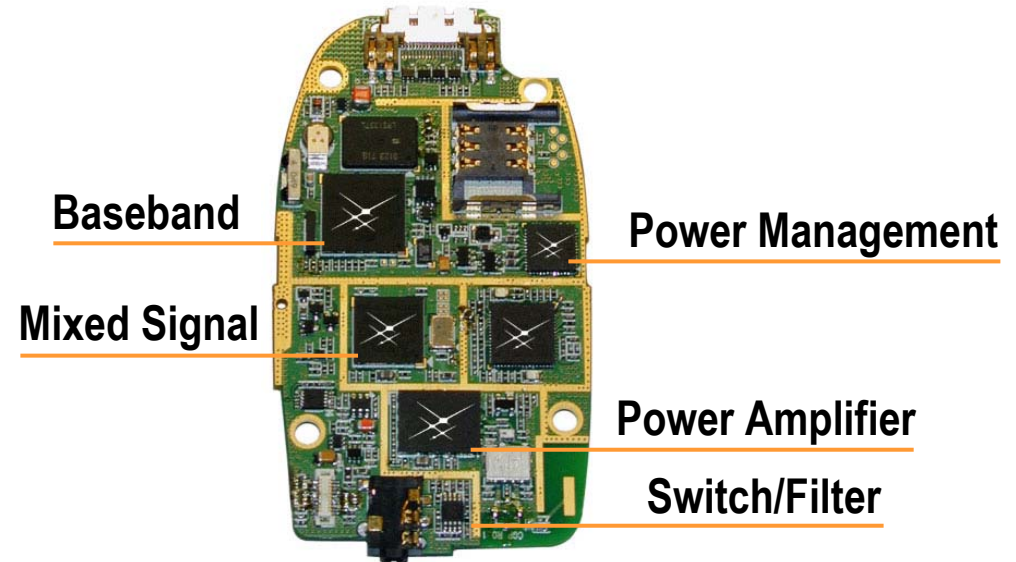
Mobile Handset Market Continues to Grow

Worldwide Handset Market

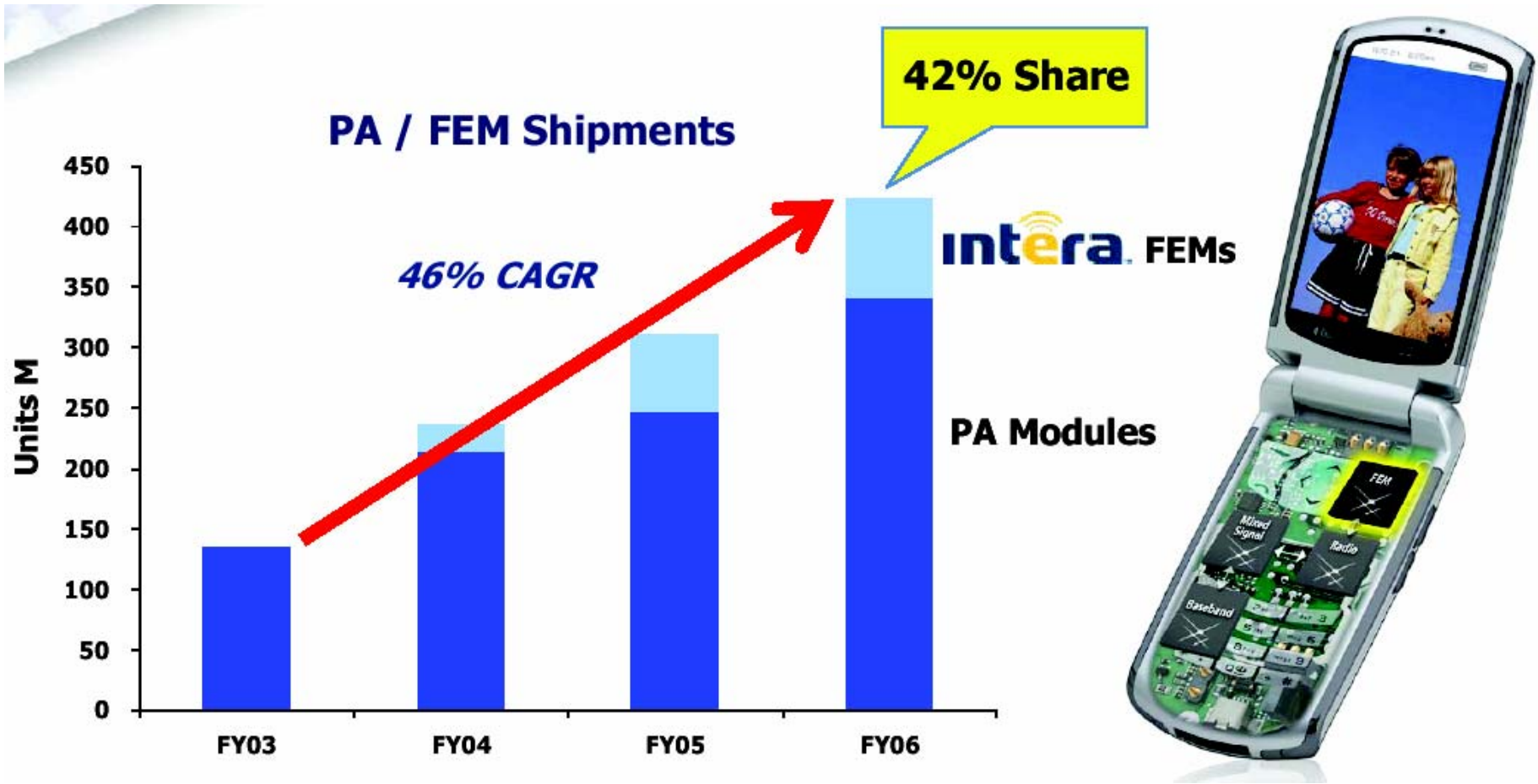


Market Forecast by Air Interface

Handset's Engine Is a MCM/PCB

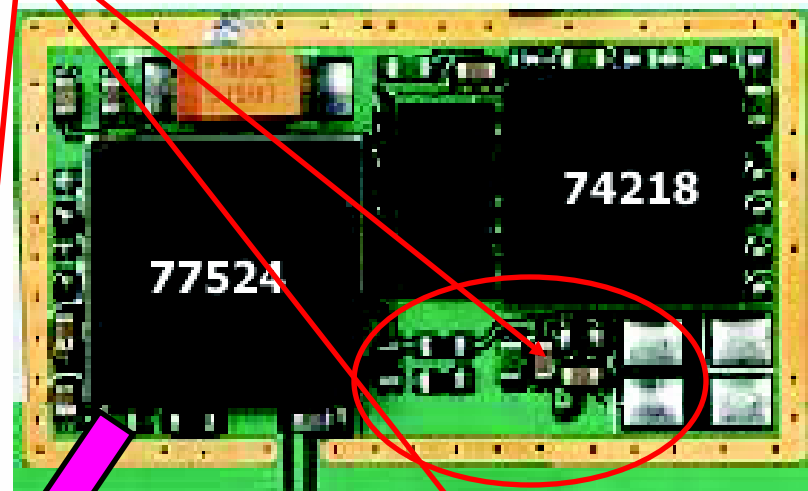
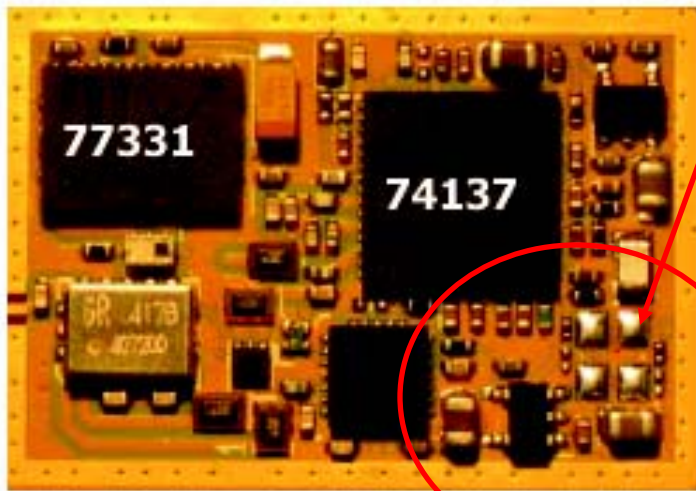


Skyworks Is A Leader in PA / Front-End Module

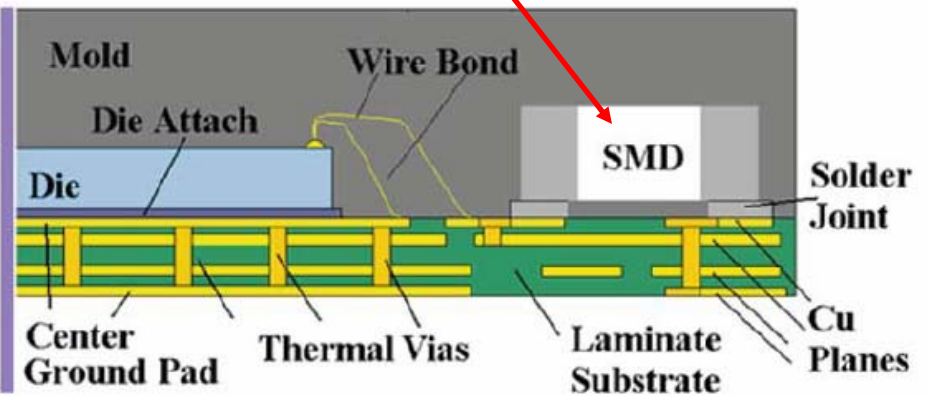
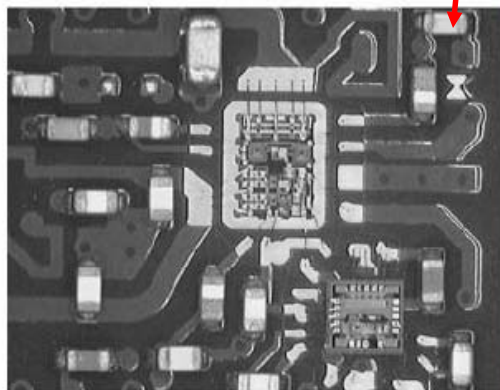


SMD Widely Used in MCM/FEMs

SMDs



MCM



What Challenges in Handset RF Design?



- **Integration of Multi-Medium Standards**

WLAN, GPRS, WCDMA, GPS, MP3, Video, Web...

- **System Miniaturization**

SOC, SiP, MCM, Stacked Die ...

- **Lower Cost**

Laminate PCB, SMT Components, Shrunk Die, Larger Wafer...

- **Improved Performance**

Efficiency, Power, Noise/Xtalk, EMI, Z Matching ...

- **System and Module Level A/D Mixed Simulation/Design**

EM Sim, Fast Spice, Mixed Signal Sim ...

How EM Simulation Helps RF Design?



- **Increased Demand for EM Co-simulation**

IR Drop, Xtalk, EMI, Embedded Matching ...

- **Passive Design Optimization**

Inductor, T-line, Wire-Bond Tuning, Vias ...

- **3D Module Design**

SMD, Stacked Die, Package, Wires, Module ...

- **Distributed Circuit at High Frequency**

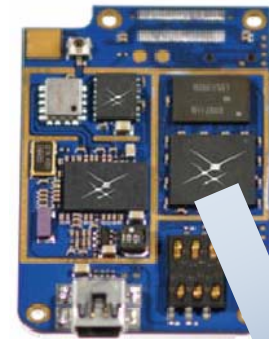
Beyond Limit of Lumped RLC, SPICE, Quasi-static Solution...

- **True Full-Wave Solution**

Loss, Coupling, Dispersion, Radiation, Cross-talk ...

Why Use SMT Components?

- Achieve Large L/C Value off-Chip
- Higher Q (lower loss)
- Easy Tuning/Design Optimization
- Reduced Development Cycle Time
- 'Lumped' and 'Discrete' for Simulation
- Competitive Vendors → Low cost

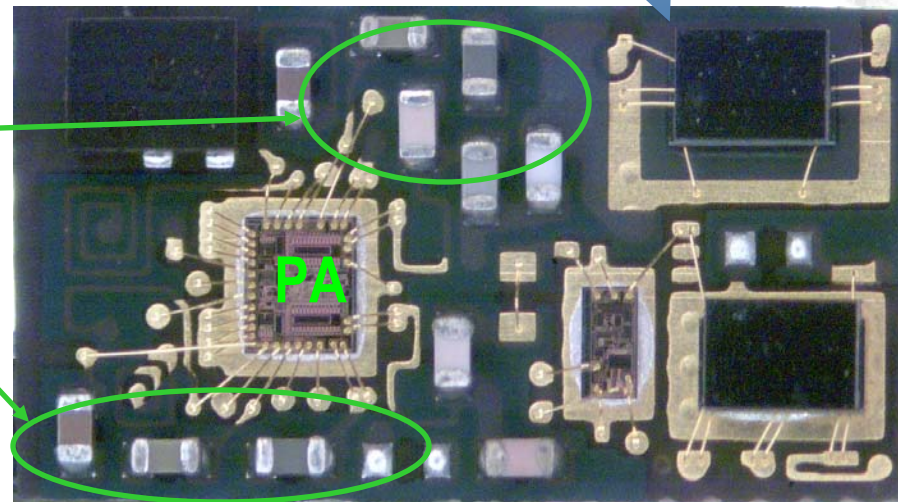


Lynx™ EDGE
Baseband
Processor

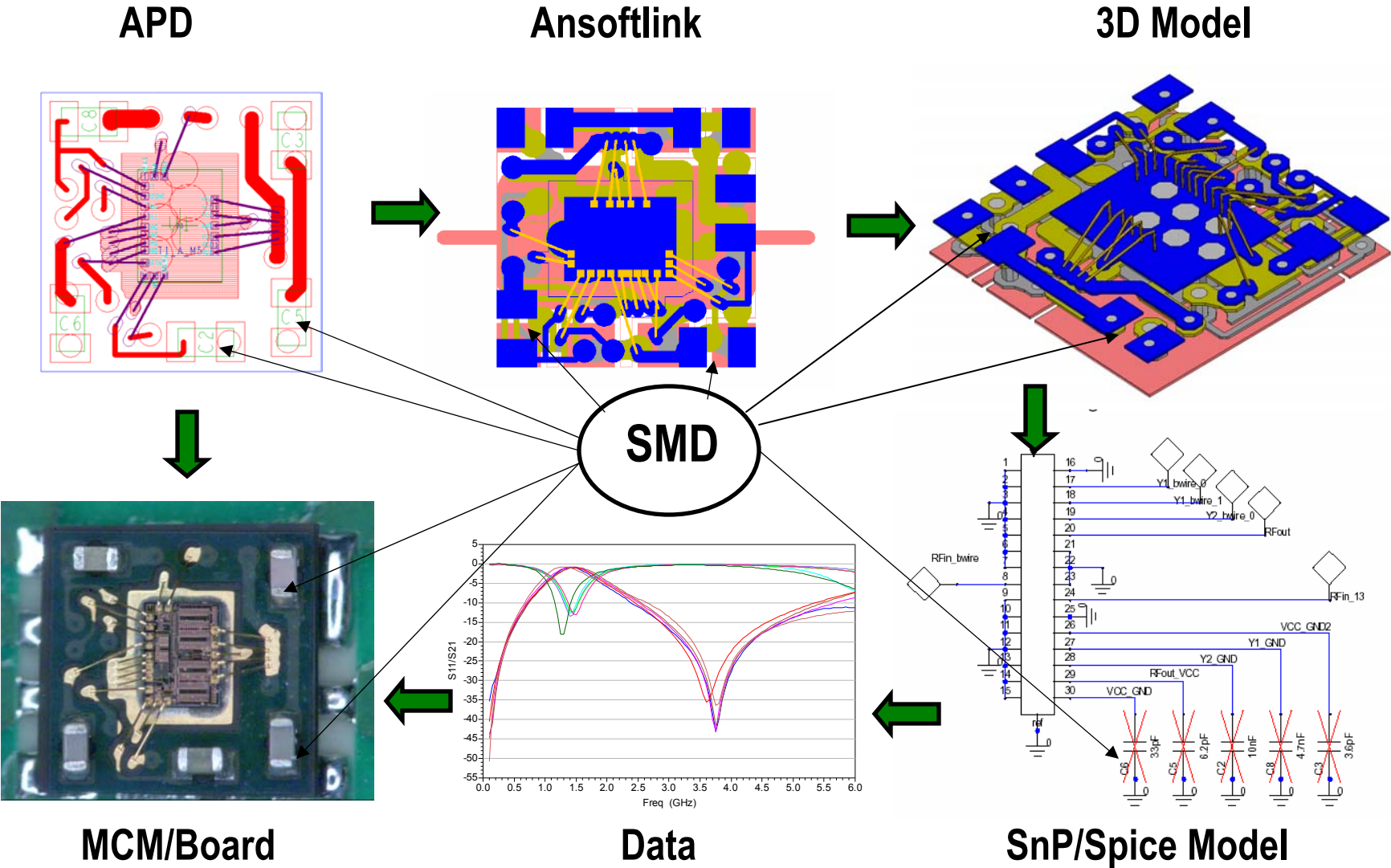


MCM

SMD



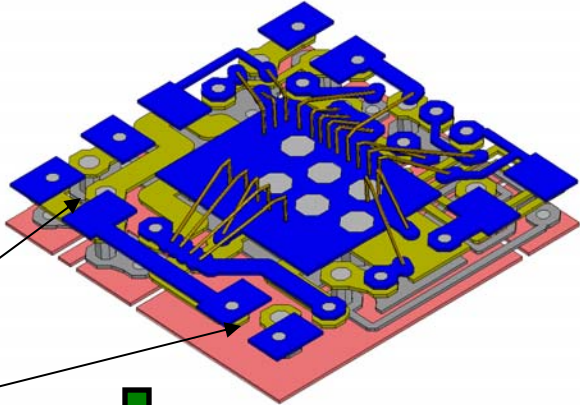
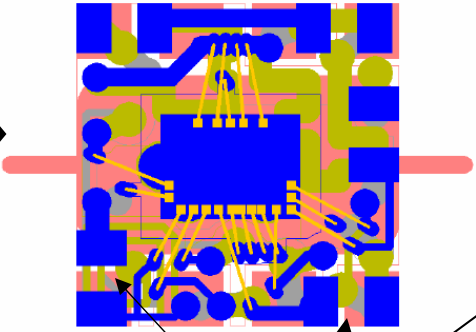
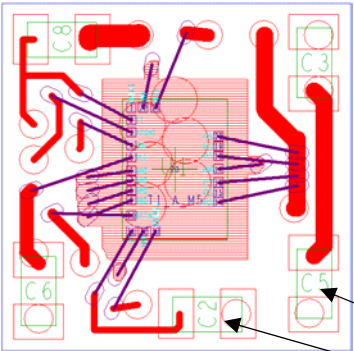
A Sample EM Simulation Flow



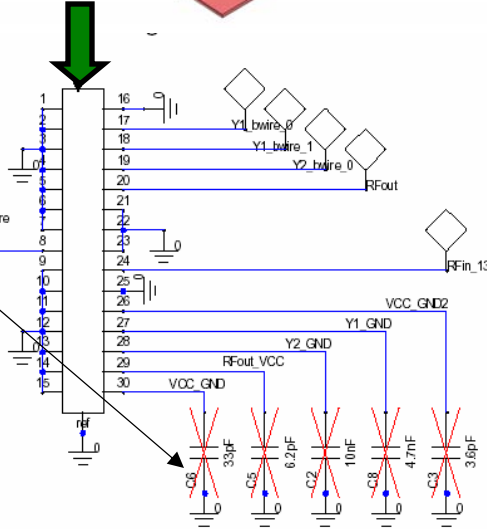
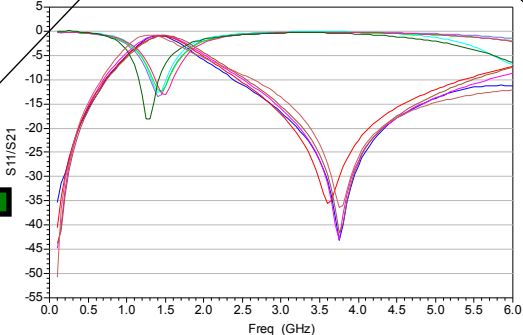
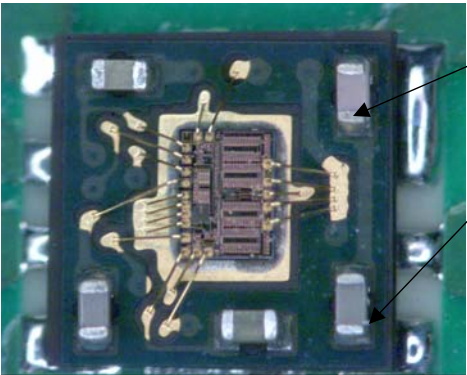
APD

Ansoftlink

3D Model



SMD



MCM/Board

Data

SnP/Spice Model

SMD Simulation Facilities in HFSS

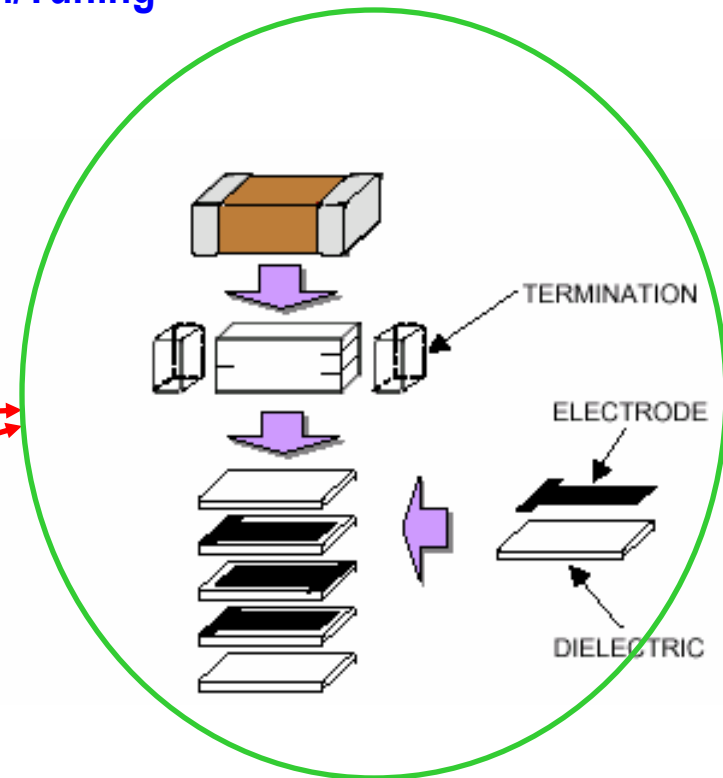
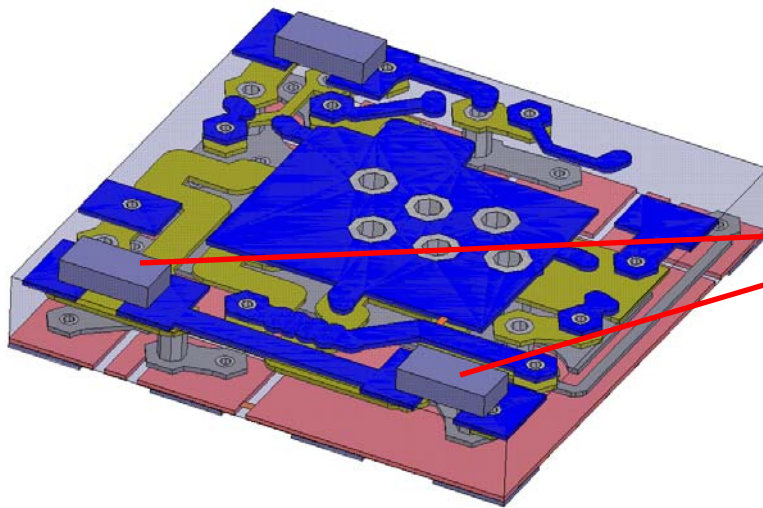


- **Add Physical SMD into Model**
 - Treat SMD as Part of the Layout Design
 - Direct FEM Meshing on Fine Structure of the SMD
- **Assign Surface/Boundary with Lumped SMD Parasitic**
 - Introduce an Artificial Impedance Surface near SMD
 - Make the Z-Surface Equivalent to SMD Parasitic from Vendor
- **Define a Lumped Port and Simulate in SPICE**
 - Define Lumped Port at SMD Pads
 - Create S-Parameter Model including SMD ports
 - Spice Simulation of the Design with the S-Parameter Model

SMD Modeling in HFSS

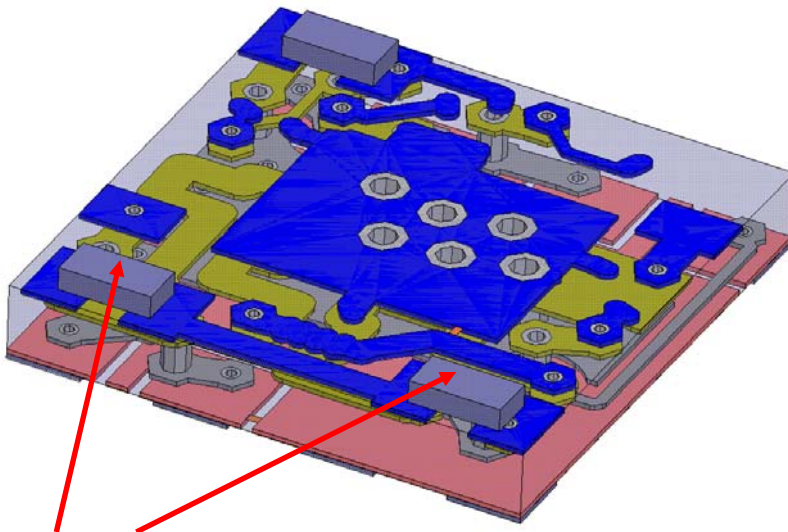
– Physical SMD Model

- Accurate and Physical
- But Most SMD Internal Material/Geometry Data Not Available
- Need Fine Mesh to Account for Micro-Structure Details
- CPU/Memory Expensive
- Not Practical in Design Optimization/Tuning



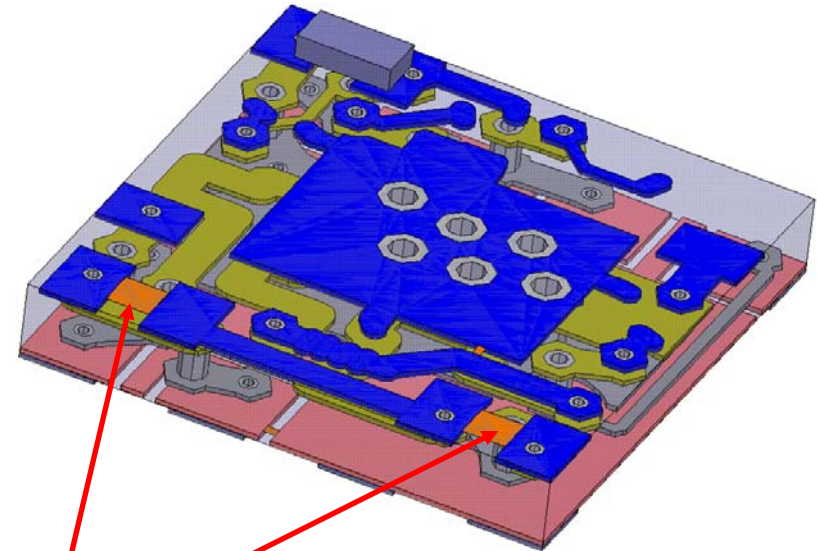
SMD Modeling in HFSS

- Lumped Port vs. Lumped RLC Surface



Lumped Surface (RLC)

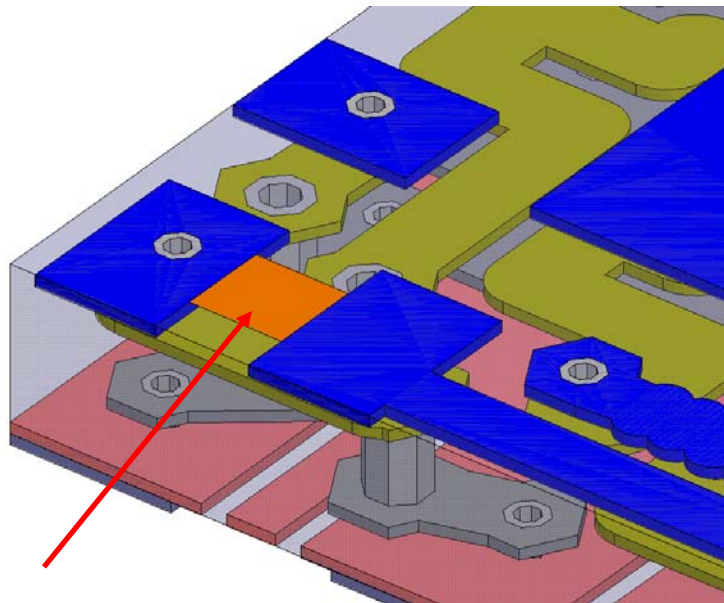
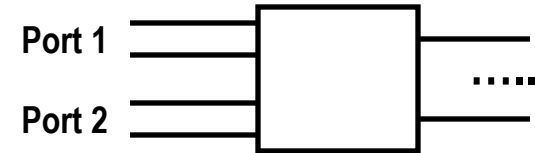
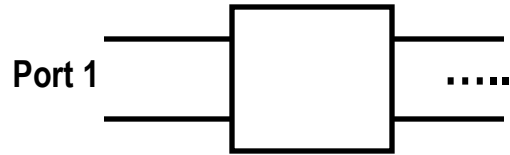
- SMD included in the model
- SMD bulk dielectric effect
- Fewer ports and smaller S-parameter file



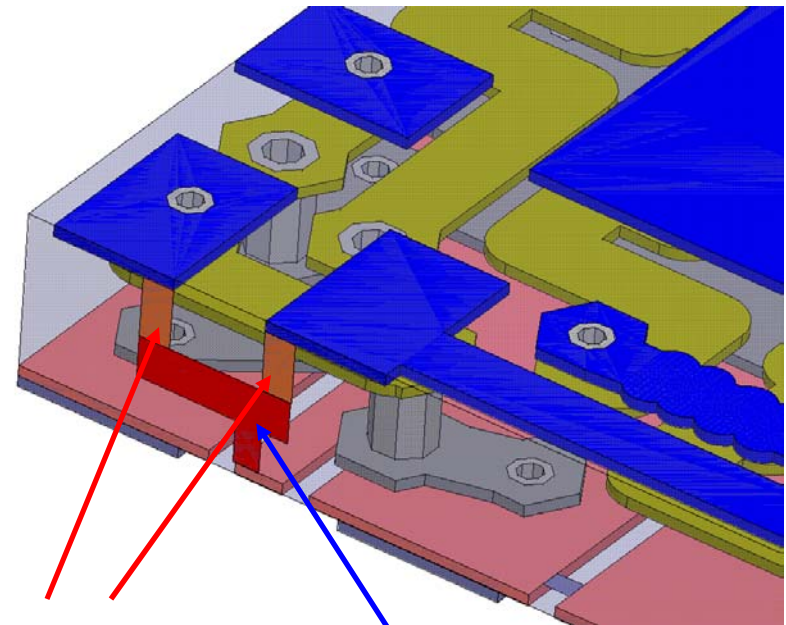
Lumped Port

- Larger S-parameter file/matrix
- Easy SMD tuning/design optimization
- May need to calibrate out SMD bulk dielectric

Setup for A Lumped SMD Port



Single Port

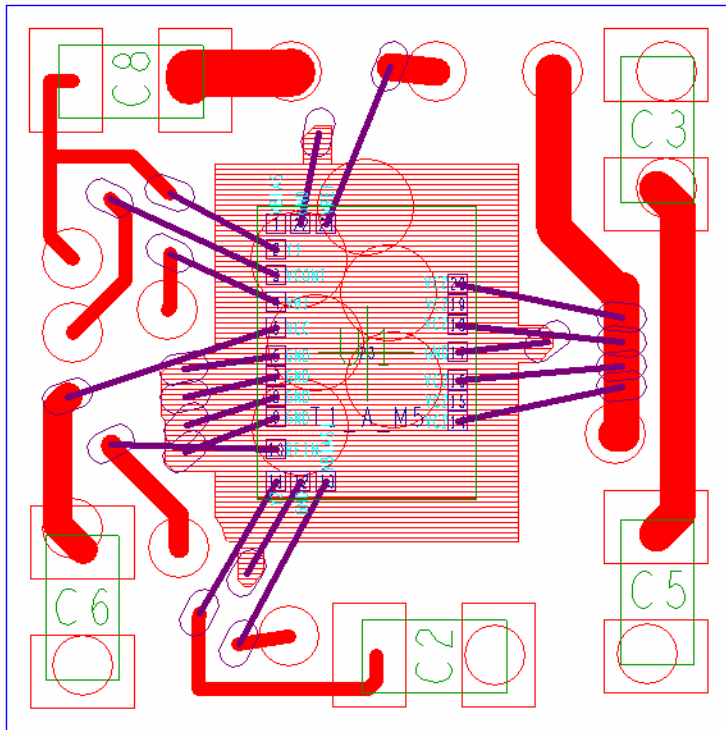


Dual Ports

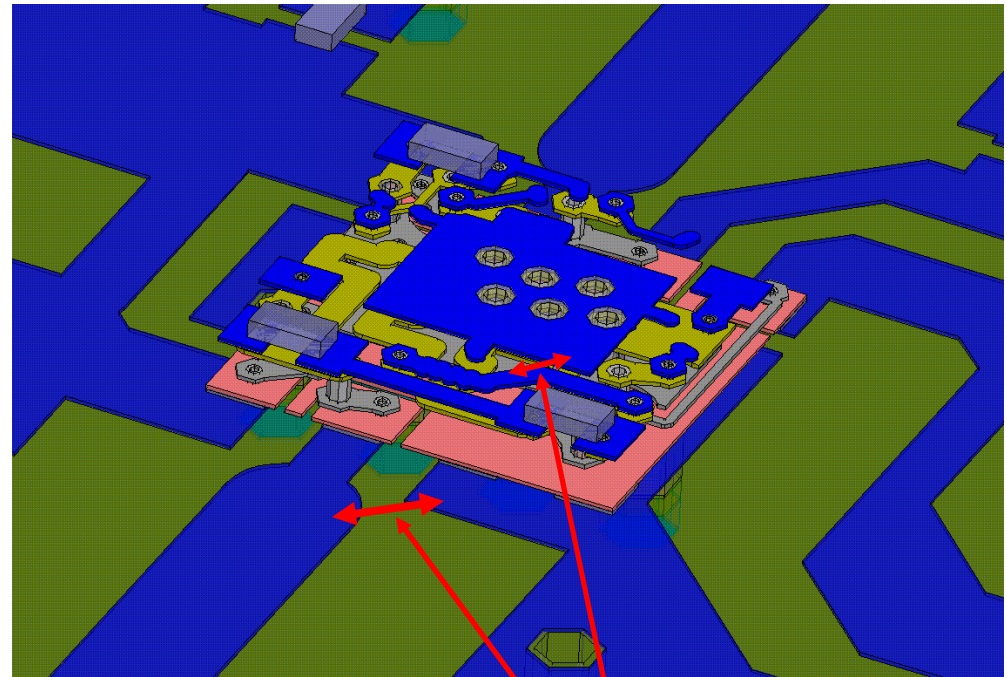
PEC to Ground Ports

A MCM Laminate Design

Laminate Design



3D Model



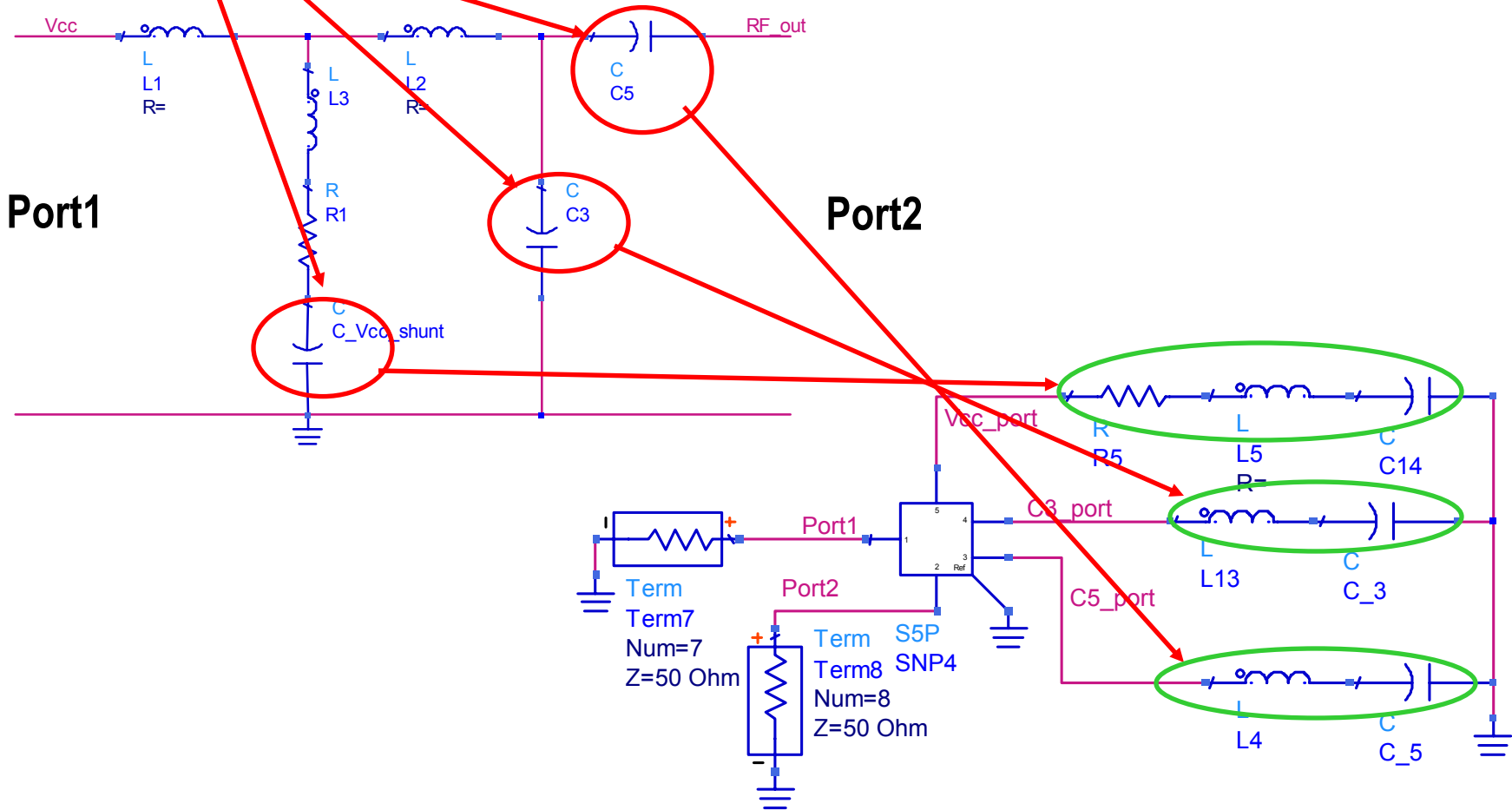
Probed

Selected Nets into a 3D Model

A MCM Laminate Design

-- Equivalent Net Circuit Modeled

SMT Components



SMD Modeling in HFSS

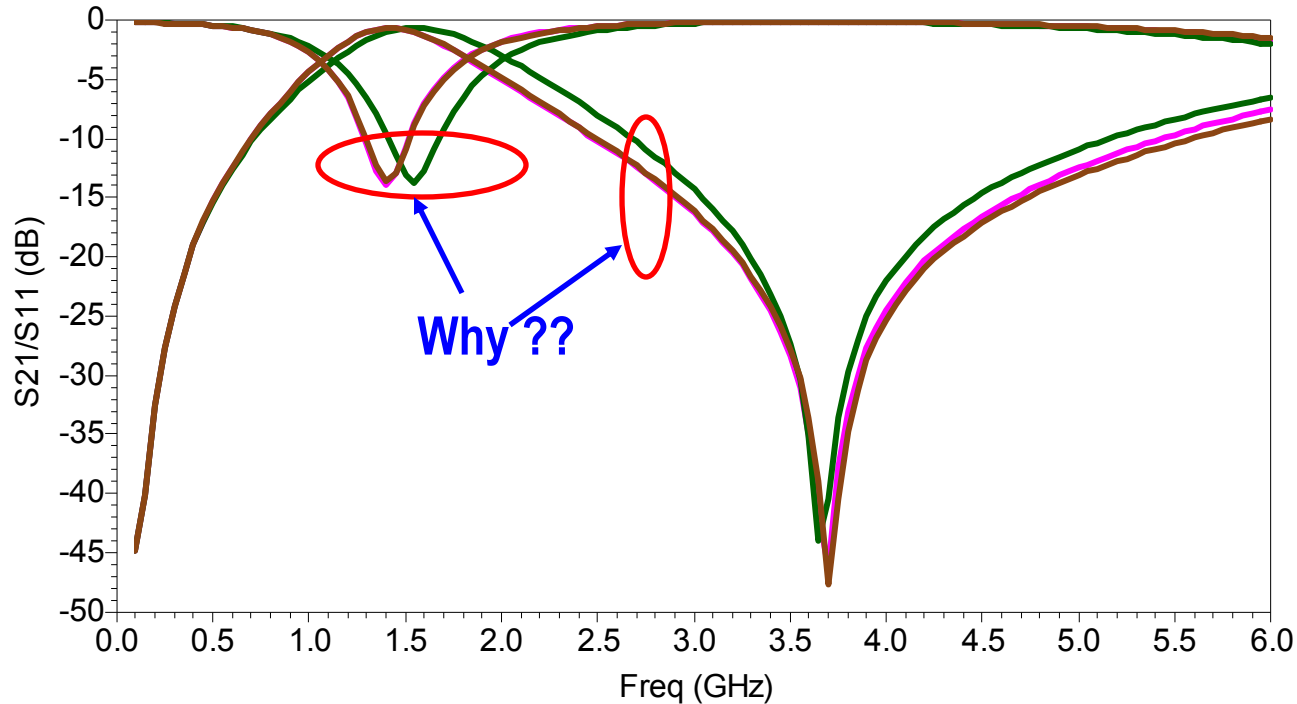
- Lumped Port vs. Lumped RLC Surface



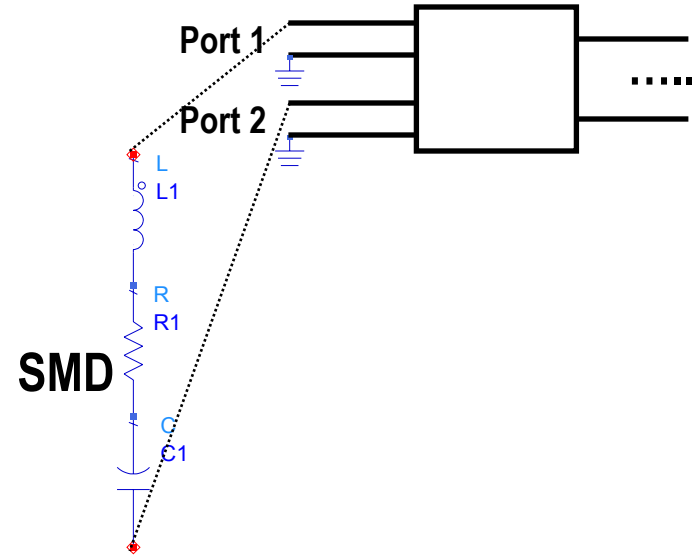
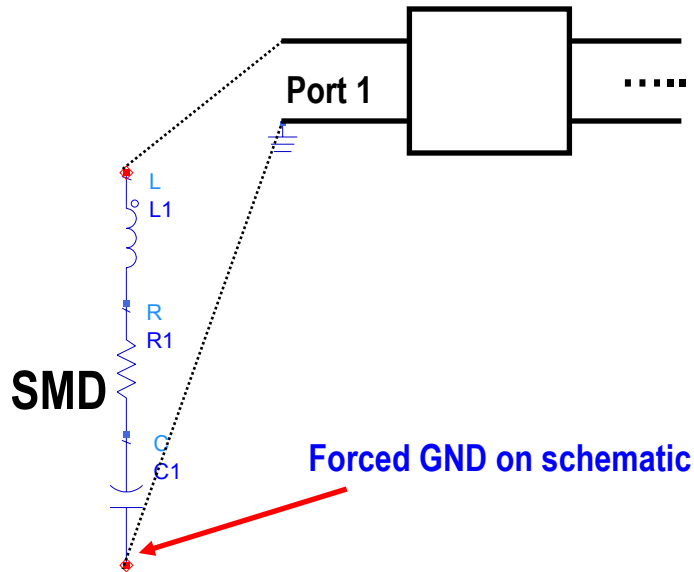
Pink: Single-Ended SMD Port Used

Brown: Dual SMD Ports Used

Green: SMD Modeled with Lumped RLC



Single SMD Port vs. Dual SMD Ports

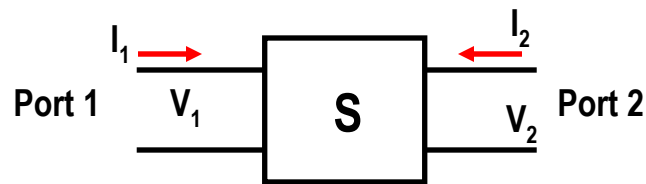


- Mathematically Equivalent
 - S Matrix – Mapping ΔV of SMD Ends
- Physically SMD End not GNDed
- Easy to Define Port for SMDs


- Schematic and Physical Connection Matched
- Bias and Decoup SMDs Can be Modeled
- But Difficult to Define Ports Ref to GND

Post Port Split from S/Y Matrix

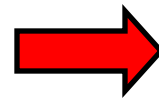
1+1 Port



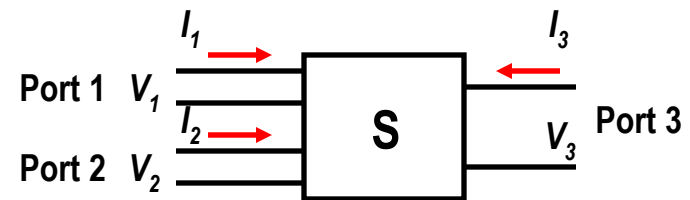
S to Y



$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$$



2+1 Port



Force: $I_1 = -I_2 = I_3$
 $V_1 = -V_2 = 0.5 V_3$



$$\begin{bmatrix} 2Y_{11} & 0 & Y_{12} \\ 0 & 2Y_{11} & -Y_{12} \\ Y_{21} & -Y_{21} & Y_{22} \end{bmatrix}$$



Y to S

Post Port Split from S/Y Matrix

-- General N Port Matrix



NxN Matrix with the i^{th} Port Split into Dual Ports (i^{th} and $(i+1)^{\text{th}}$)

$$\begin{bmatrix} Y_{1,1} & Y_{1,2} & \dots & Y_{1,N} \\ Y_{2,1} & Y_{2,2} & \dots & Y_{2,N} \\ \dots & \dots & \dots & \dots \\ Y_{N,1} & Y_{N,2} & \dots & Y_{N,N} \end{bmatrix}_{N \times N} \xrightarrow{\text{Red Arrow}} \begin{bmatrix} Y_{1,1} & \dots & Y_{1,i-1} & Y_{1,i} & -Y_{1,i} & Y_{1,i+1} & \dots & Y_{1,N} \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ Y_{i-1,1} & \dots & Y_{i-1,i-1} & Y_{i-1,i} & -Y_{i-1,i} & Y_{i-1,i+1} & \dots & Y_{i-1,N} \\ Y_{i,1} & \dots & Y_{i,i-1} & 2Y_{i,i} & 0 & Y_{i,i+1} & \dots & Y_{i,N} \\ -Y_{i,1} & \dots & -Y_{i,i-1} & 0 & 2Y_{i,i} & -Y_{i,i+1} & \dots & -Y_{i,N} \\ Y_{i+1,1} & \dots & Y_{i+1,i-1} & Y_{i+1,i} & -Y_{i+1,i} & Y_{i+1,i+1} & \dots & Y_{i+1,N} \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ Y_{N,1} & \dots & Y_{N,i-1} & Y_{N,i} & -Y_{N,i} & Y_{N,i+1} & \dots & Y_{N,N} \end{bmatrix}_{(N+1) \times (N+1)}$$

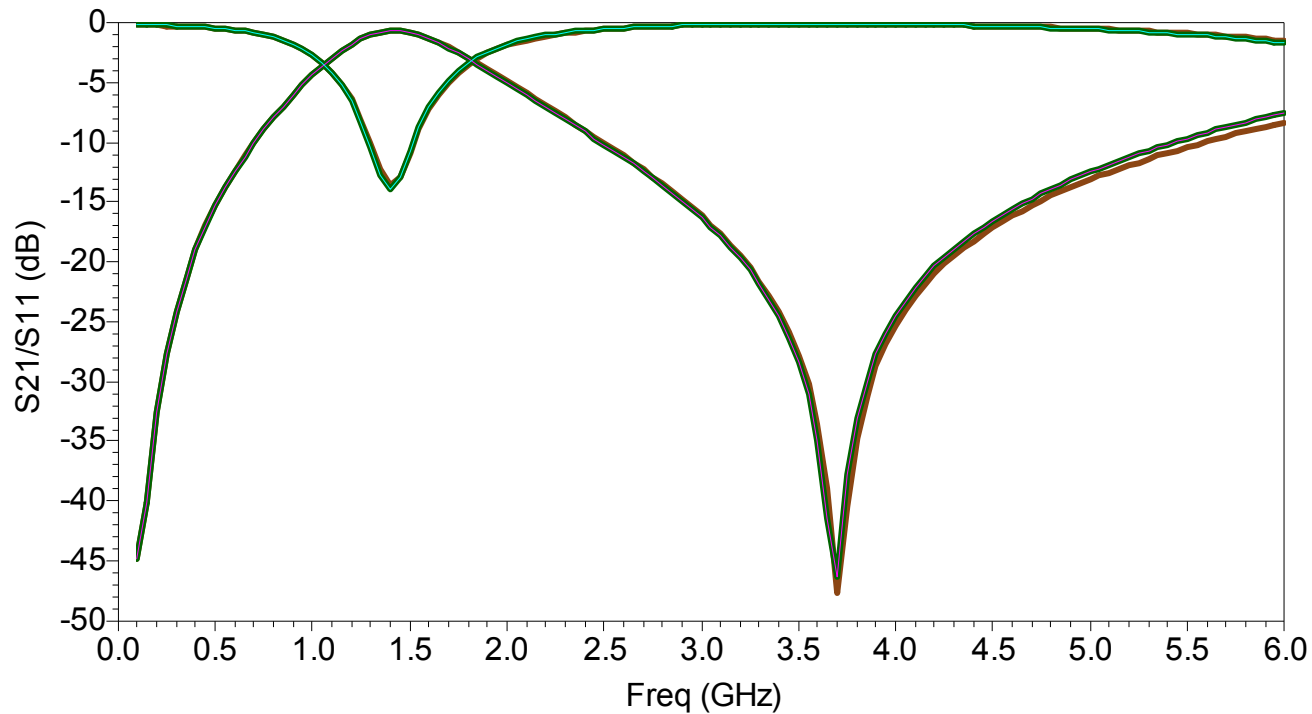
i
 $i+1$

Post Port Split

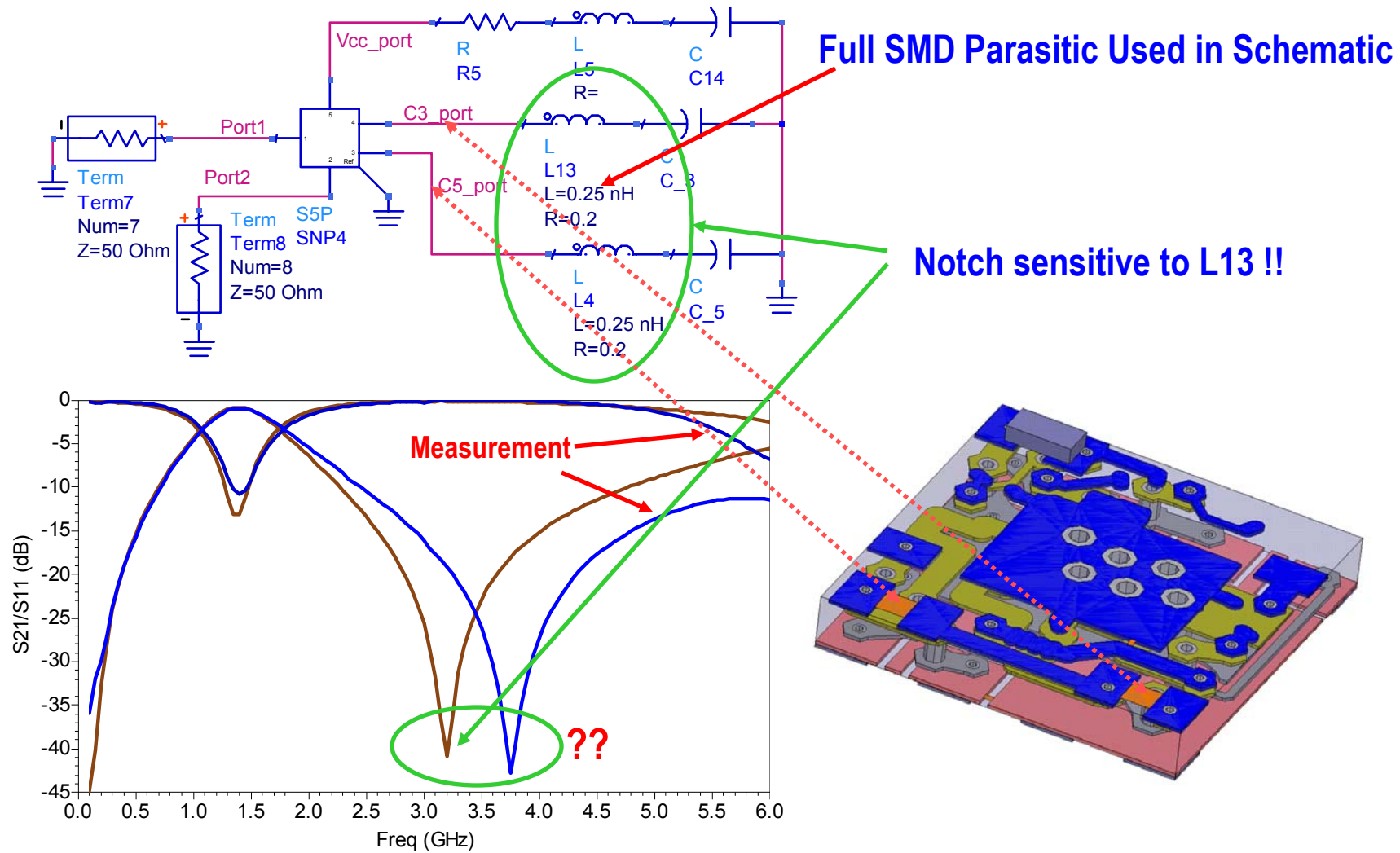
Pink: Single-Ended SMD Port Used

Brown: Dual SMD Ports Used

Green: Single SMD Port with Post Split into Two

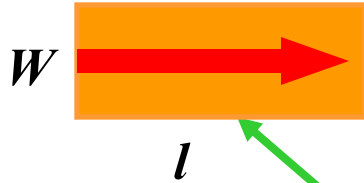


Simulation vs. Measurement

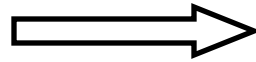


Any Intrinsic Inductance in a Lumped Port ?

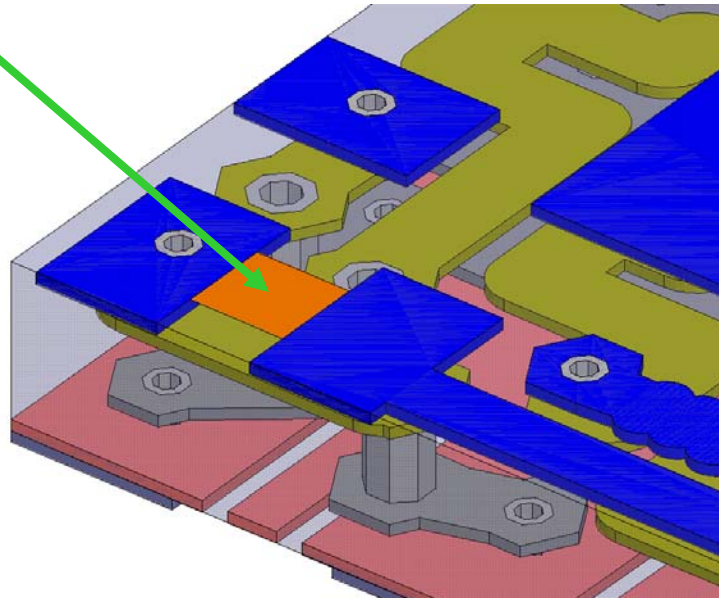
Current Sheet



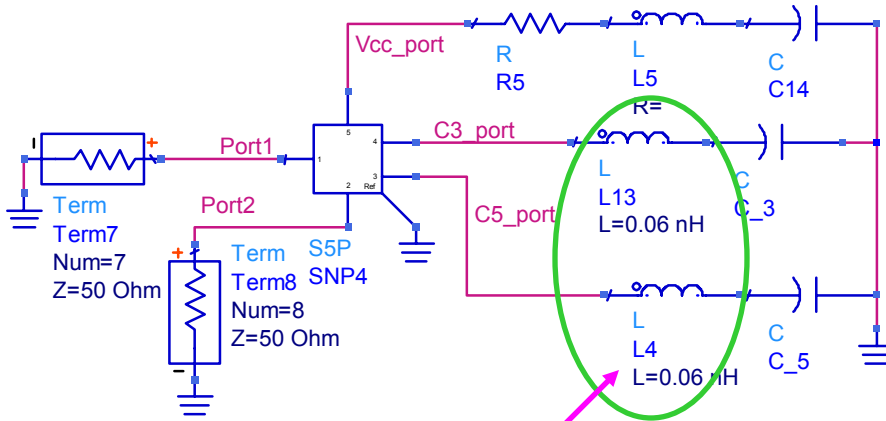
$$L \propto \int J \cdot A dV$$



$$L = \frac{\mu_0 l}{2\pi} \left[\ln\left(\frac{2l}{W}\right) + 0.50049 + \frac{W}{3l} \right]$$

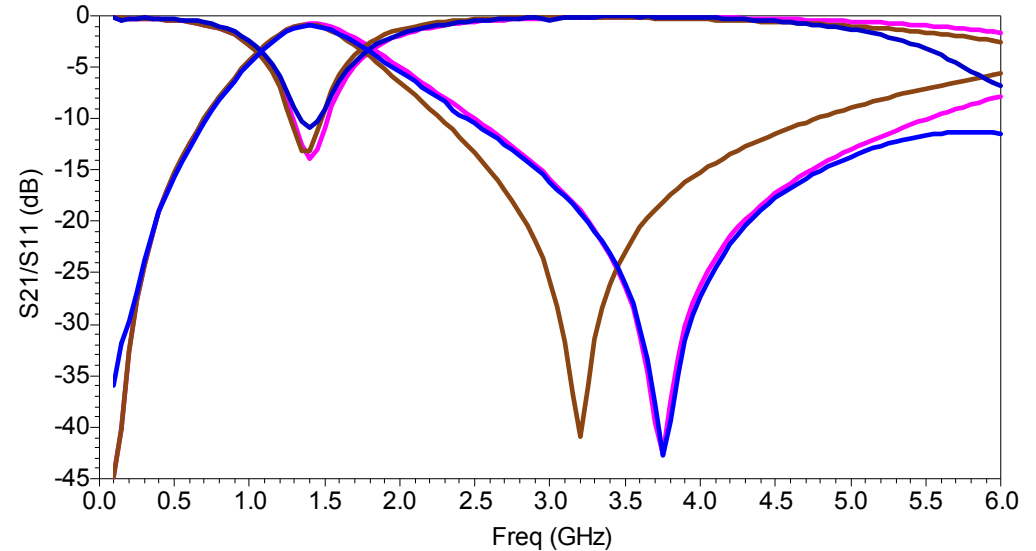


Intrinsic Inductance in a Lumped Port

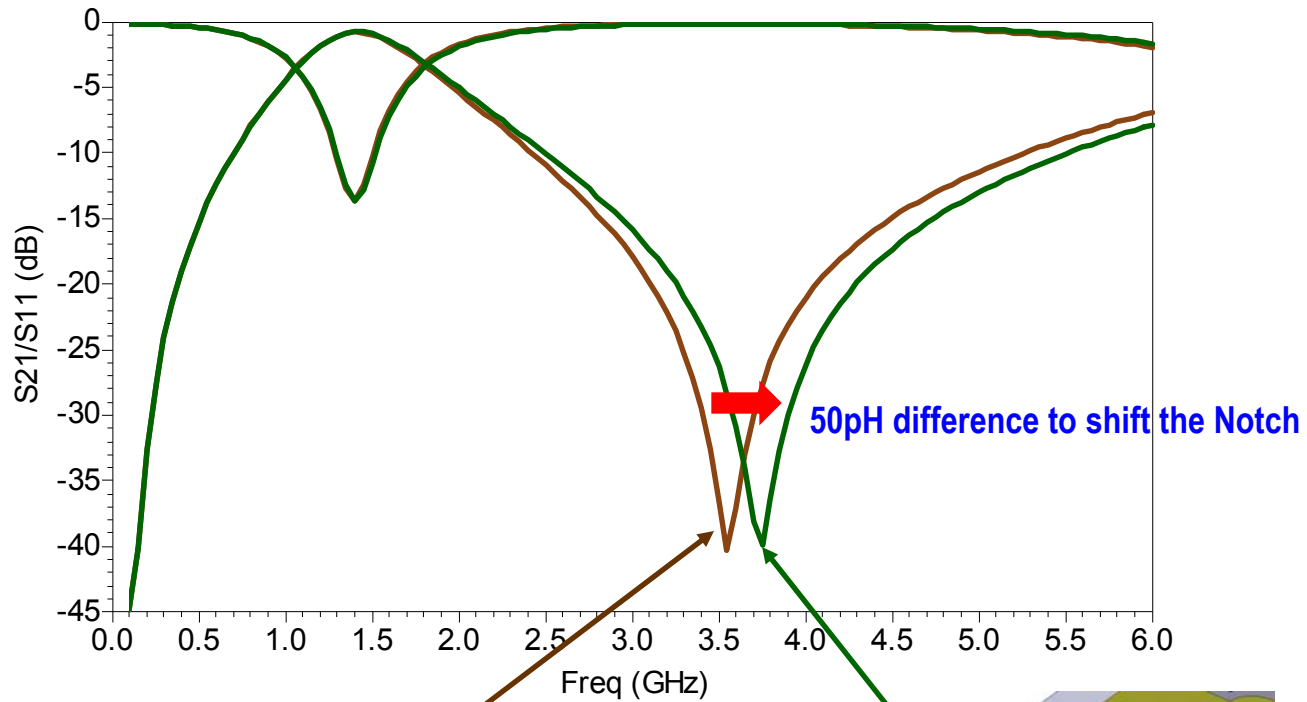


Brown: SMD Parasitic from Data Sheet
Blue: Measurement
Pink: SMD Port Intrinsic L Deducted

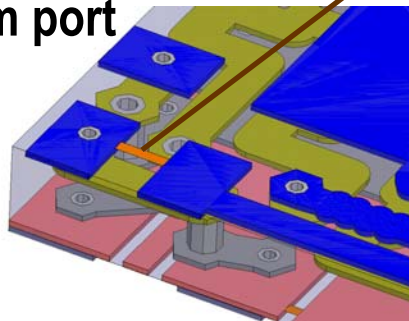
Port Intrinsic Inductance Corrected



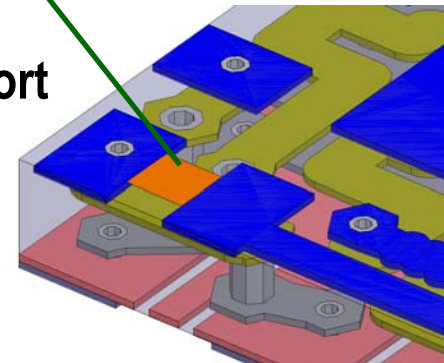
Intrinsic Inductance vs. Port Shape



Slim port

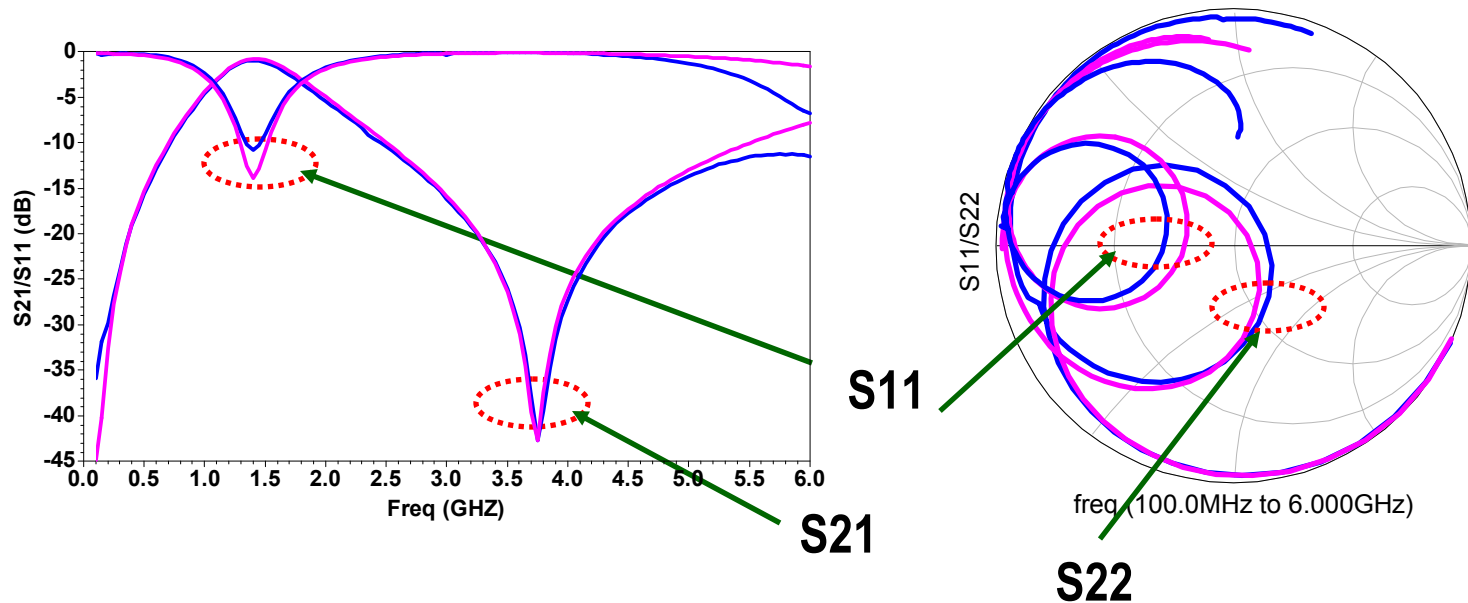


Wide port



A Second Check with Measurement

- S21 Matches Well
- S11/S22 Show Different Circle Diameter on Smith Chart



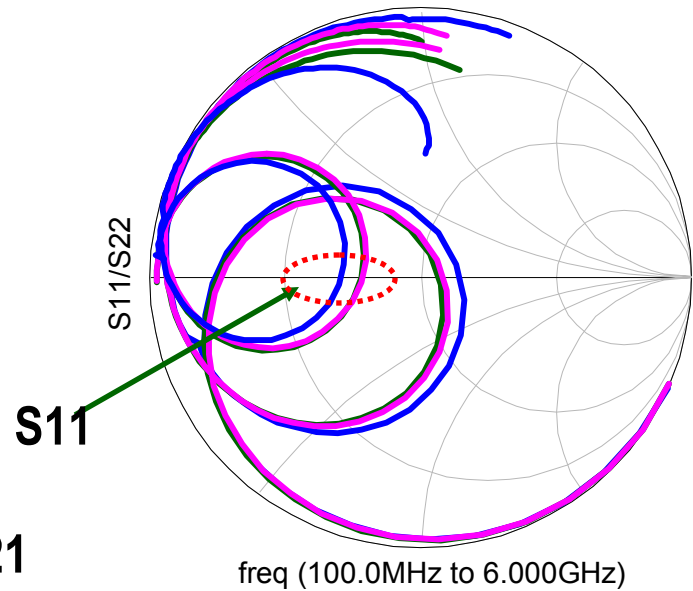
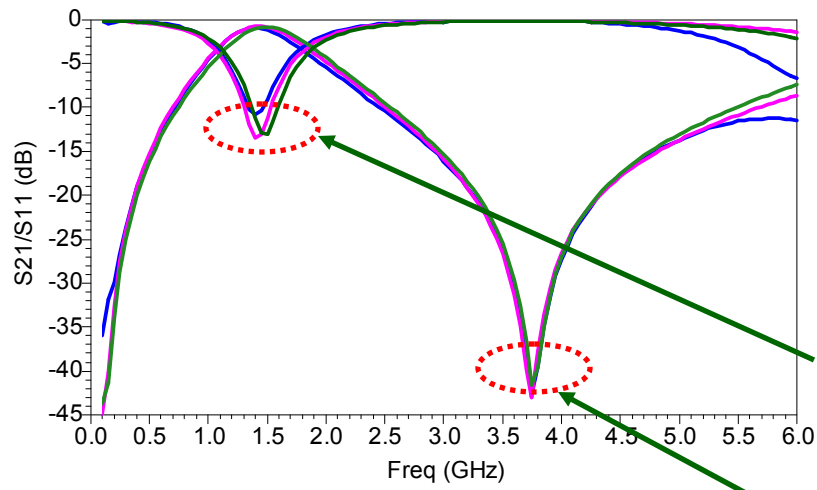
Pink: HFSS

Blue: Measurement

Simulation or Measurement?

-- A Second Try With an FDTD Simulator

- HFSS and FDTD Match Well (S21, S11, S22)
- Still S11/S22 Not Match to Measurement

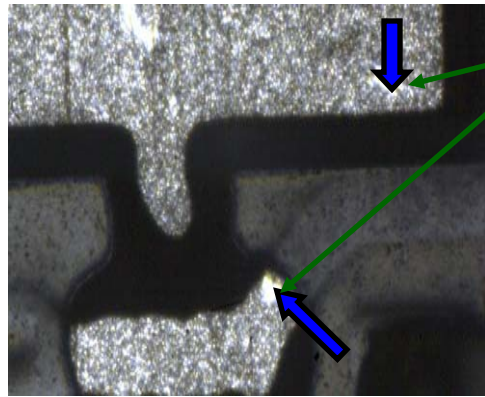


Pink: HFSS

Blue: Measurement

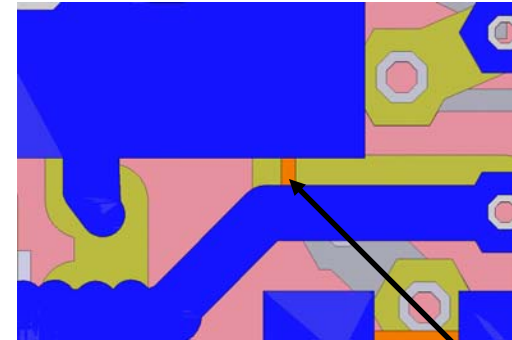
Green: FDTD

Is Reference 50 Ohm at Probed Port?

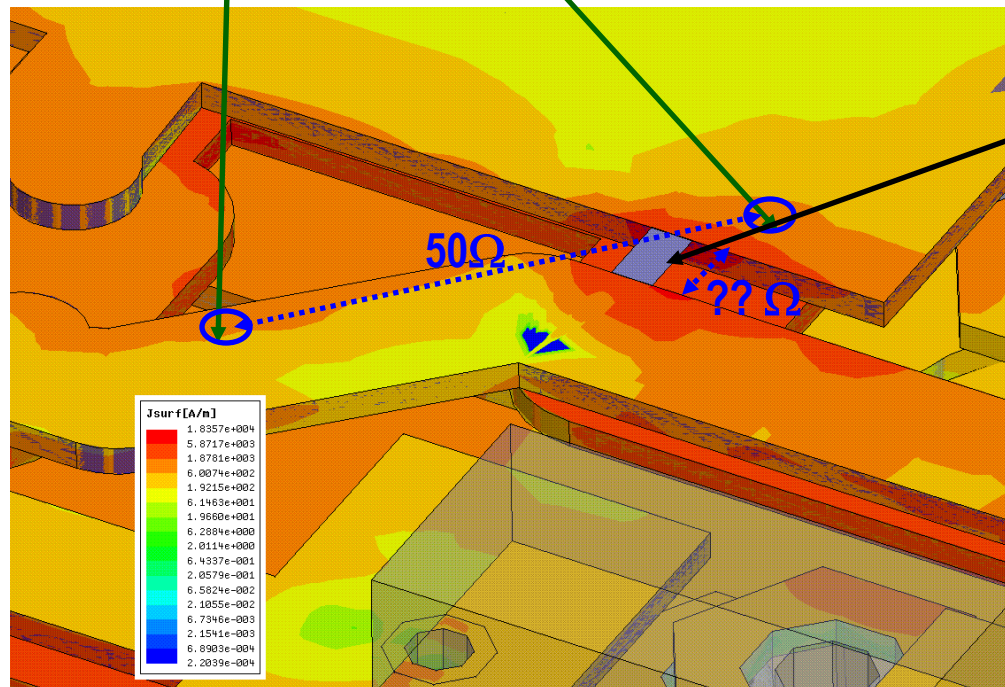


Probed Spot

Model

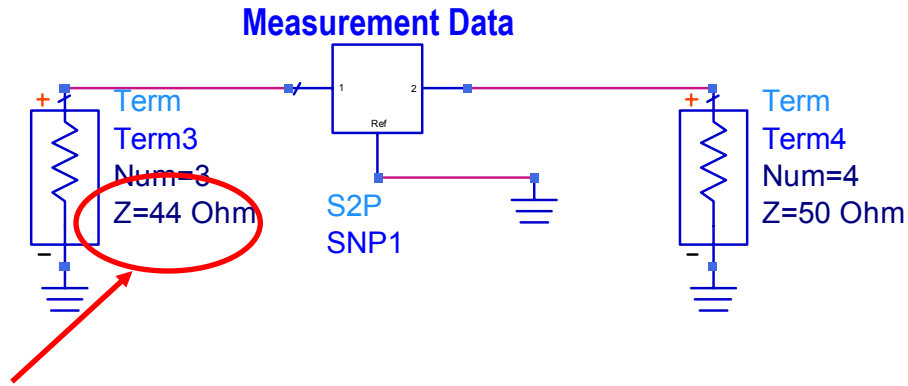


Port

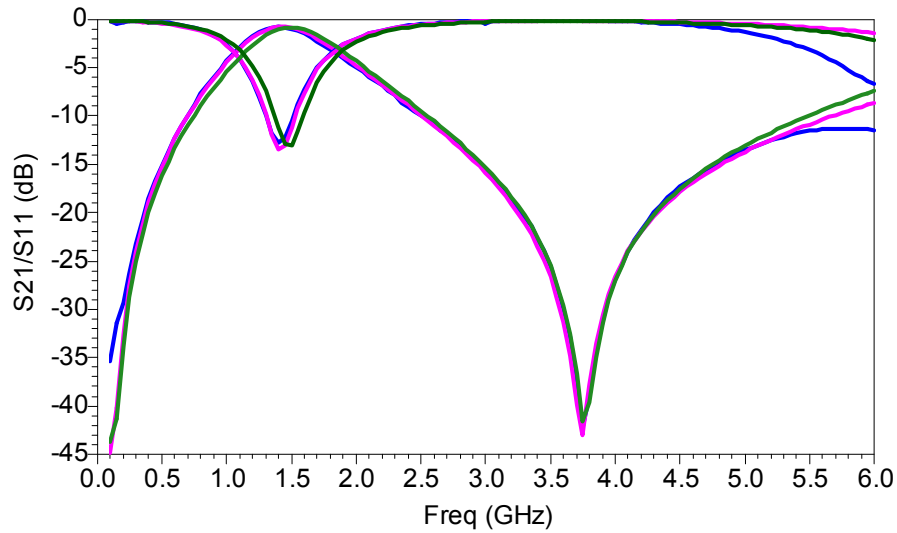


Jsuf
@1.5 GHz

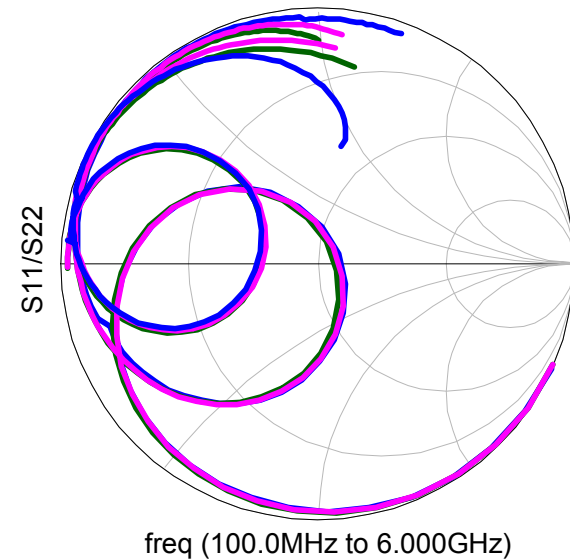
Is Reference 44 Ohm at Probed Port?



If reference to 44 Ohm (measured)



Pink: HFSS Blue: Measurement Green: FDTD



- **Use of SMDs is Very Popular in MCM/SiP RFIC Designs**
- **SMD Can Be Modeled and Simulated Well with HFSS and Spice**
- **Lumped SMD Port Seems Preferable over Lumped RLC**
- **Lumped SMD Port Bears Intrinsic Inductance, and Port Aspect Ratio Could Make Difference**
- **Single-Ended Port with Post Split Can Model SMD Equally Well**

- **Facilitate Lumped Serial RLC Boundary**
- **Implement Post Port Split Matrix Operation**
- **Explore Difference between Lumped Boundary vs. Lumped Port**
- **Facilitate Voltage Contour in Fields Plot**
- **Option to Deembed Lumped Port Intrinsic Inductance**
 - Name as SMD Port?

Acknowledgement



- **Special Thanks to Russ Reisner from Skyworks Solutions for Sharing the Measurement Data and Exploring the Sample Laminate Design**

Thanks