FIRST-PASS SYSTEM SUCCESS

APPLICATION WORKSHOPS FOR HIGH-PERFORMANCE ELECTRONIC DESIGN

Ramping to Volume

-Including Critical PCB/Package Effects in RFIC Design

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UMC Group (USA)

Design Trend

- 1990s: Desktop computing experienced *"Application Spiral"* driving processor performance

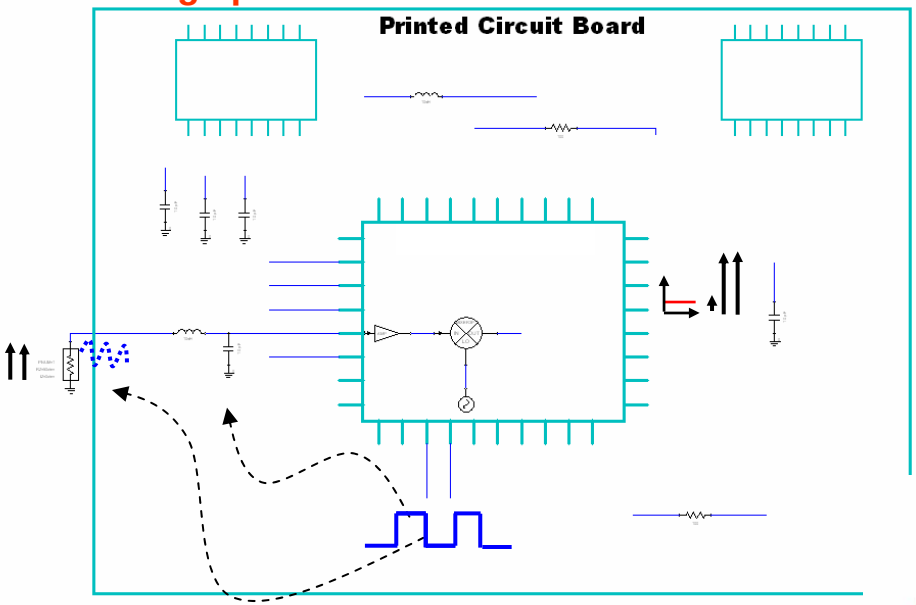
- Today: Handheld device will experience similar *"Application Spiral"* establishing the Wireless Internet
  - Anand Chandrasekher, Intel

- Form-factor, functionality, and integration
- Multicom: GSM, GPS, WiMax, WiFi, RFID, DVB, UWB
- Analog + Digital Integration

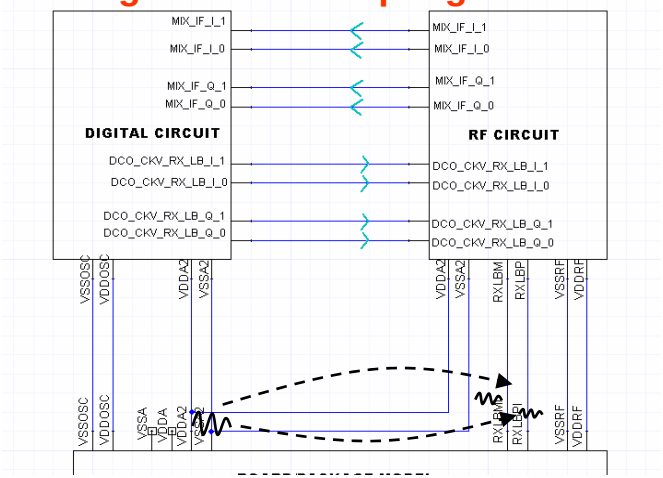
Challenges of First-Pass System Success

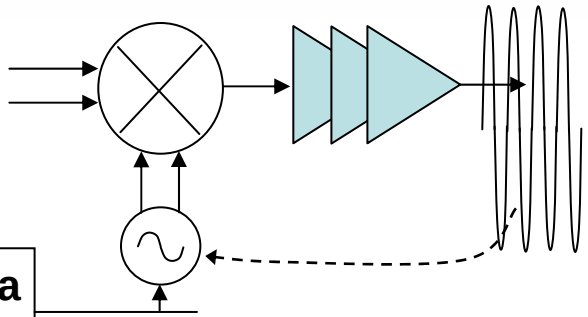
Three Major Challenges in Direct Conversion Transceiver Design

Leakage power ➔ Mixer DC offset ➔ OIP2 or OIP3



Digital noise coupling

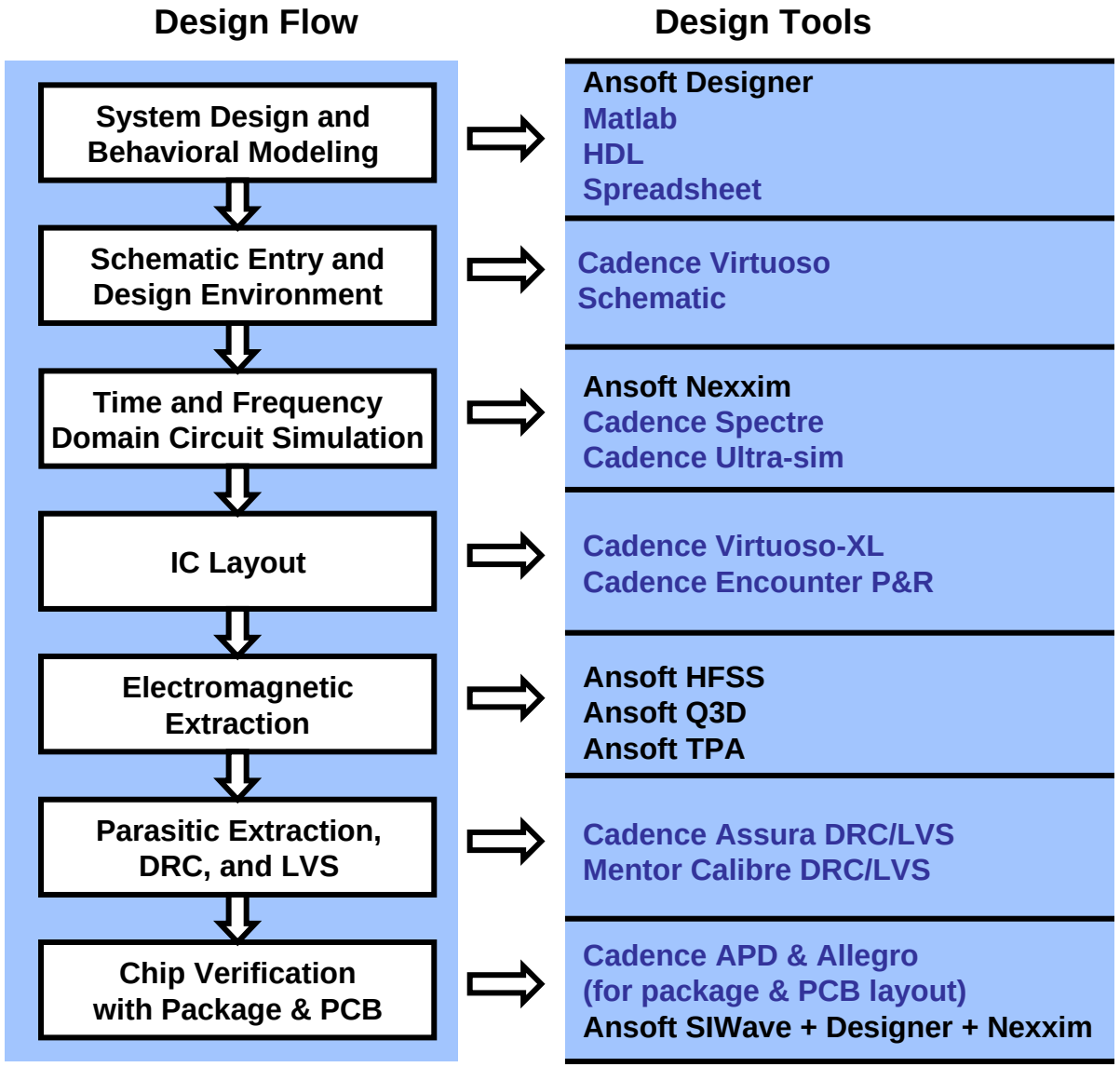




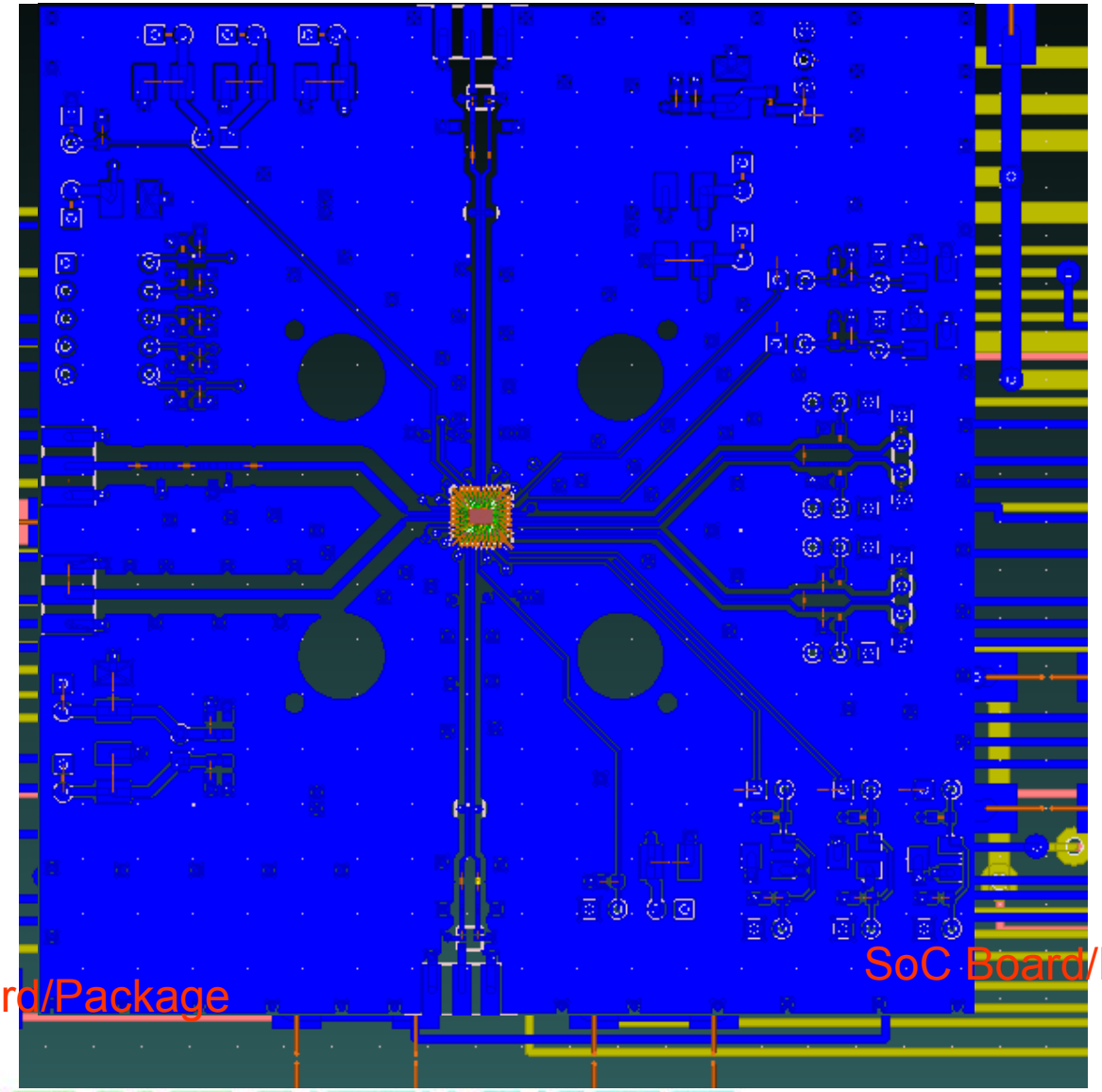
Sigma-Delta PLL

LO pulling

A Platform for First-Pass System Success



Ideal and “Real” PCB/Packages



Test Board/Package

SoC Board/Package

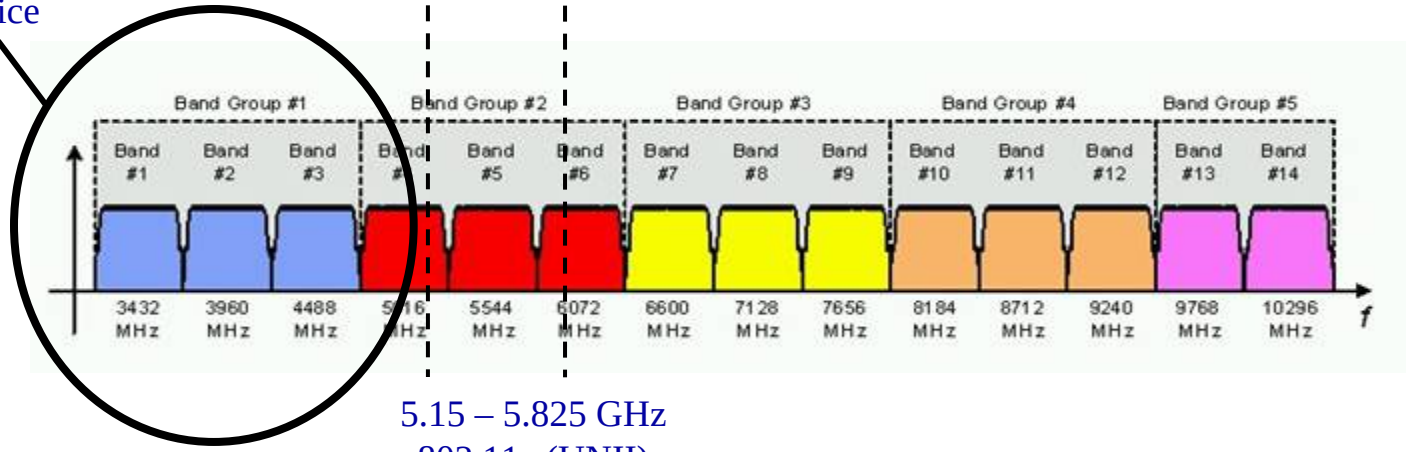
Outline of the Presentation

- Overview of the UWB Radio Design
- Performance in an “ideal” test board/package
  - › Simulation setup
  - › Results with LO clock traces
    - — Leakage power ➔ DC offset ➔ P1dB, OIP2 or OIP3
  - › Results without LO clock traces
    - — Leakage power ➔ DC offset ➔ P1dB, OIP2 or OIP3
- Problems in the “*REAL*” world
  - › The SoC Board/Package Design
  - › Degradation in performance
    - — Leakage power ➔ DC offset ➔ P1dB, OIP2 or OIP3
- A new methodology for handling digital circuits in RF simulations
- Conclusion

Ultra Wideband: Standards and Applications

- Frequency Bands
  - Band Group 1 is mandatory and used in the design
  - Bandwidth = 528MHz, Total Spectrum = 3*528MHz
    - 122 Sub-carriers per 528MHz band
    - Hopping patterns spread signal over entire band group
- Applications
  - Wireless Peripheral Interface (wireless USB)
  - Wireless Body Area Network (WBAN)

Mode 1 Device

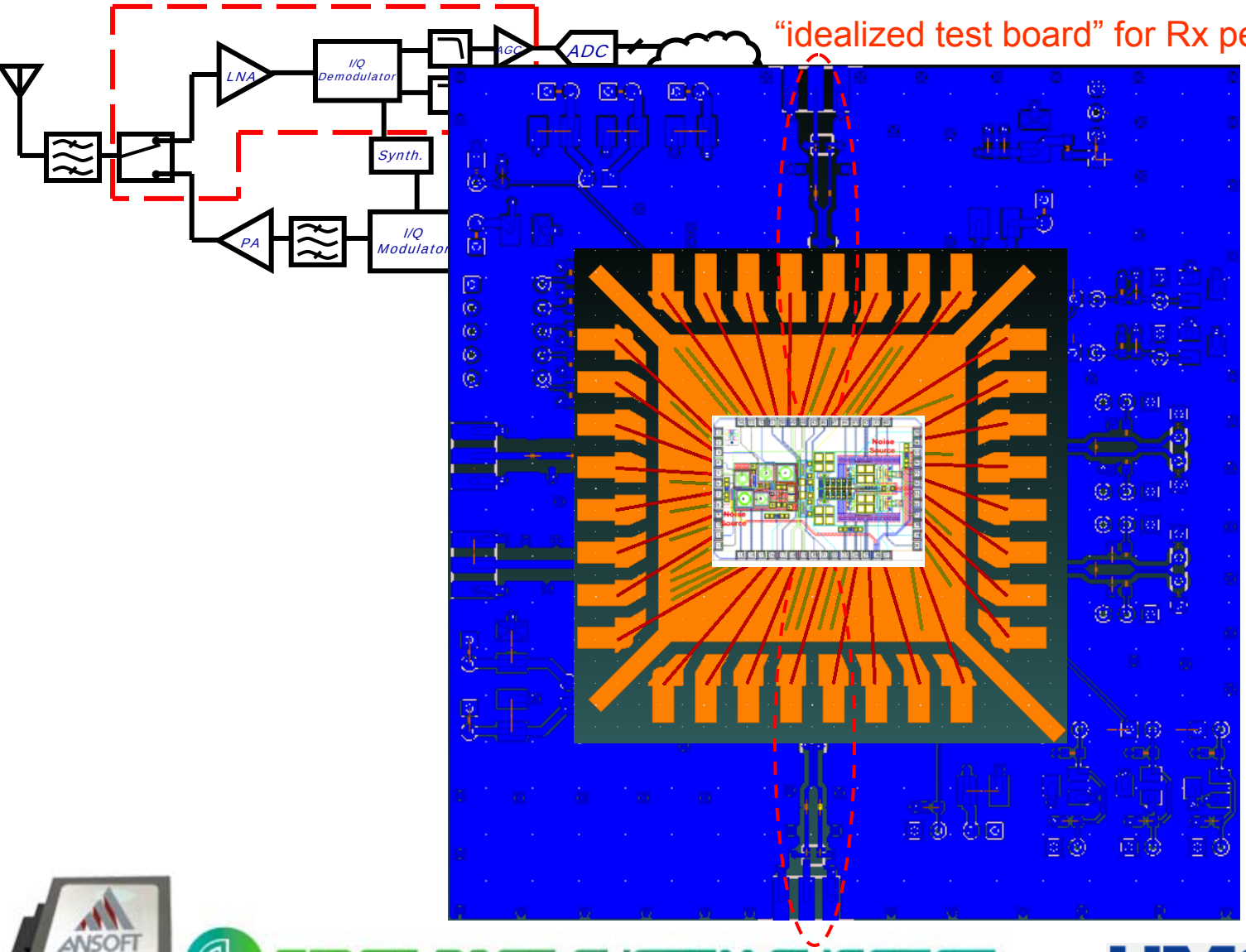


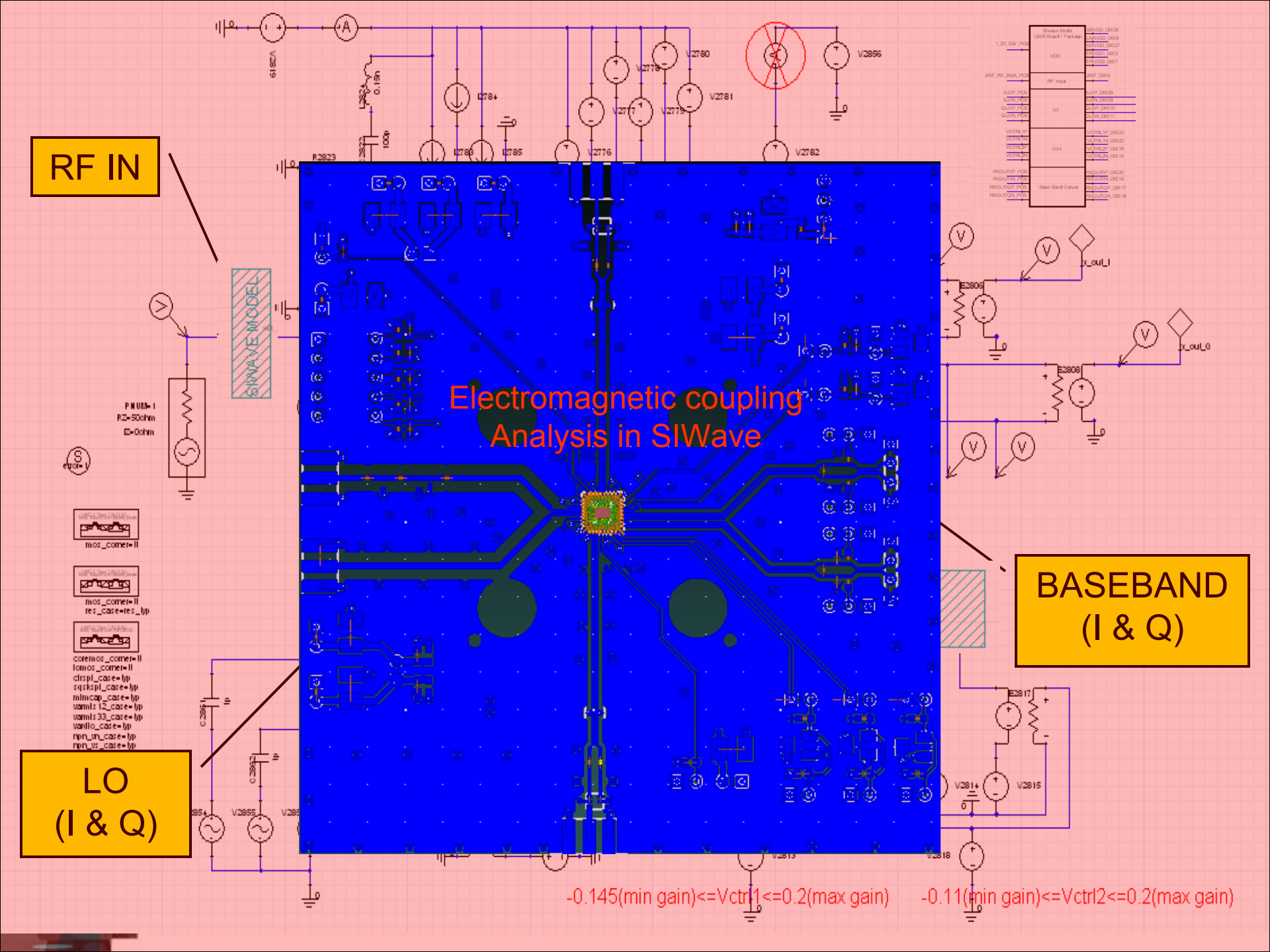
5.15 – 5.825 GHz
802.11a (UNII)

Ref: IEEE P802.15-03/268r3

“Idealized” Test Board/Package

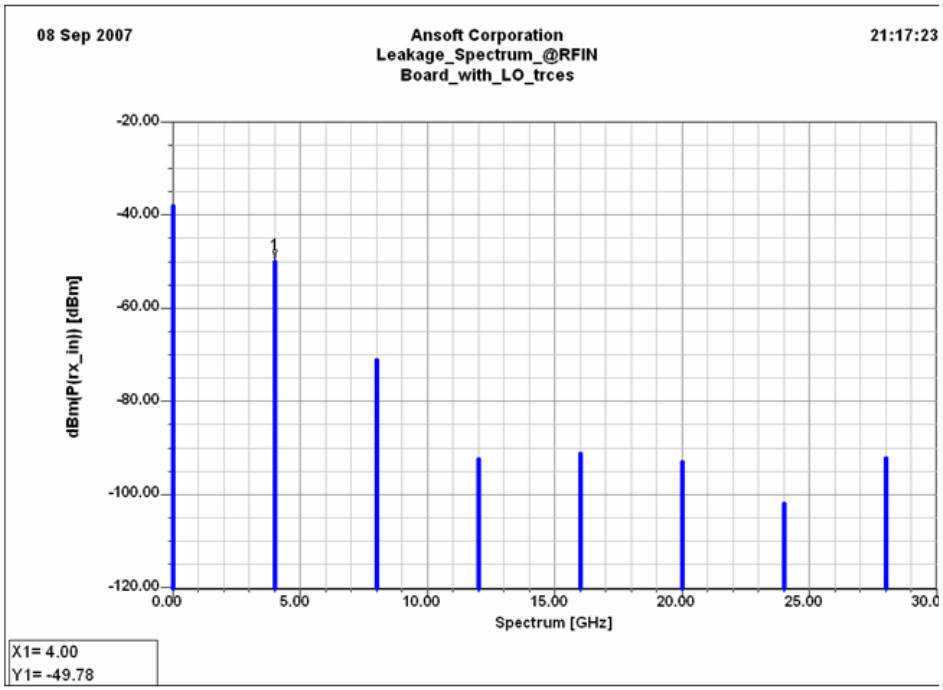
Rx made by Ansoft/UMC 0.13um CMOS process

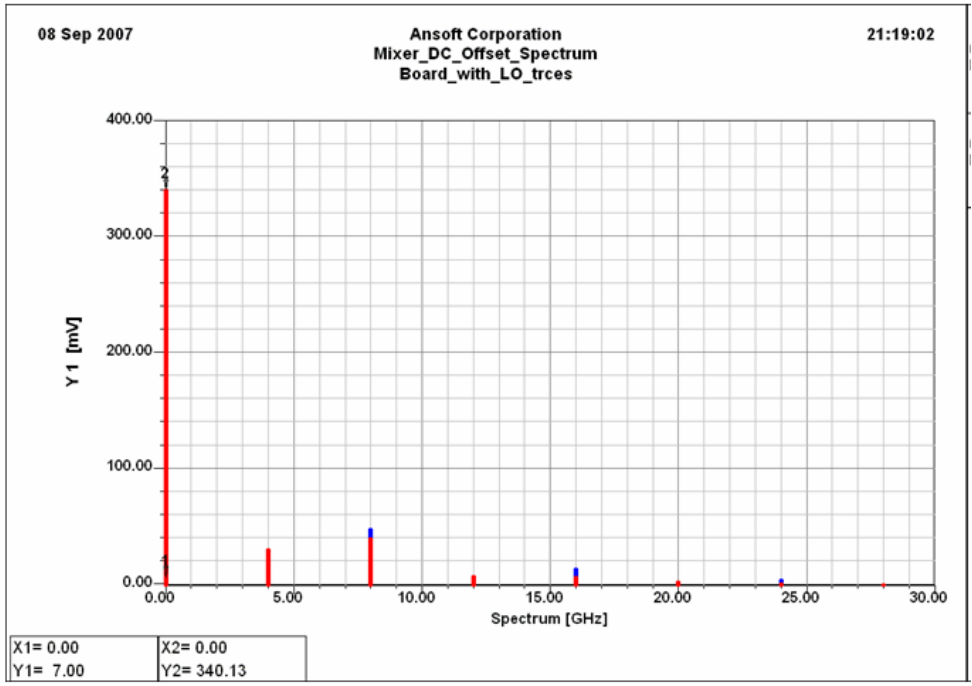



RF IN
Electromagnetic coupling
Analysis in SIWave
BASEBAND
(I & Q)
LO
(I & Q)
-0.145(min gain)<=Vctrl1<=0.2(max gain)
-0.11(min gain)<=Vctrl2<=0.2(max gain)

LO Leakage & Mixer DC Offset on test board with LO traces

1-tone HB Analysis, flo=4GHz, maxK=7



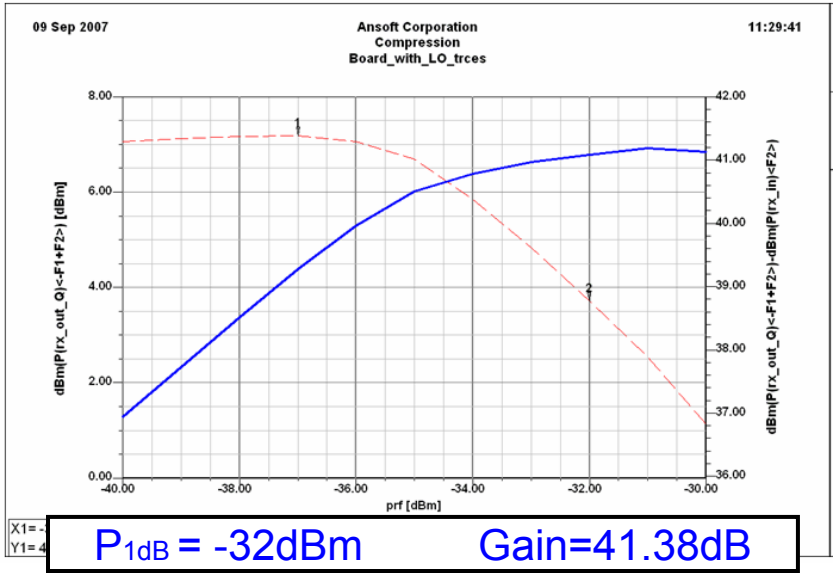


P_{Leak} = -49.78dBm

VIoffset=7mV VQoffset=340.13mV

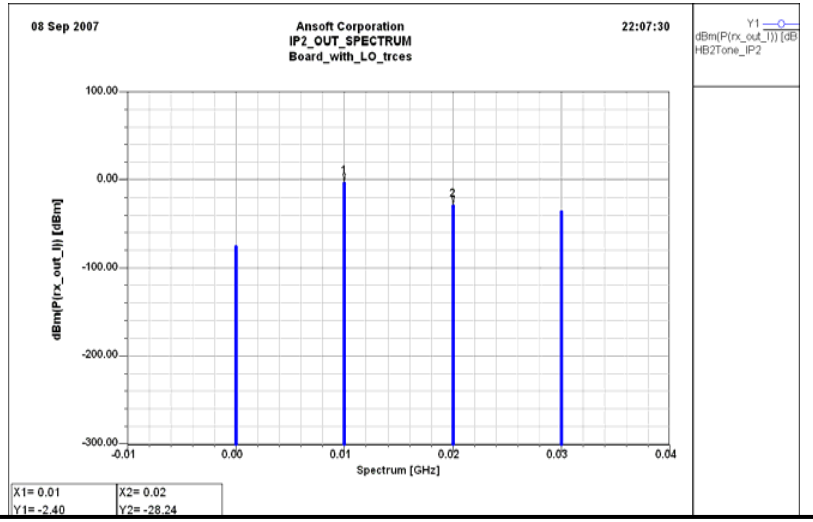
P1dB, OIP2, & OIP3 on test board with LO traces

2-tone HB Analysis, flo=4GHz, frf=4.01GHz



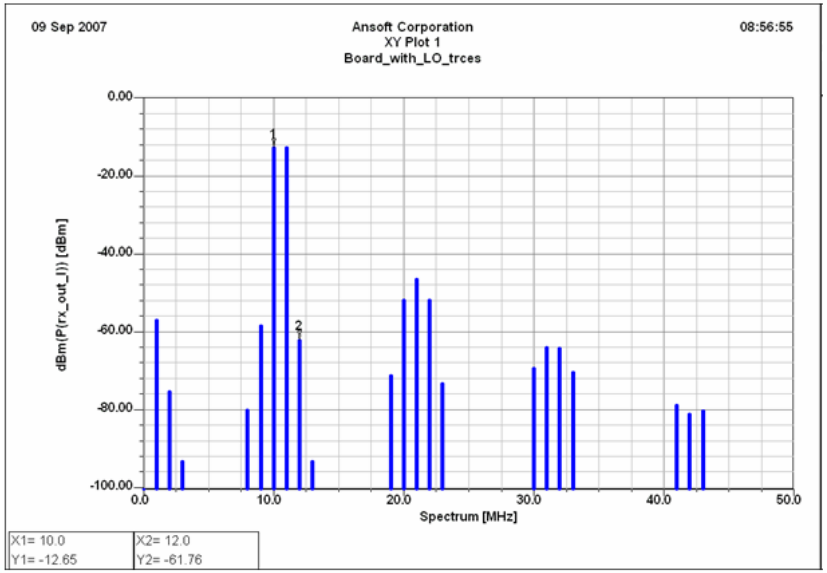
P_{1dB} = -32dBm Gain=41.38dB

@ Pin = -40dBm

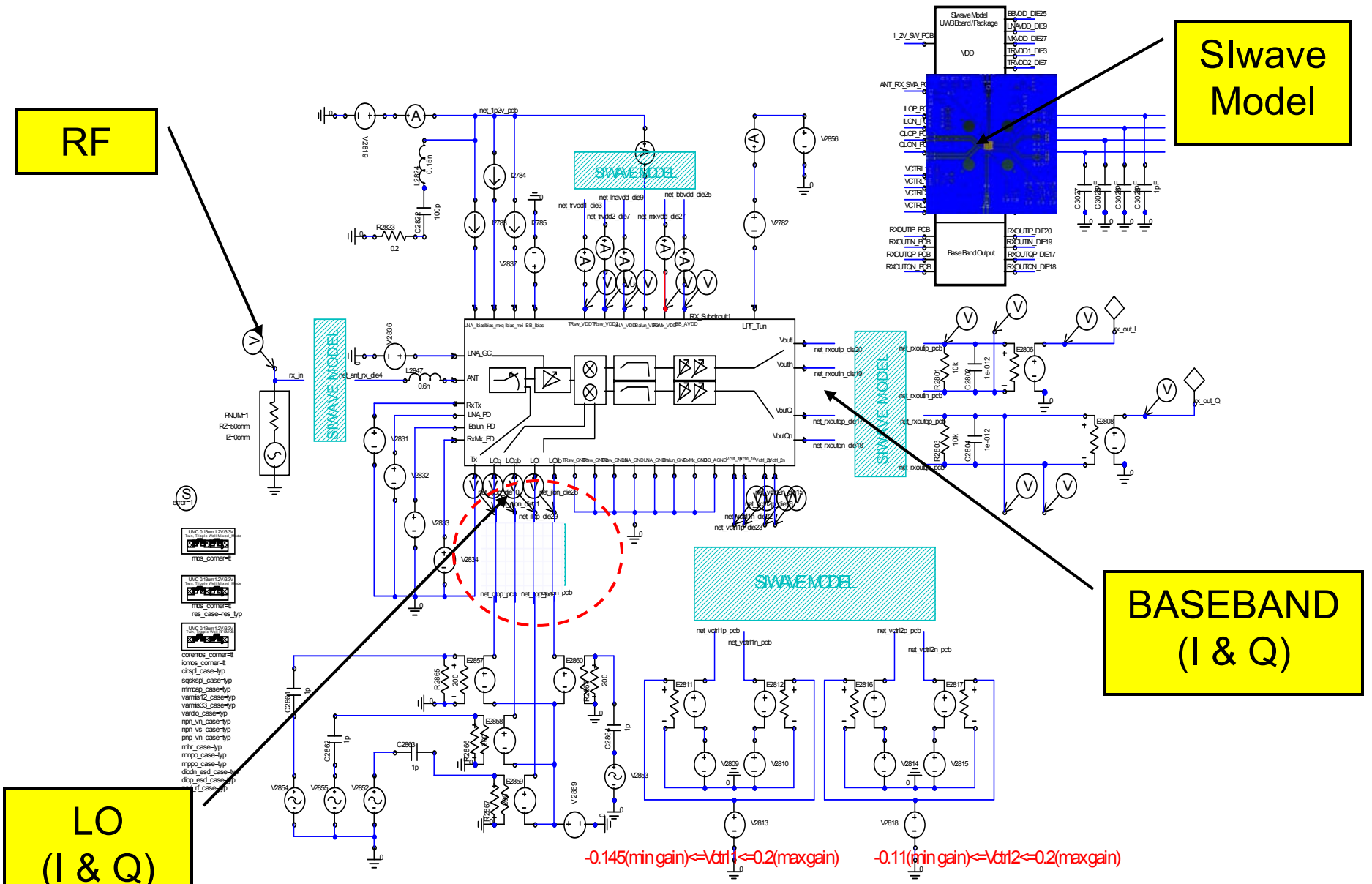


OIP2= 2*Prf-Pspur=2*(-2.4)-(-28.24) =23.44 (dBm)

3-tone HB Analysis
flo=4GHz
frf=4.01GHz
frf2=4.011GHz
Pin = -50dBm

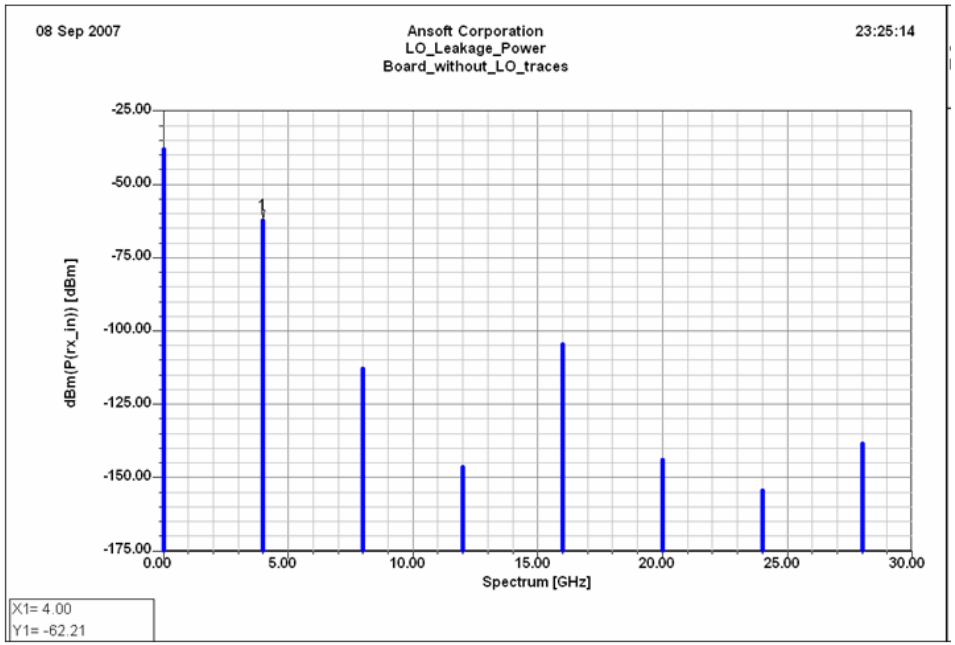


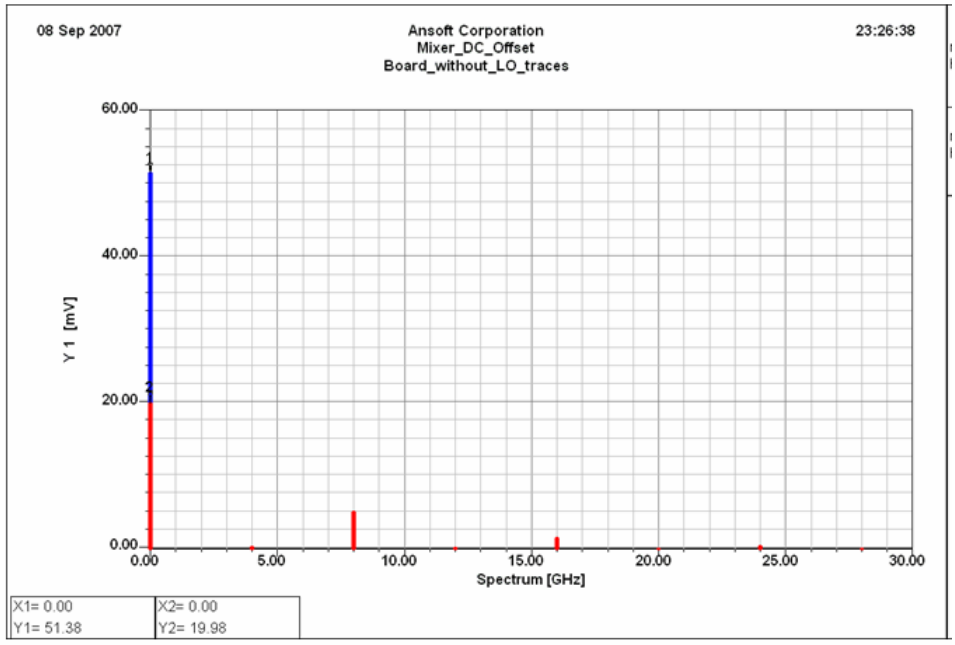
OIP3= Prf+(Prf-Pspur)/2
=-12.65-(-12.65-(-61.76))/2
=11.9 (dBm)


RF
SIwave Model
BASEBAND (I & Q)
LO (I & Q)
SIWAVE MODEL
-0.145(min gain)<=Vctrl1<=0.2(max gain)
-0.11(min gain)<=Vctrl2<=0.2(max gain)

LO Leakage & Mixer DC Offset on test board w/o LO traces

1-tone HB Analysis, flo=4GHz, maxK=7





P_{Leak} = -62.21dBm

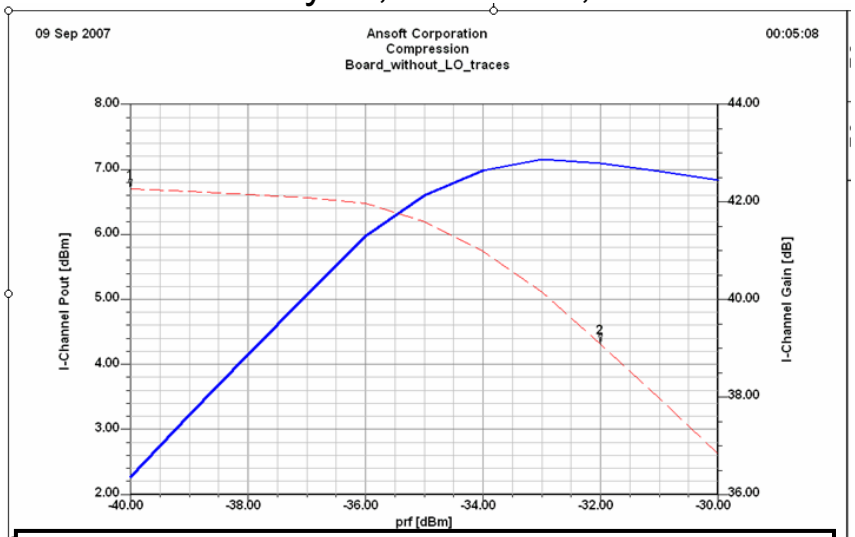
Vloffset=51.38mv VQoffset=19.98mv

P_{Leak} = -49.78dBm with LO traces

Vloffset =7mv VQoffset=340.13mv with LO traces

P_{1dB}, OIP2, & OIP3 on test board without LO traces

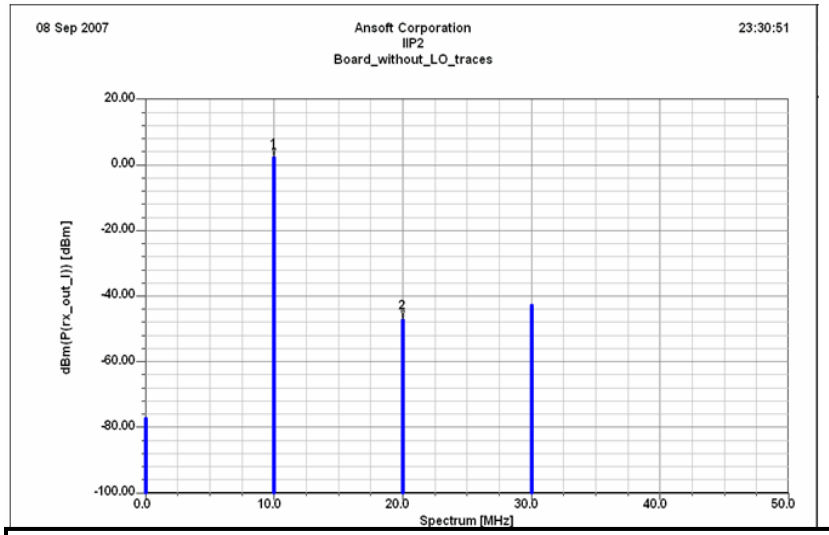
2-tone HB Analysis, flo=4GHz, frf=4.01GHz



P_{1dB} = -32dBm Gain=44.27dB

P_{1dB} = -32dBm Gain=41.38dB with LO traces

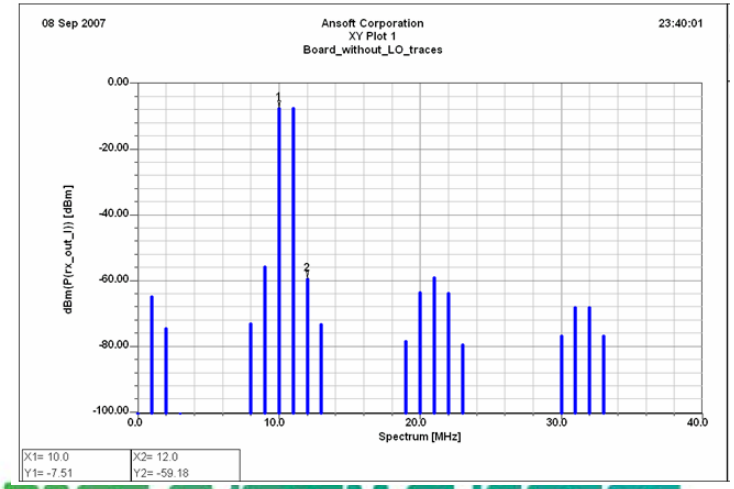
@ Pin = -40dBm



OIP2= 2*Prf-Pspur=2*(2.27)-(-47.04) =52.58 (dBm)

OIP2=23.4dBm with LO traces

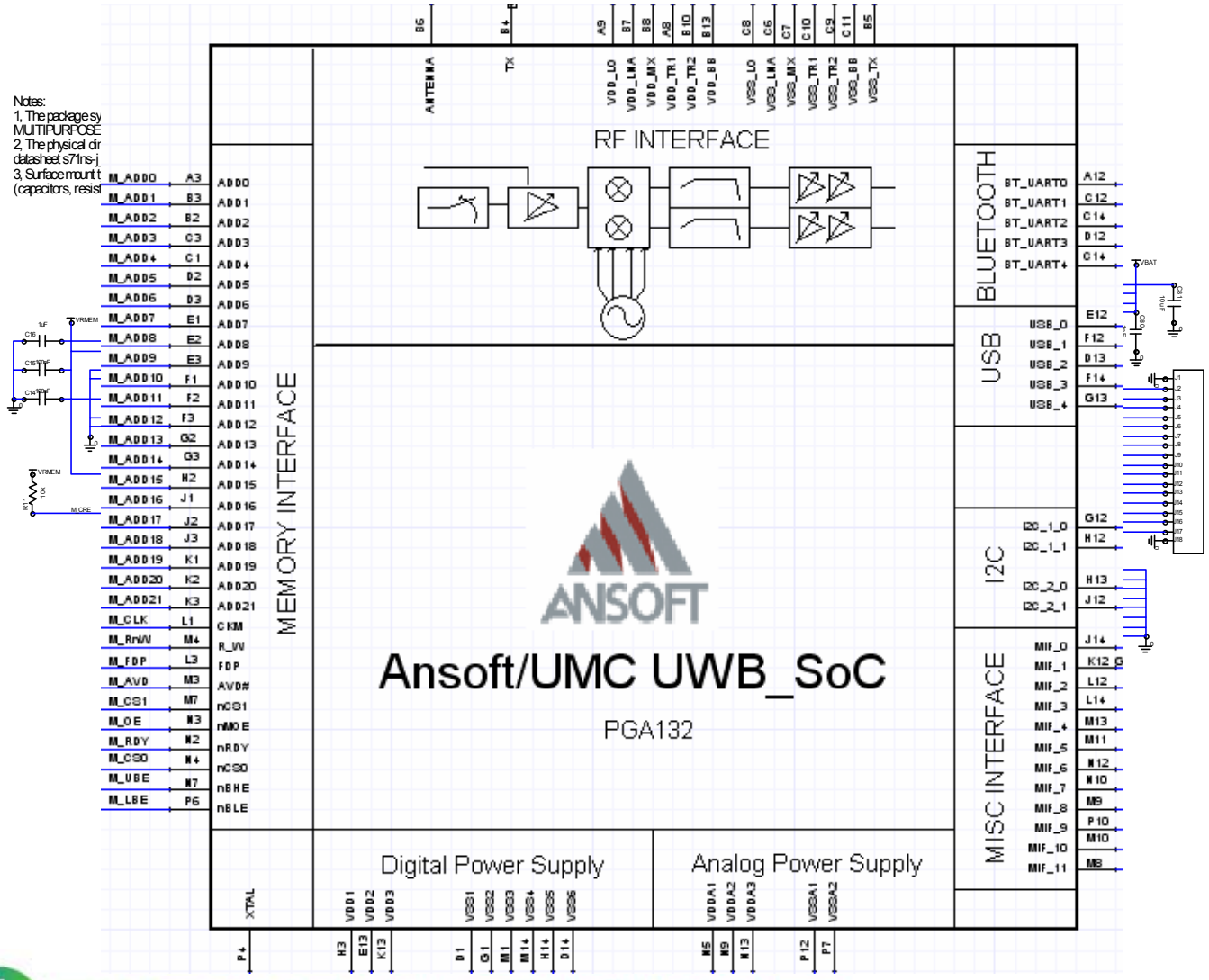
3-tone HB Analysis
flo=4GHz
frf=4.01GHz
frf2=4.011GHz
Pin = -50dBm



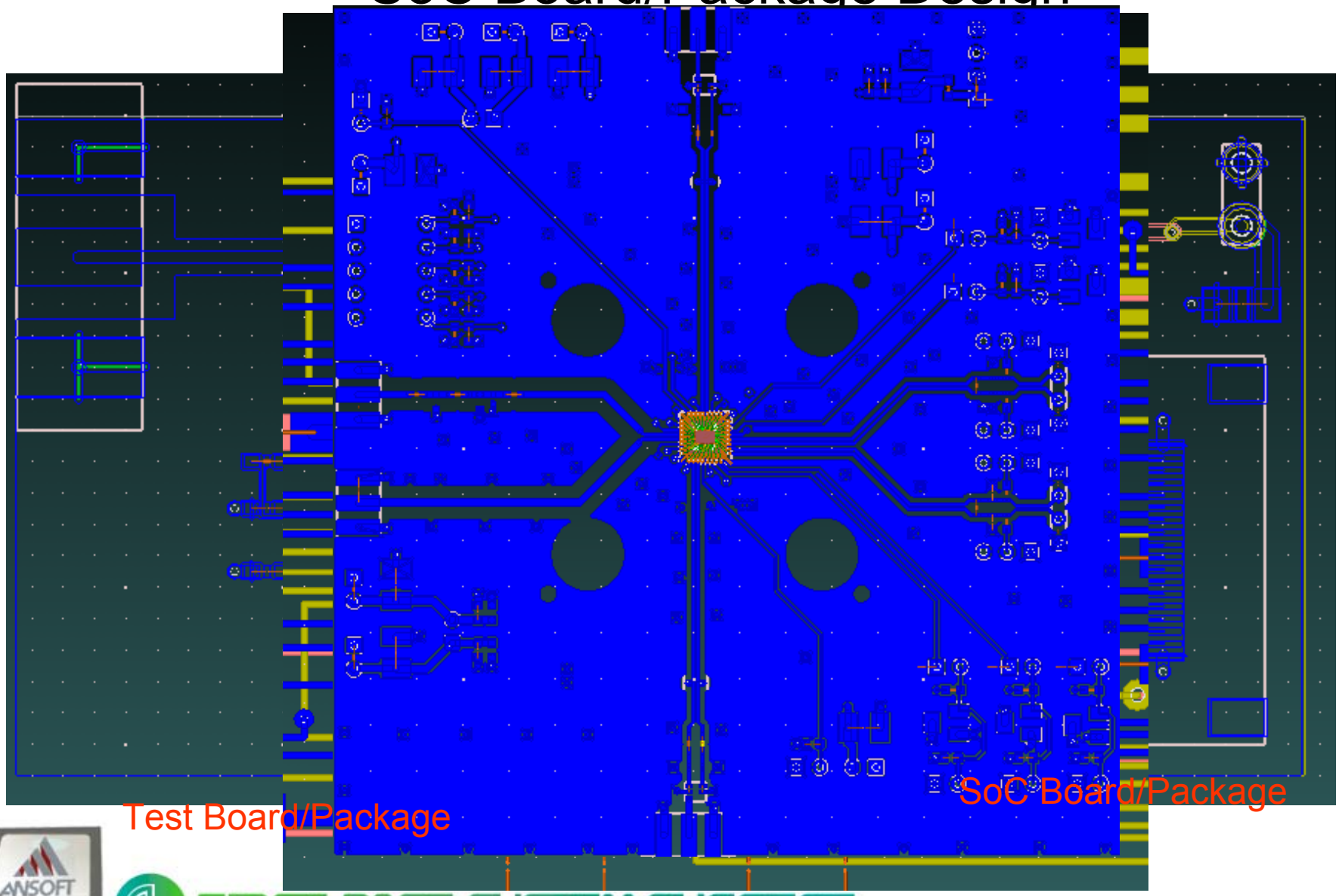
OIP3= Prf+(Prf-Pspur)/2
=(-7.51)-(-7.51-59.18)/2
=18.33 (dBm)

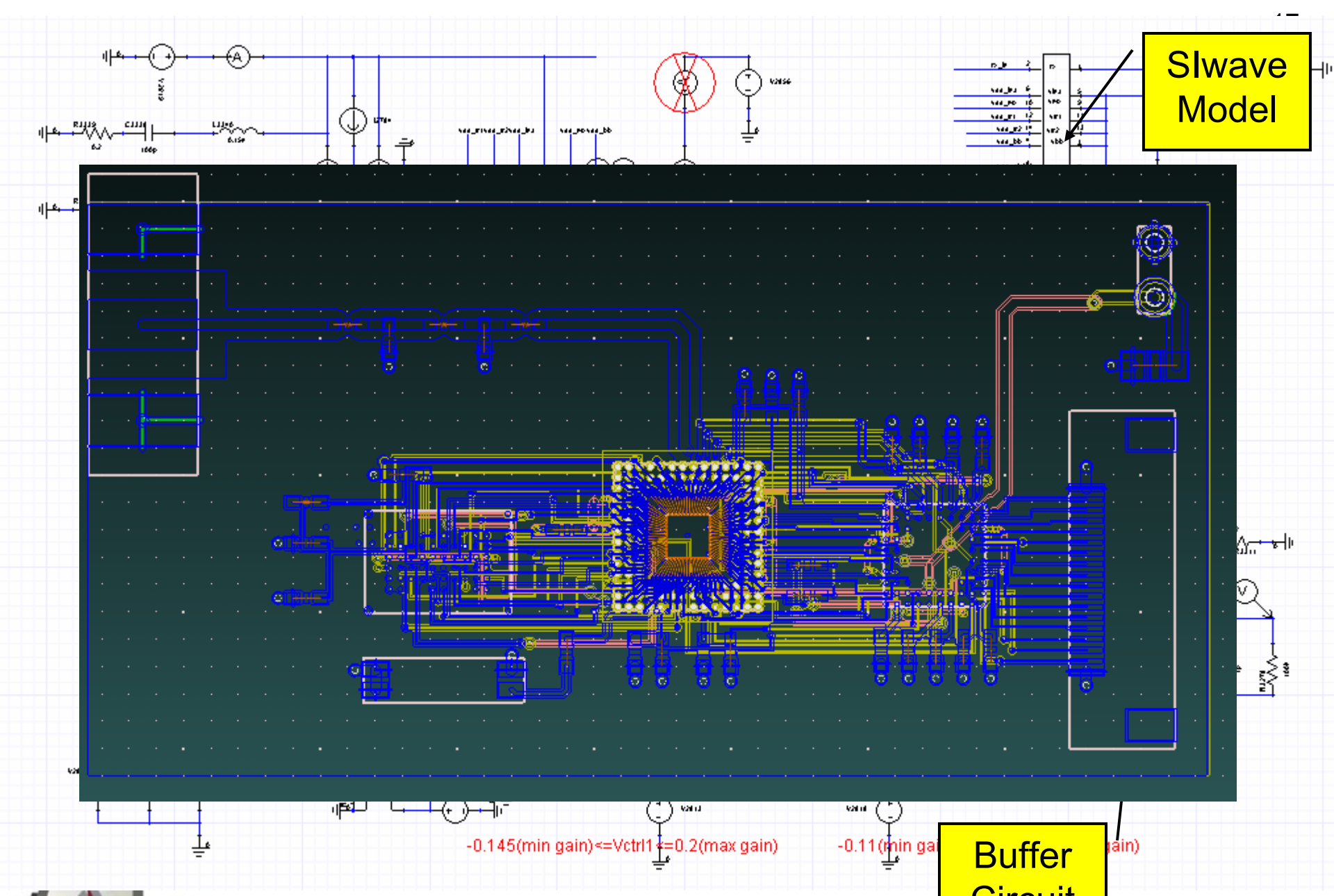
OIP3= 11.9dBm with LO traces

An SoC Scenario



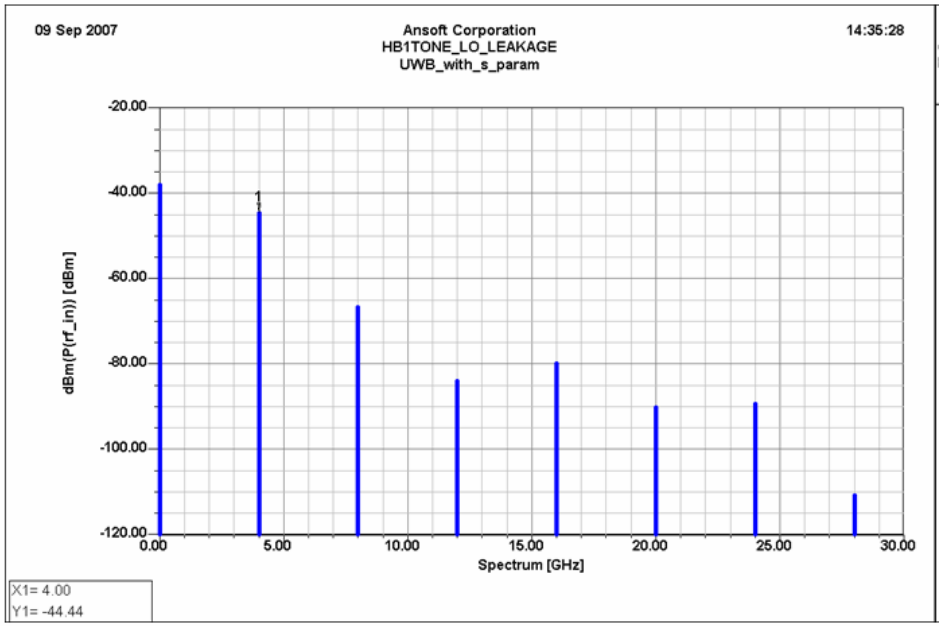
SoC Board/Package Design

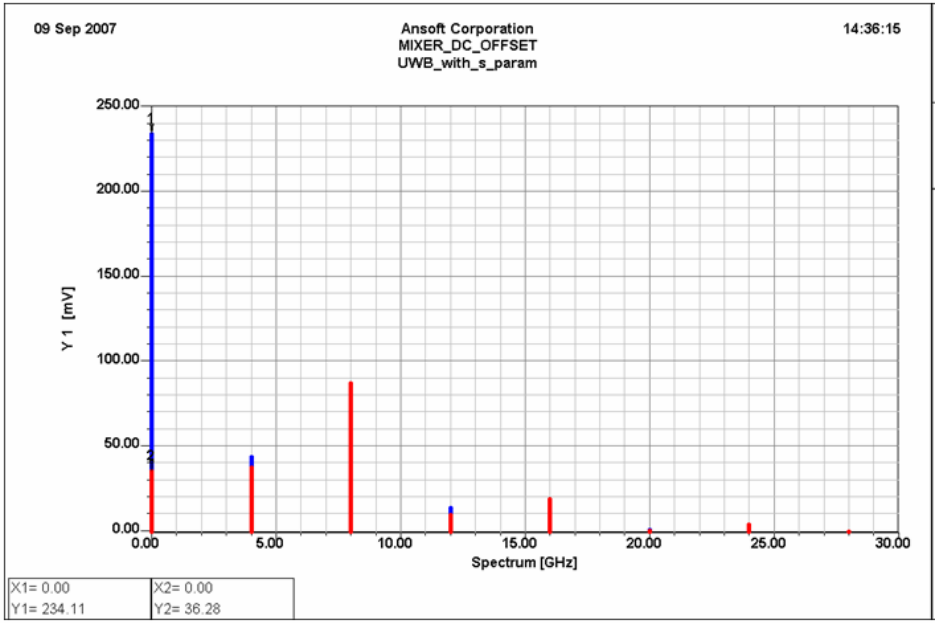



SIwave Model
-0.145(min gain)<=Vctrl1<=0.2(max gain)
Buffer Circuit

LO Leakage & Mixer DC Offset on SoC brd/pkg with LO Buffer

1-tone HB Analysis, flo=4GHz, maxK=7



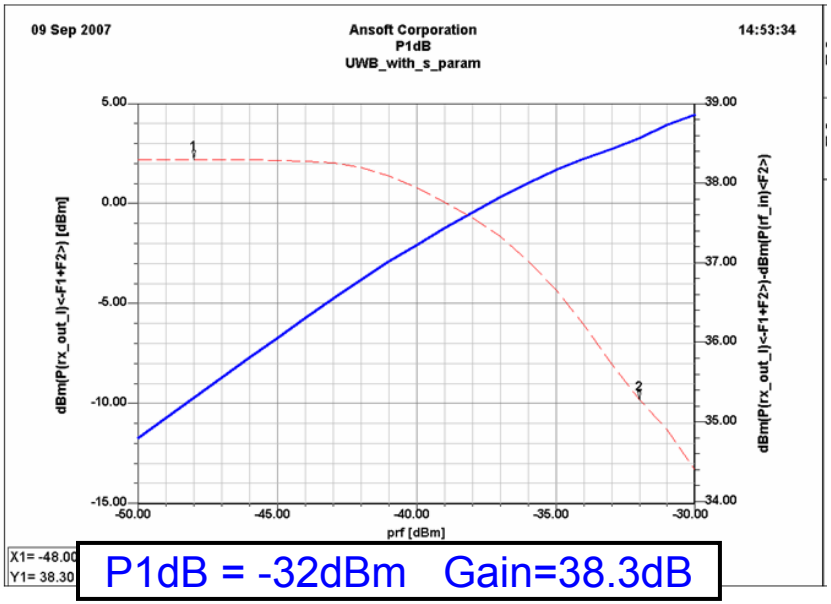


P_{Leak} = -44.44dBm

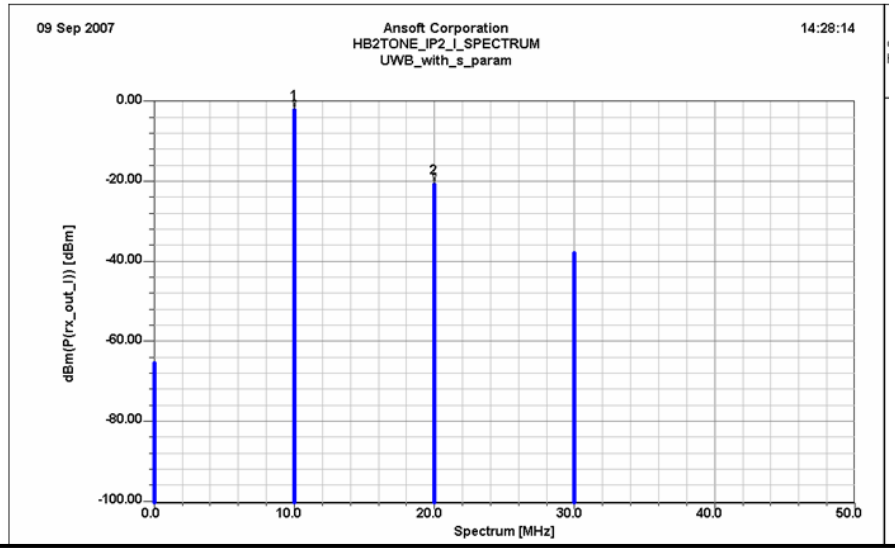
VIoffset=234.11mv VQoffset=36.28mv

P1dB, OIP2, & OIP3 on SoC brd/pkg with LO Buffer

2-tone HB Analysis, flo=4GHz, frf=4.01GHz @ Pin = -40dBm

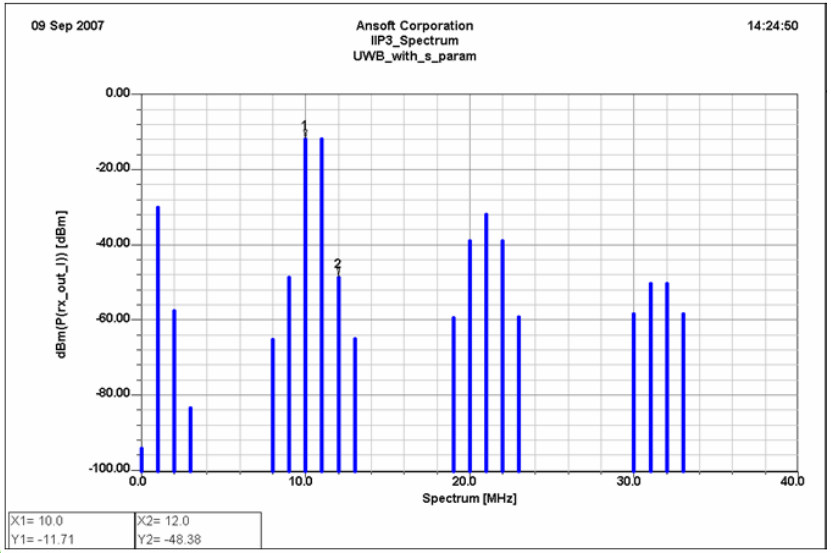


P1dB = -32dBm Gain=38.3dB



OIP2= 2*Prf-Pspur=2*(-2.05)-(-20.59) =16.5(dBm)

3-tone HB Analysis
flo=4GHz
frf=4.01GHz
frf2=4.011GHz
Pin = -50dBm

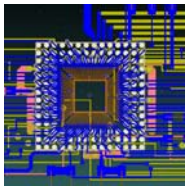


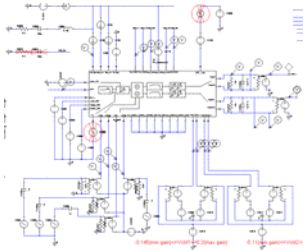
OIP3= Prf+(Prf-Pspur)/2
=(-11.71)-(-11.71-(-48.38))/2
=6.63 (dBm)

Summary of Results

Performance Parameter	Test brd/pkg with LO Traces	Test brd/pkg w/o LO Traces	SoC brd/pkg With LO Buffer
LO Leakage Power (dBm)	-49.78	-62.1	-44.44
Mixer DC Offset (mV)	340.1(I)+7.0(Q)	51.4(I)+19.4(Q)	234.1(I)+36.1(Q)
Gain (dB)	41.38	44.27	38.3
P1dB (dBm)	-32.0	-32.0	-32.0
OIP2 (dBm)	23.44	52.58	16.5
OIP3 (dBm)	11.9	18.33	6.63

One solver, two domains

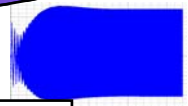




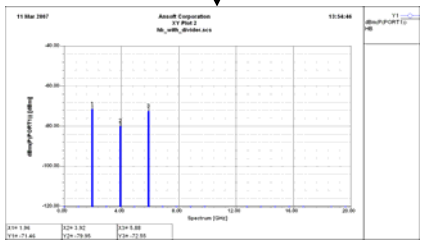
Circuit Design

State-Space Fitting

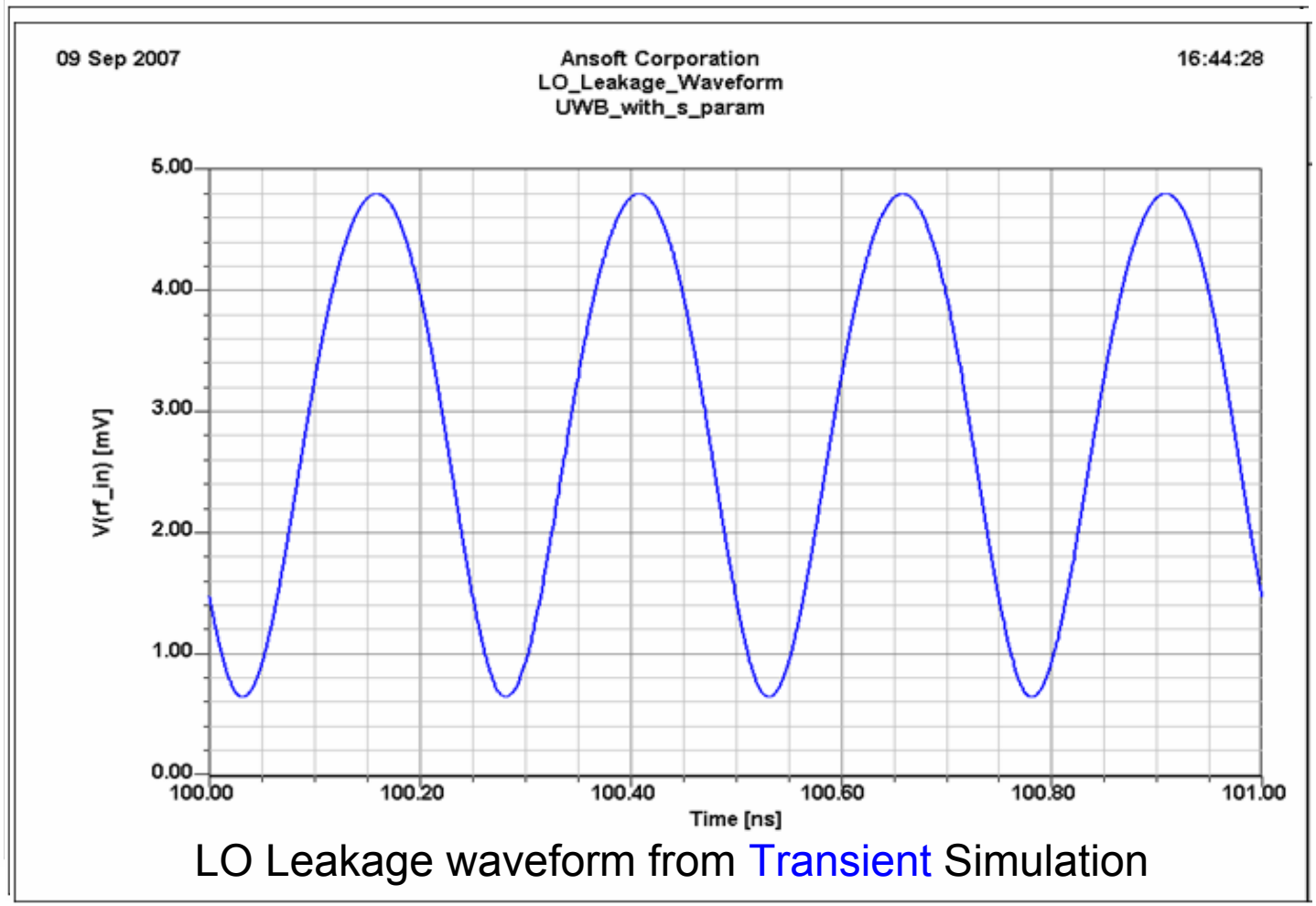
Solver



Fast Fourier Transform

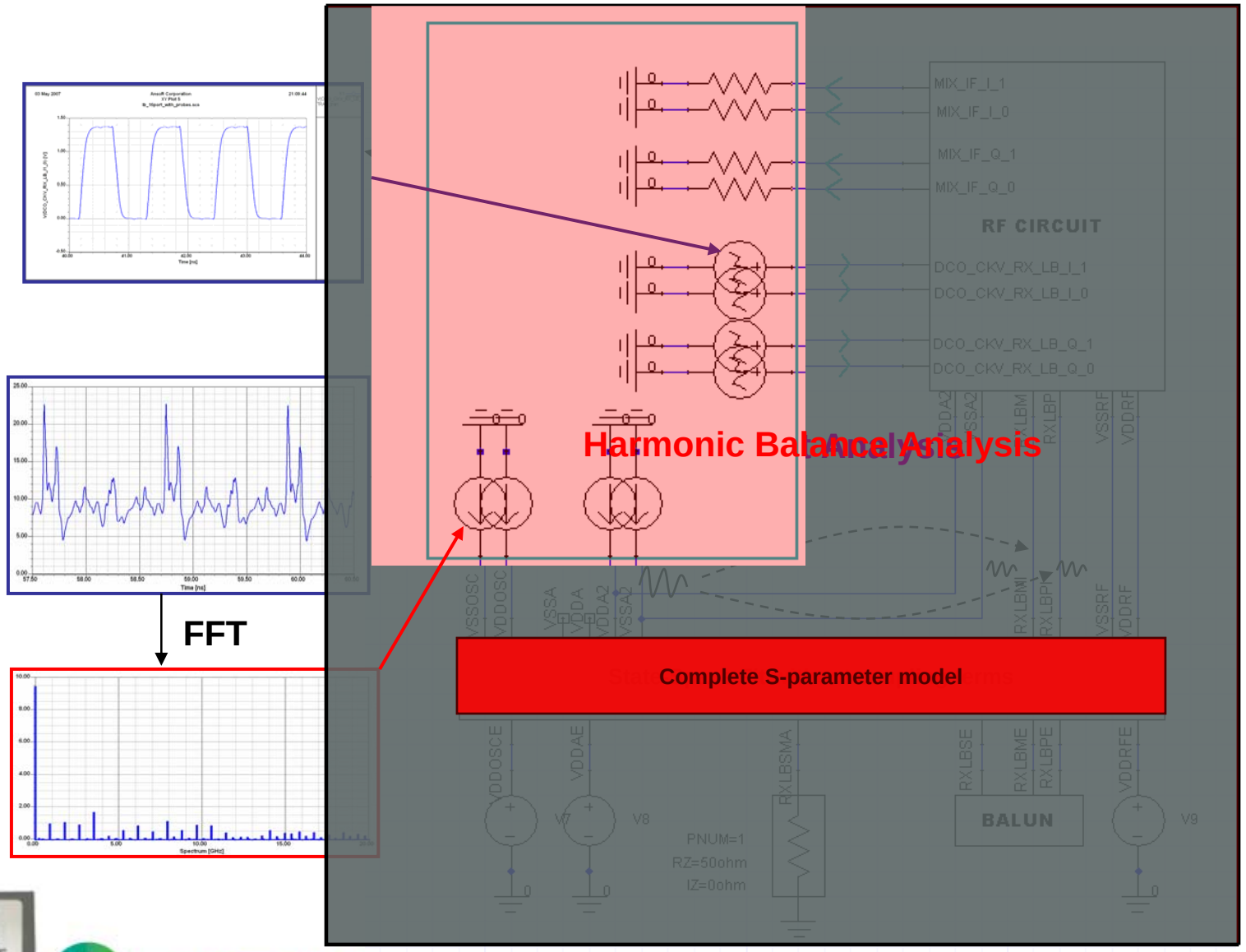


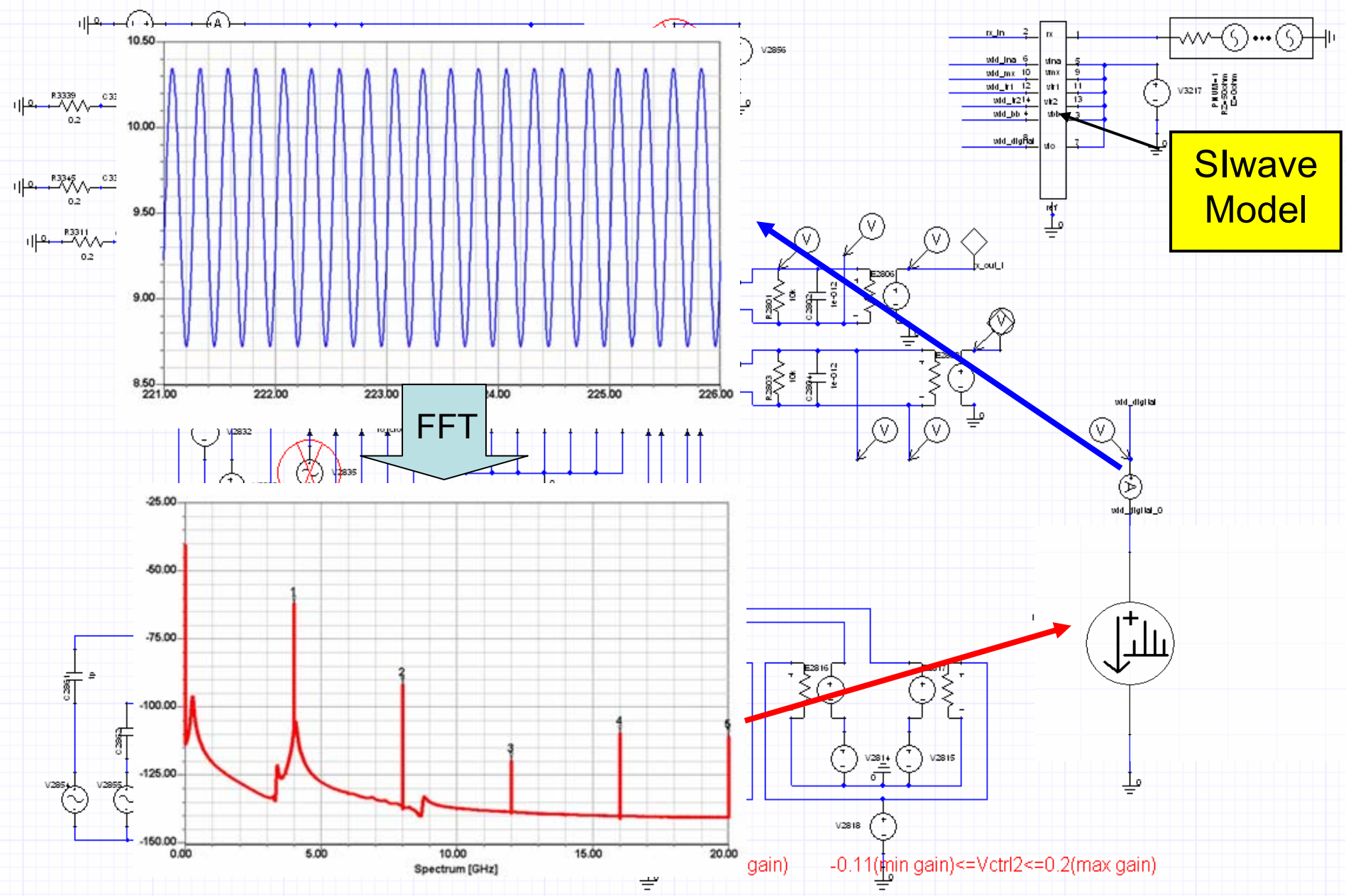
Two domains, Same Result



LO Leakage waveform from Transient Simulation

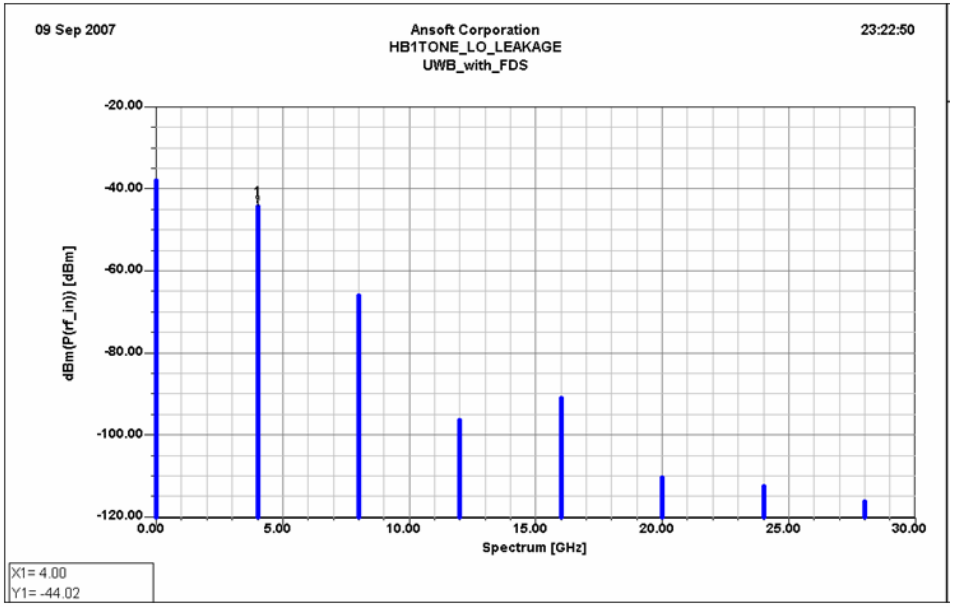
A New Methodology for RFIC Signal Integrity

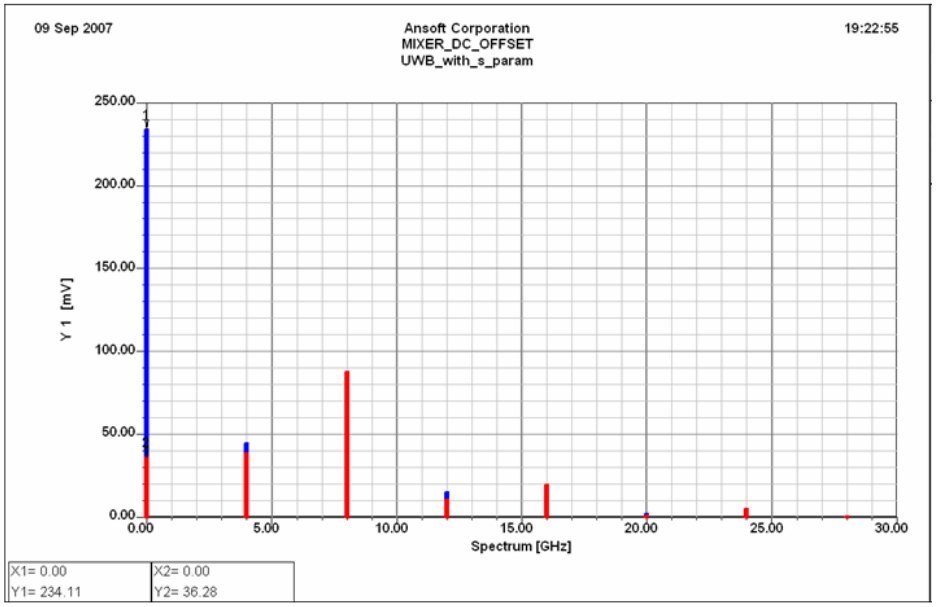



SIwave Model
FFT
Spectrum [GHz]
gain)
-0.11(min gain)<=Vctrl2<=0.2(max gain)

LO Leakage & Mixer DC Offset on SoC brd/pkg with LO Buffer

1-tone HB Analysis, flo=4GHz, maxK=7





P_{Leak} = -44.02dBm

P_{Leak} = -44.44dBm from pure HB simulation

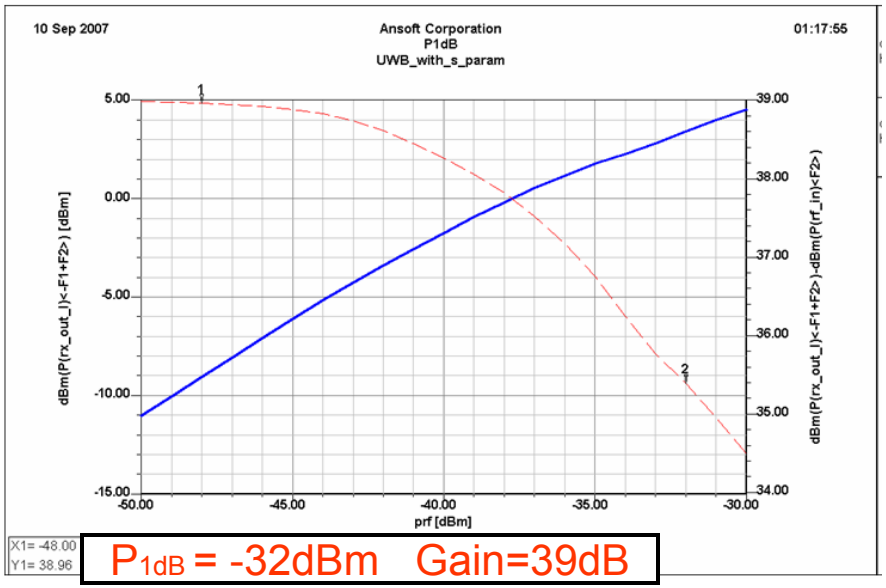
Vloffset=234.11mv VQoffset=36.28mv

Vloffset=234.11mV VQoffset=36.28mV from pure HB simulation

P1dB, OIP2, & OIP3 on SoC brd/pkg with LO Buffer

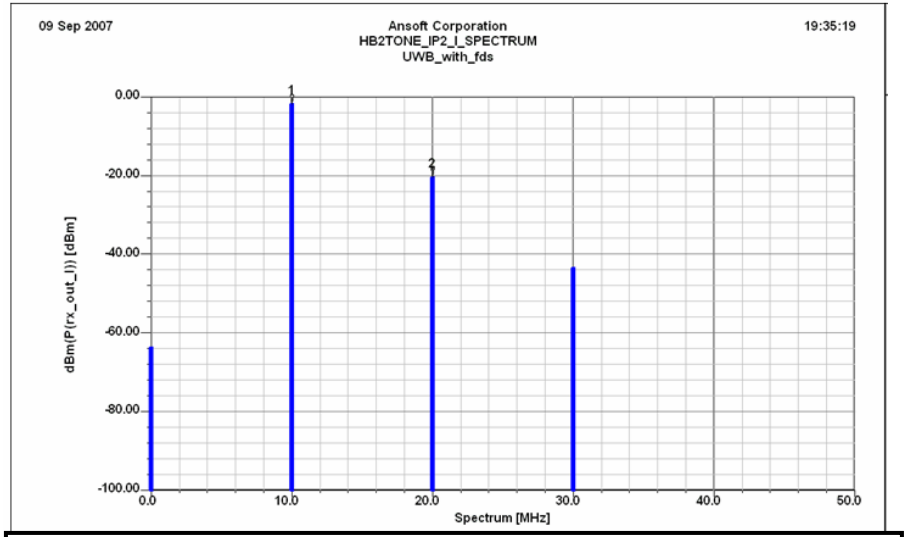
2-tone HB Analysis, flo=4GHz, frf=4.01GHz

@ Pin = -40dBm



P_{1dB} = -32dBm Gain=39dB

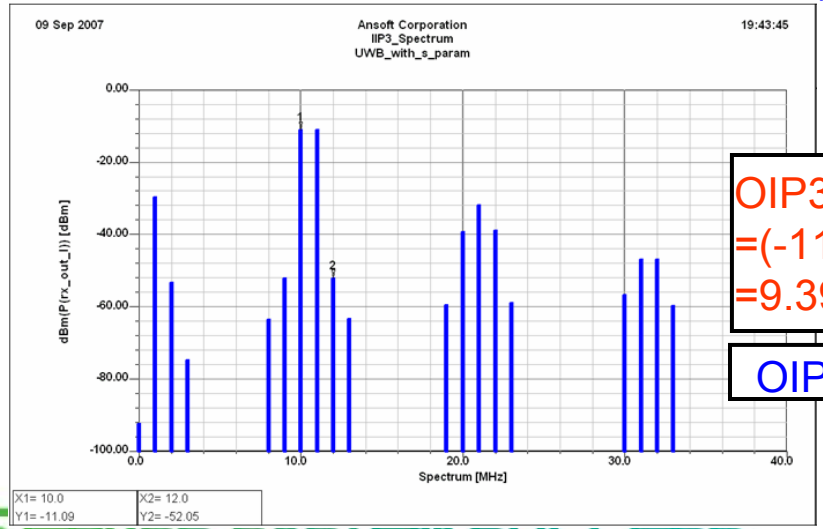
P_{1dB} = -32dBm Gain=38.3dB from pure HB simulation



OIP2= 2*Prf-Pspur=2*(-1.74)-(-20.47) =16.99(dBm)

OIP2= =16.5(dBm) from pure HB simulation

3-tone HB Analysis
flo=4GHz
frf=4.01GHz
frf2=4.011GHz
Pin = -50dBm



OIP3= $P_{rf}+(P_{rf}-P_{spur})/2$
=(-11.09)-(-11.09-(-52.05))/2
=9.39 (dBm)

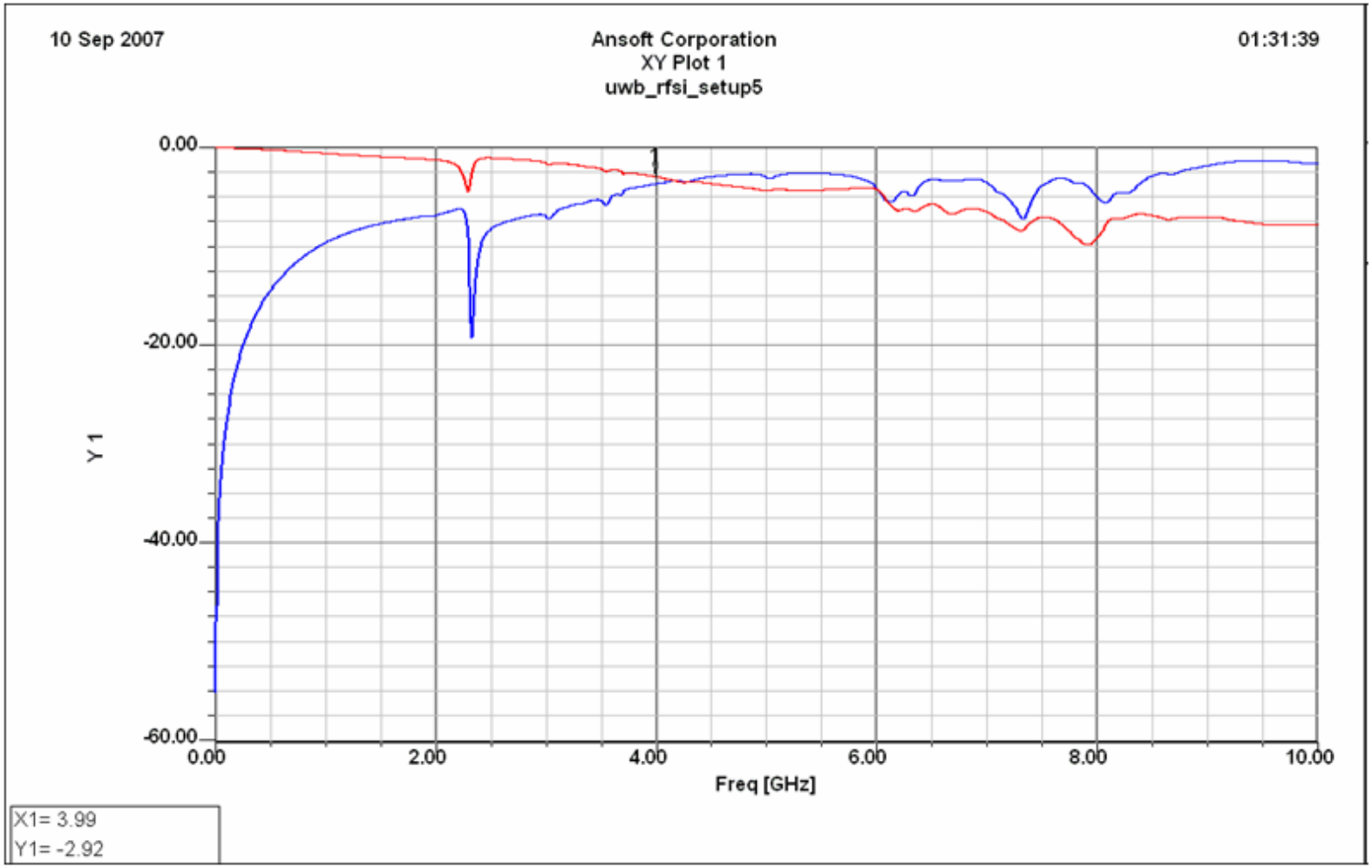
OIP3= 6.36 dBm from pure HB simulation

Conclusions

- The performance of a UWB receiver circuit varied significantly in three different board/package environment.
- Simulation tools from Ansoft enable designers to *predict* the performance of the RF circuit in situ, and thus achieve first-pass system success while ramping to volume in production.
- A new methodology was introduced to include the effects digital noise in RF performance evaluation.

Questions?

RF Signal Path on SoC Brd/Pkg



U