Design of a Custom Printed Circuit Board for a Receiver System in Package (SiP) Test

2003 HFSS Users' Workshop
February 21, 2003

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Overview

- Ditrans uses RF input return loss as a key metric comparing Ditrans' digital receiver module measurement and simulation
- All testing must be conducted with the module in a socket on a test board
- Problems
  - The test board and socket affect the measured RF performance of Ditrans' module
  - The Ball Grid Array (BGA) pad interface at the module prevents any direct measurement at that interface
- Solution
  - De-embed the test board and socket at the module interface

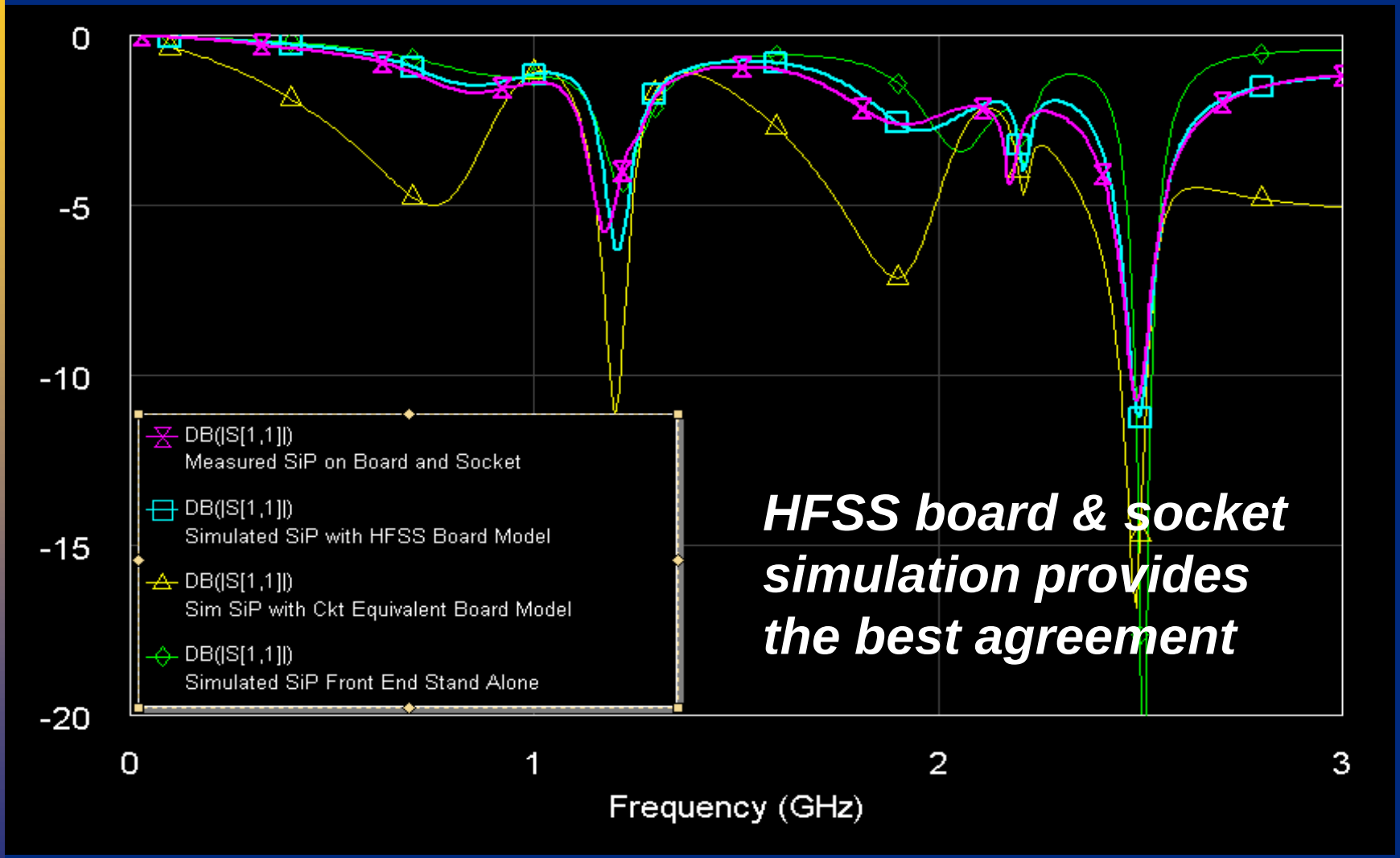
Overview

- Mass production efforts would use dedicated, custom ceramic substrate to perform a calibration at the socket-SiP interface
  - Not cost effective or timely for prototype effort
- Board and socket lumped element equivalent circuit yields poor return loss prediction
- HFSS derived 3D EM model incorporates the entire test board & socket geometry into a single simulation and improves the module measured v. modeled agreement

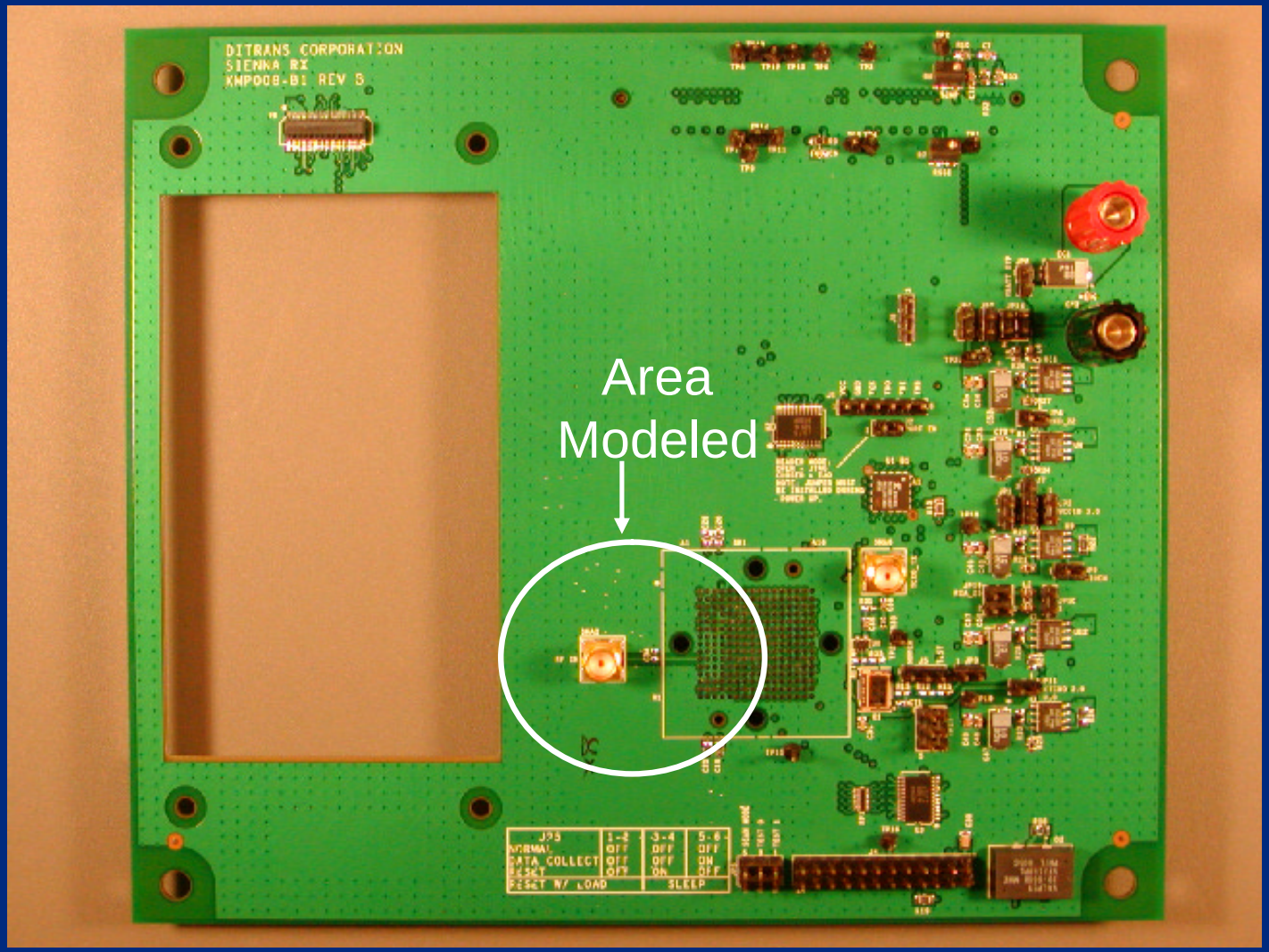
Overview

- **HFSS Versatility**
  - **Basic HFSS geometry can be used to evaluate alternative socket and socket materials**
- **Simulations of a “direct attach” of the module to the PCB using BGA solder balls also completed**
  - **Customers will evaluate the Ditrans’ receiver directly attached to a reference board**
  - **Ditrans can account for the impacts of the reference board on measurements with HFSS board simulations**
  - **HFSS simulations can account for performance variations with and without epoxy underfill beneath the module**

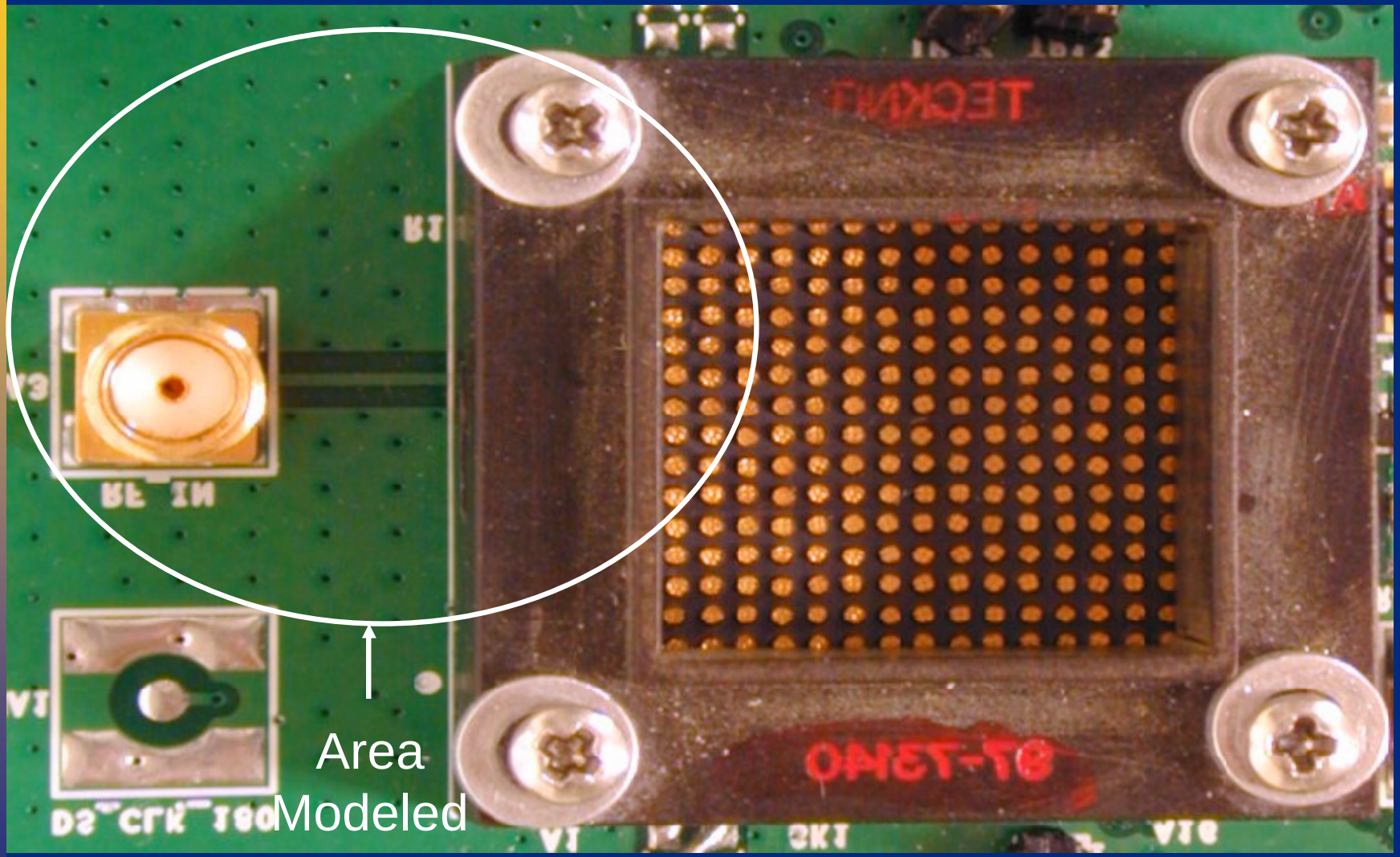
SiP Return Loss at Test Board Input



Test Board



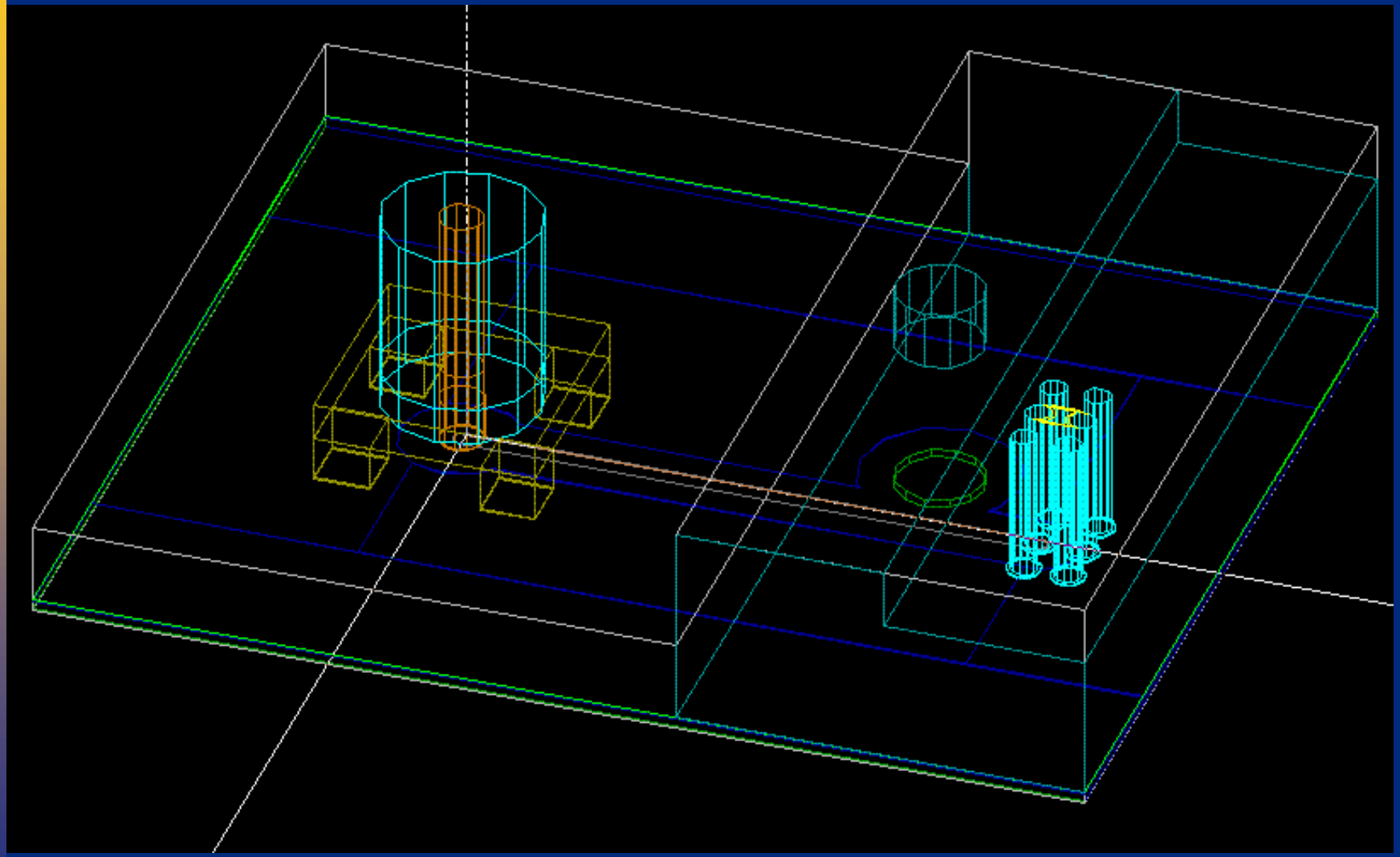
Test Board with Socket Attached



Methodology

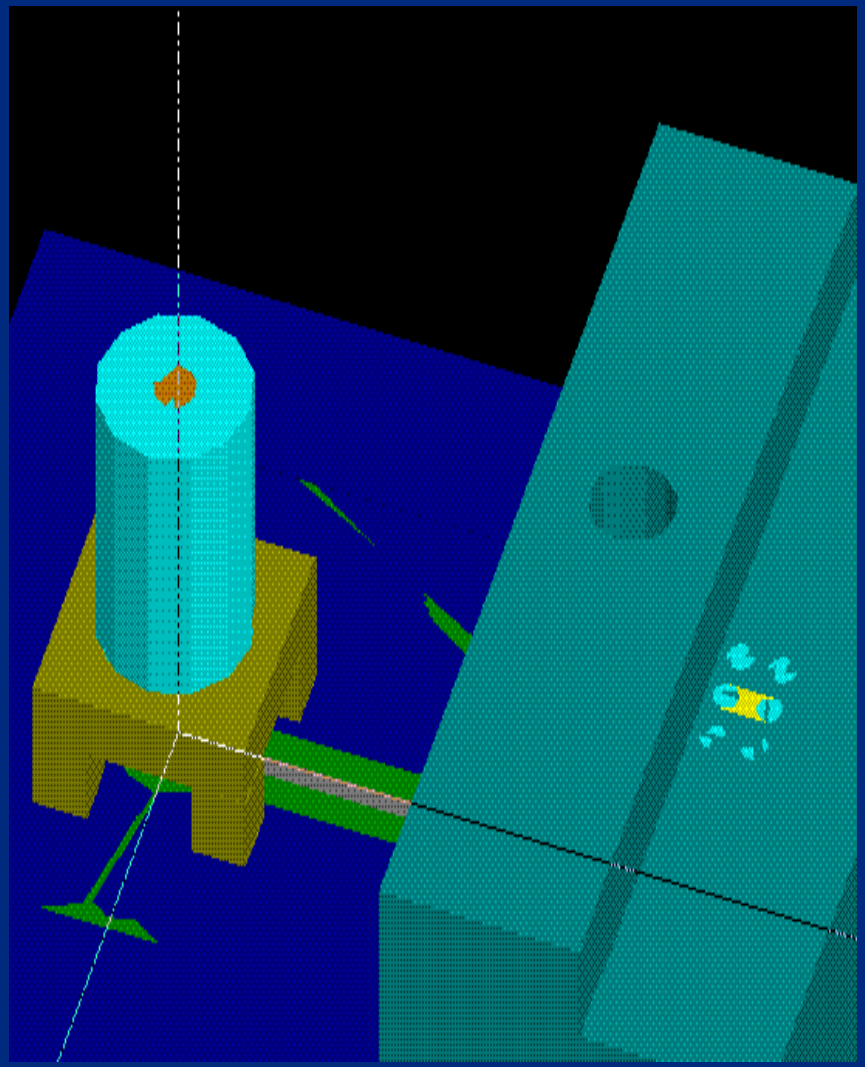
- Module interface cannot be probed
- Test input return loss of the test board & socket under 3 conditions
  - Matched load 50 ohm chip resistor between socket package RF IN and GND contacts
  - Open (no connection) circuit at socket package contacts
  - Shorted wire across socket package RF IN and GND contacts
- Test and modeled input return loss of each test piece
  - Matched, open, and short loads tested separately
  - Modeled the loads to determine their parasitics
  - Isolates performance limitations of the loads from the test board & socket models
- Compare simulated board & socket + cascaded load with measured data

Test Board and Socket HFSS Model



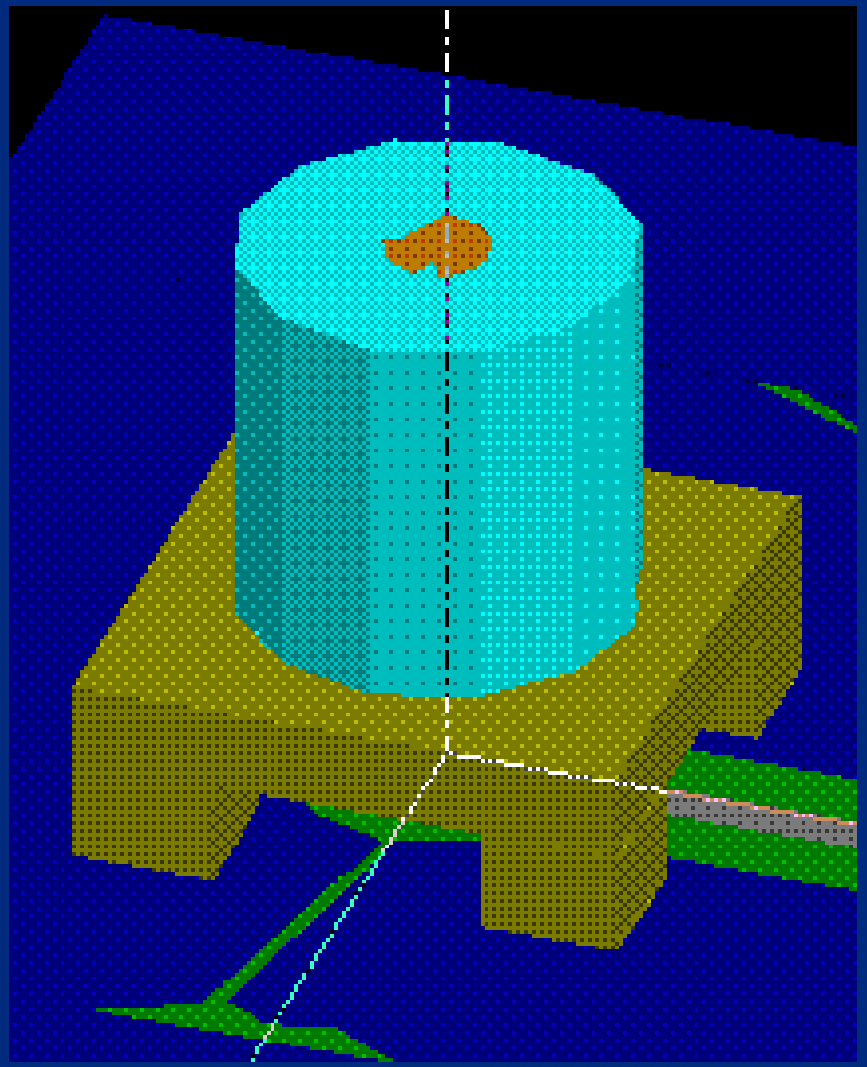
Model Components

- 3 Major Model Pieces
  - Straight Jack Receptacle SMA
  - Horizontal PCB microstrip trace
  - Plastic socket with vertical connectors
  - Air above printed circuit board included!



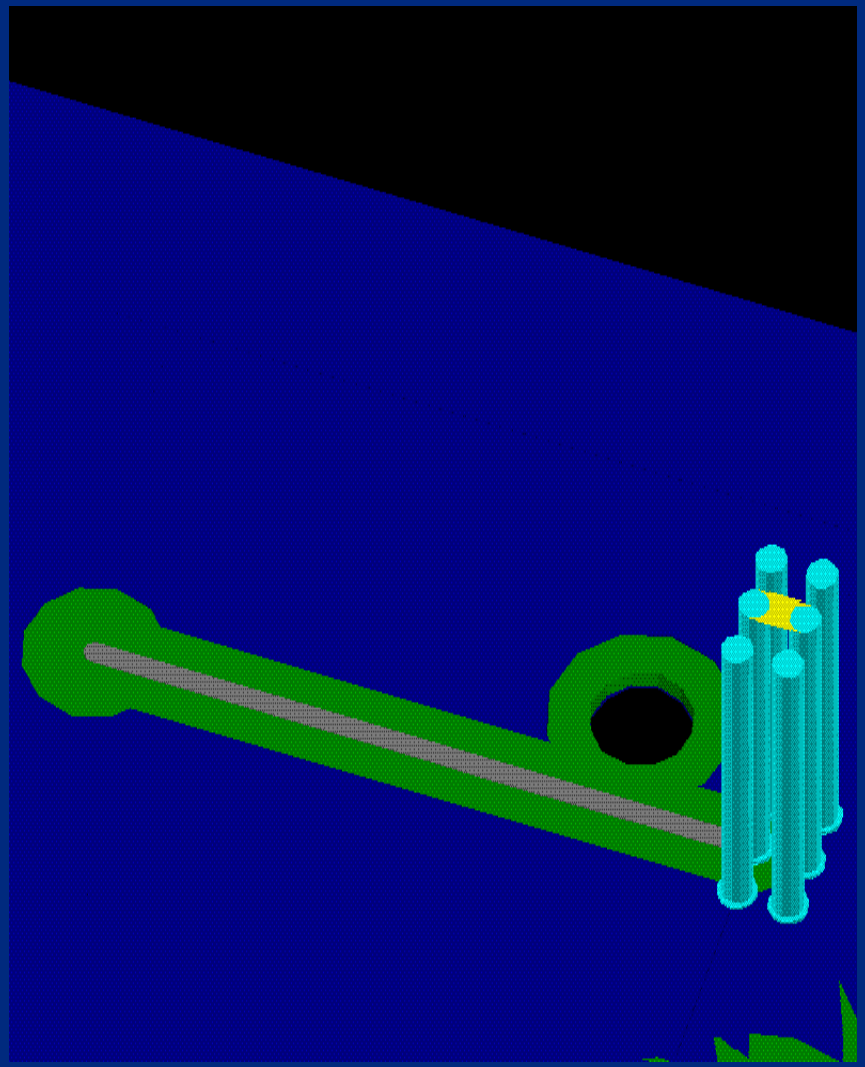
Model Components

- **SMA**
  - **No shell around the coax dielectric for simplicity**
    - **Ground reference provided by external background**
    - **Thanks to Peter Shin**
  - **Dimensions & materials provided on the Johnson Components website**
  - **Wave port input at SMA connector face**
  - **Impedance line defined**



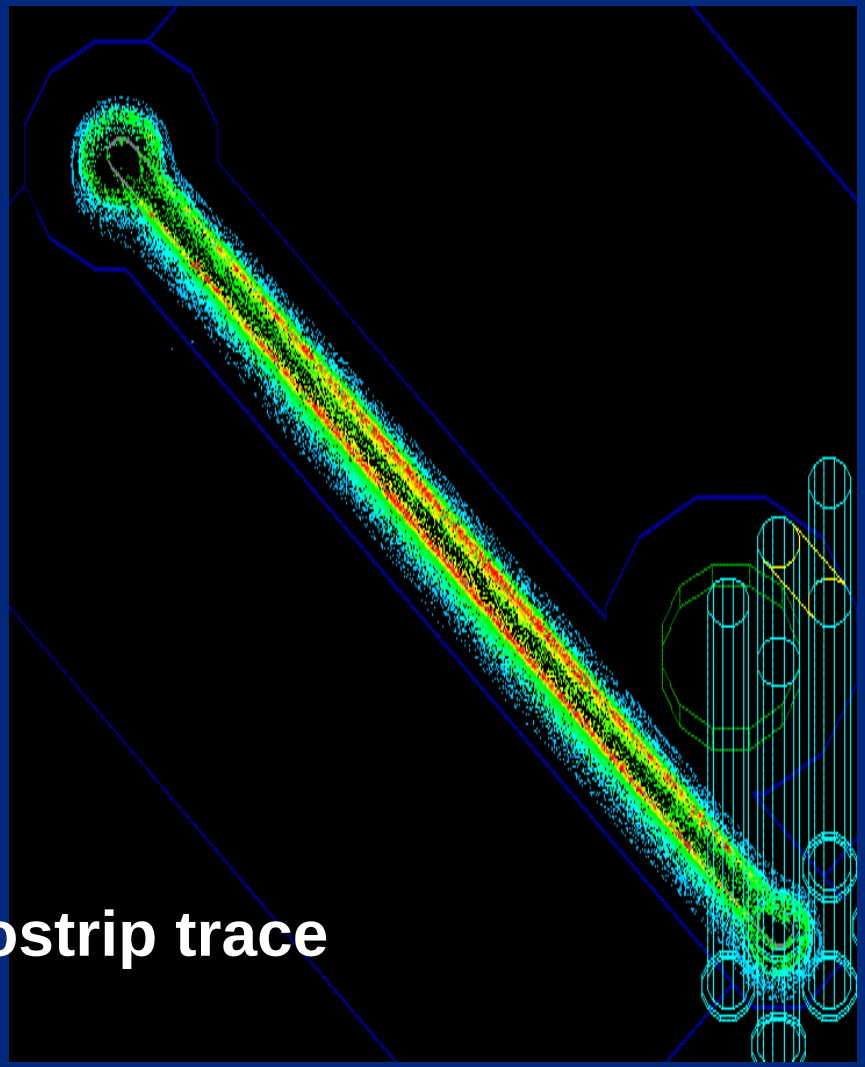
Model Components

- PCB with microstrip trace
  - ½ oz copper top metal trace and ground planes
  - 1 oz copper internal (ground) plane
  - FR-4 board material with 2 mil overcoat
  - Material properties from the DuPont website



Model Components

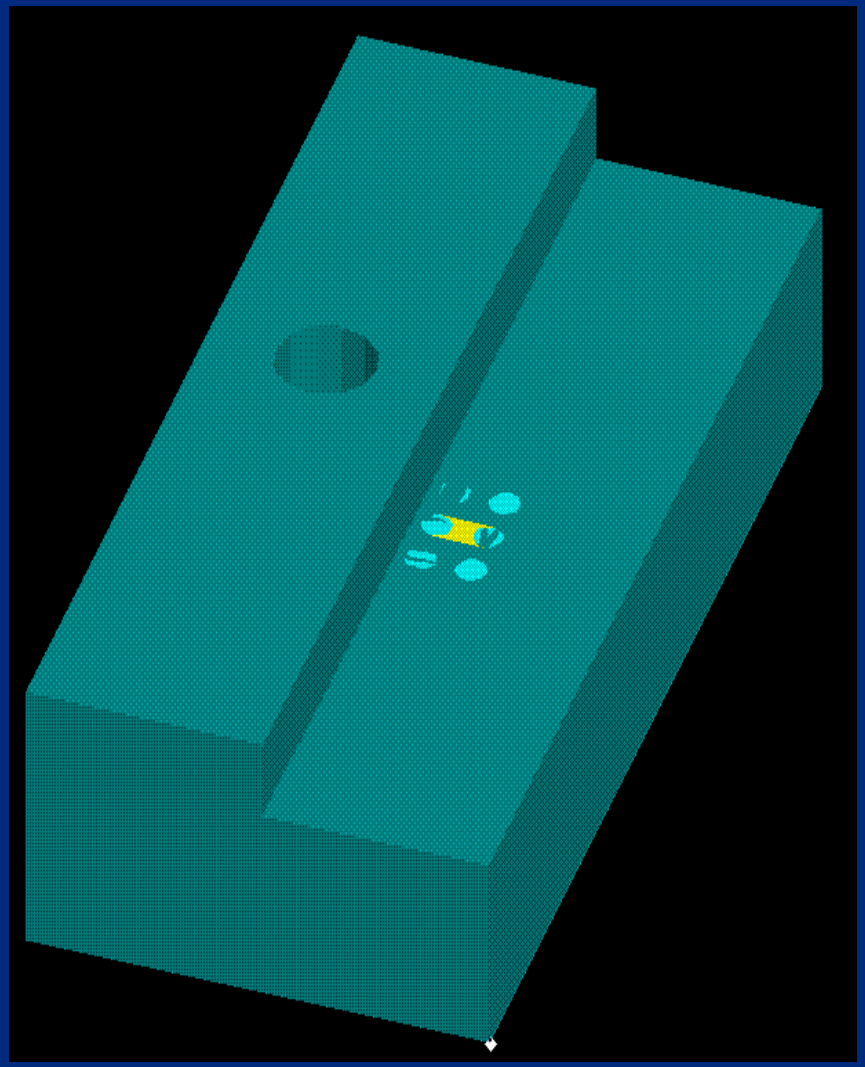
- **PCB with microstrip trace (cont'd)**
  - **Field viewer shows E-field contained between RF IN trace line and the ground plane beneath it**



This is a microstrip trace

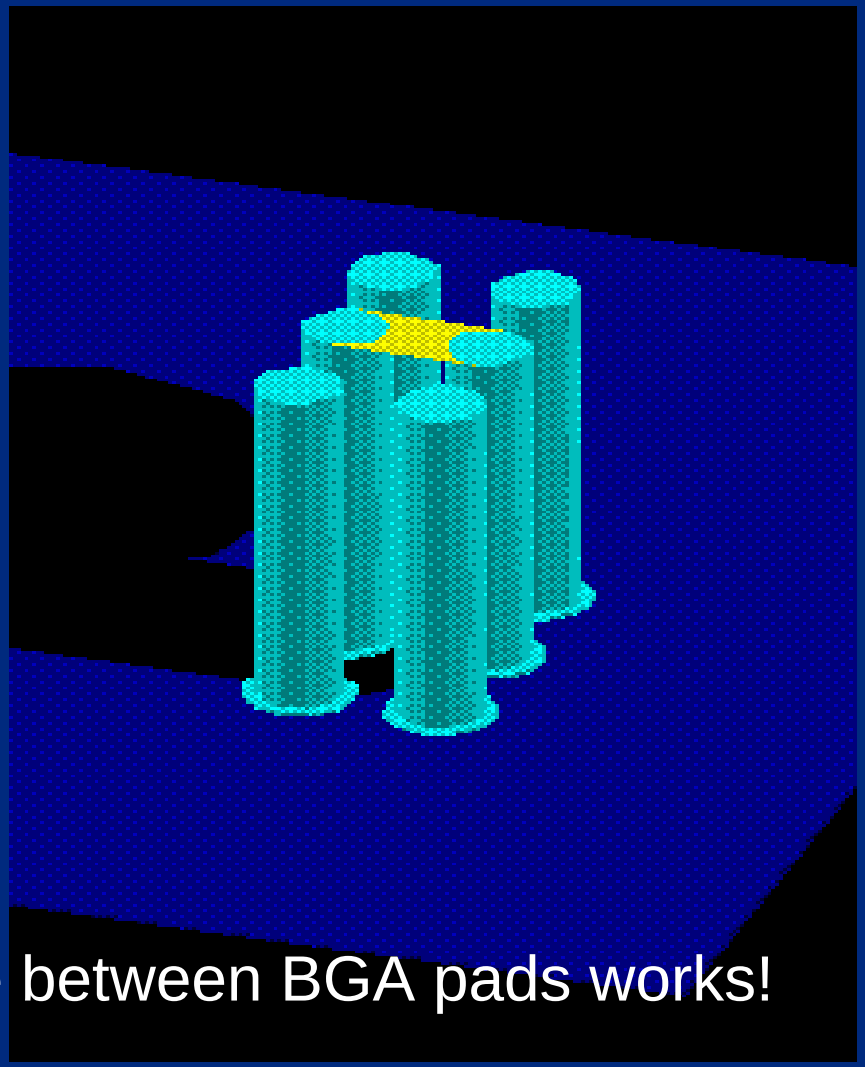
Model Components

- **Socket**
  - **Simplified socket model**
  - **Design includes an RF input trace surrounded by GND BGA pads**
  - **HFSS consistent with manufacturer's model based on measured results**
  - **HFSS representation closely fits our socket application unlike the manufacturer’s generalized model**



Model Components

- **Socket (cont'd)**
  - **Lumped gap source port between RF input pad and a single GND pad sufficient**
  - **Socket ground pads grounded to background through PCB ground – consistent with grounding scheme in test (with board ground tied to earth ground)**
  - **Ground bounce and other issues should be considered in design**

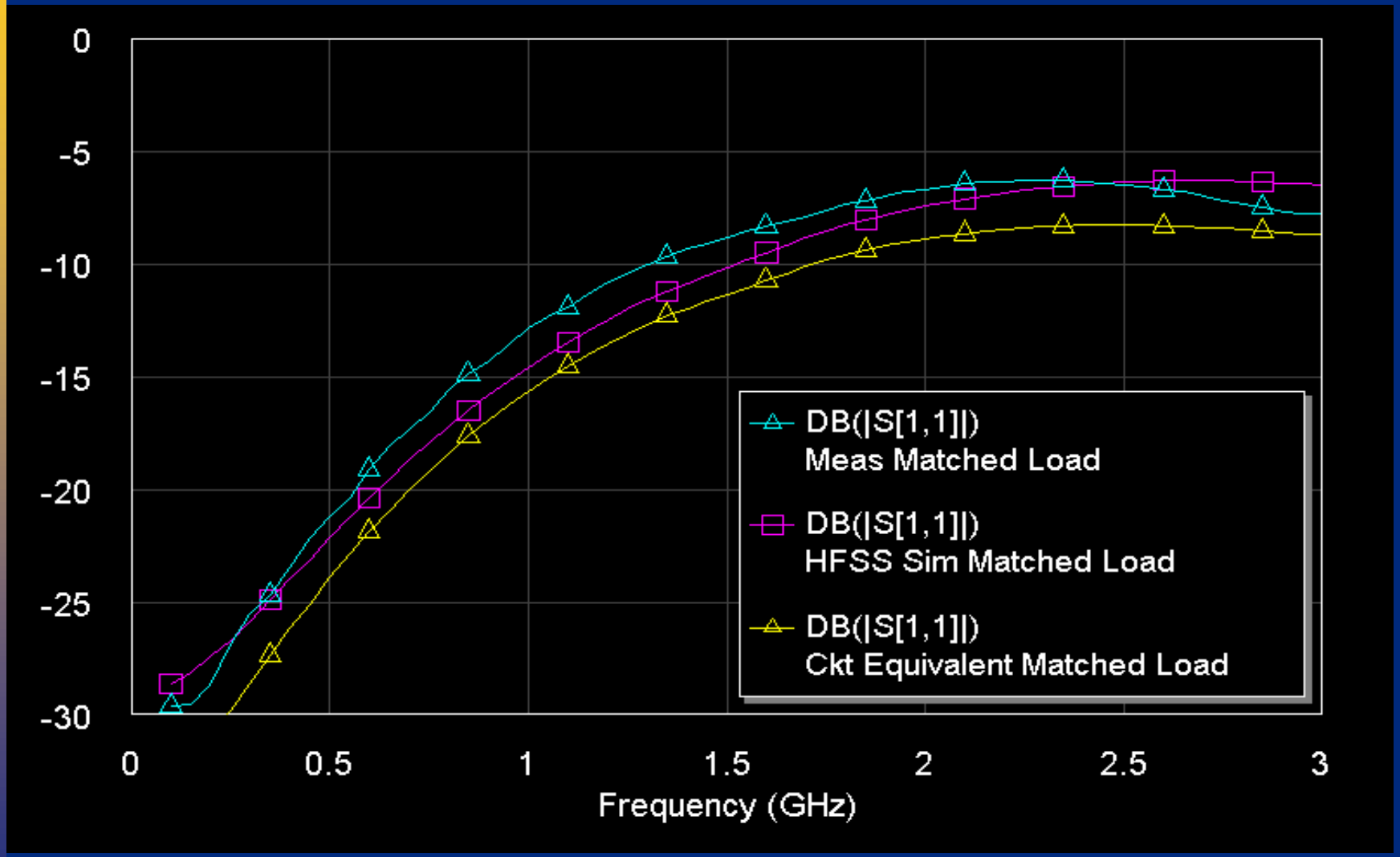


Simple lumped gap source between BGA pads works!

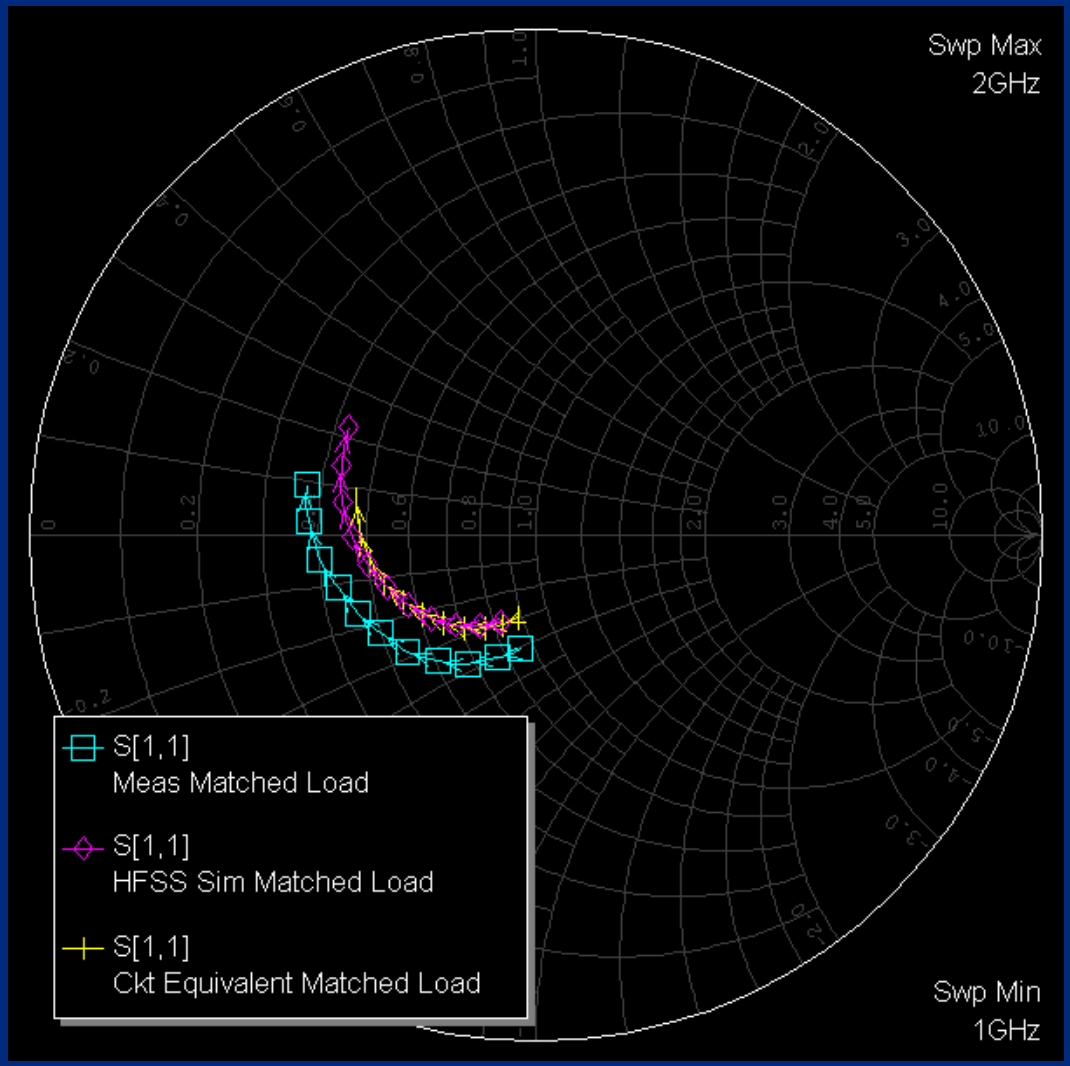
Measurements

- Matched, open, and short load at package interface
- 50 ohm chip resistor contacting the RF input and a ground connection with pressure applied by a pencil eraser
- Open air isolation
- Short circuit with a thin gauge wire
- Input return loss measured at SMA

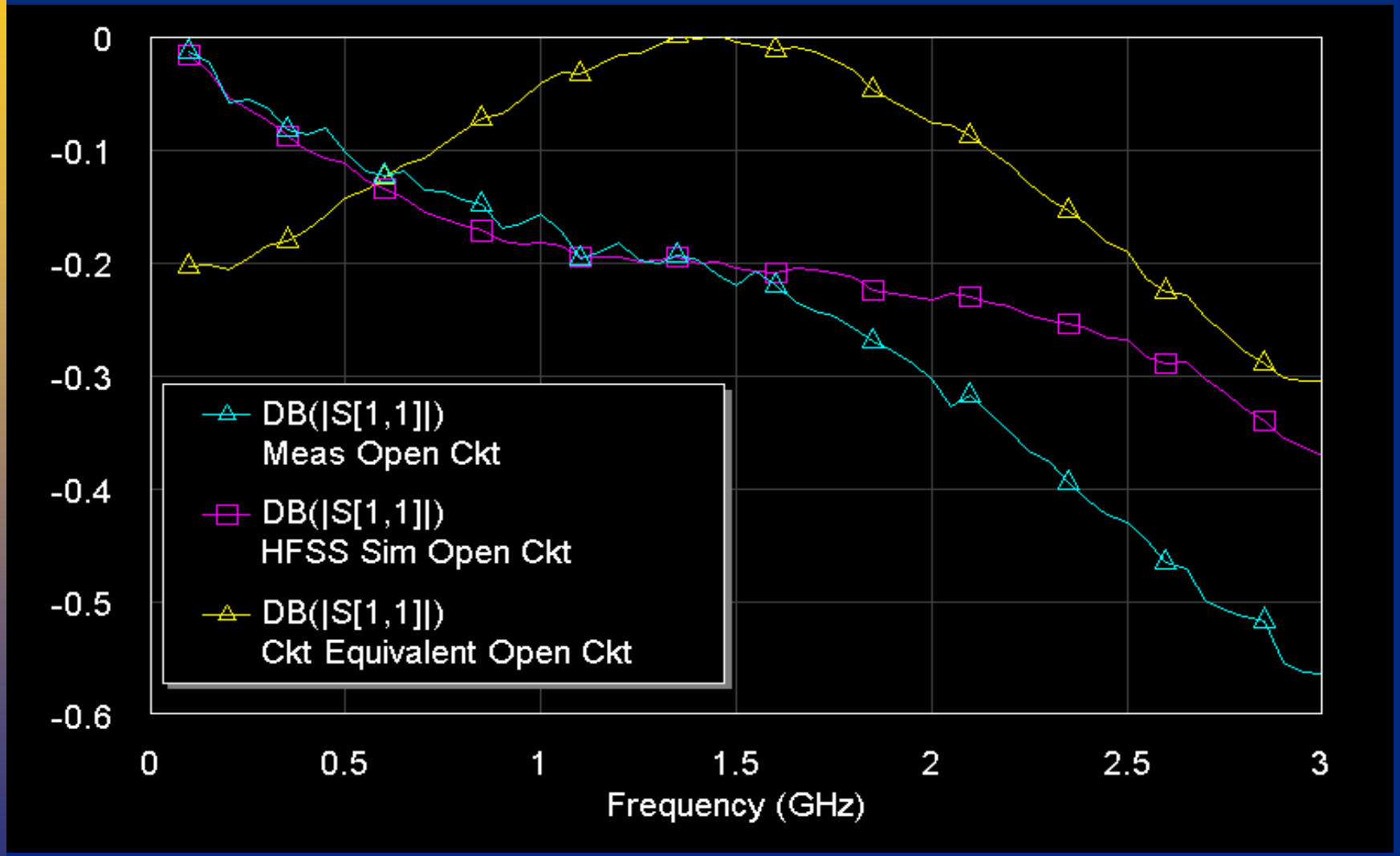
Return Loss for Matched Load – Meas v. Model



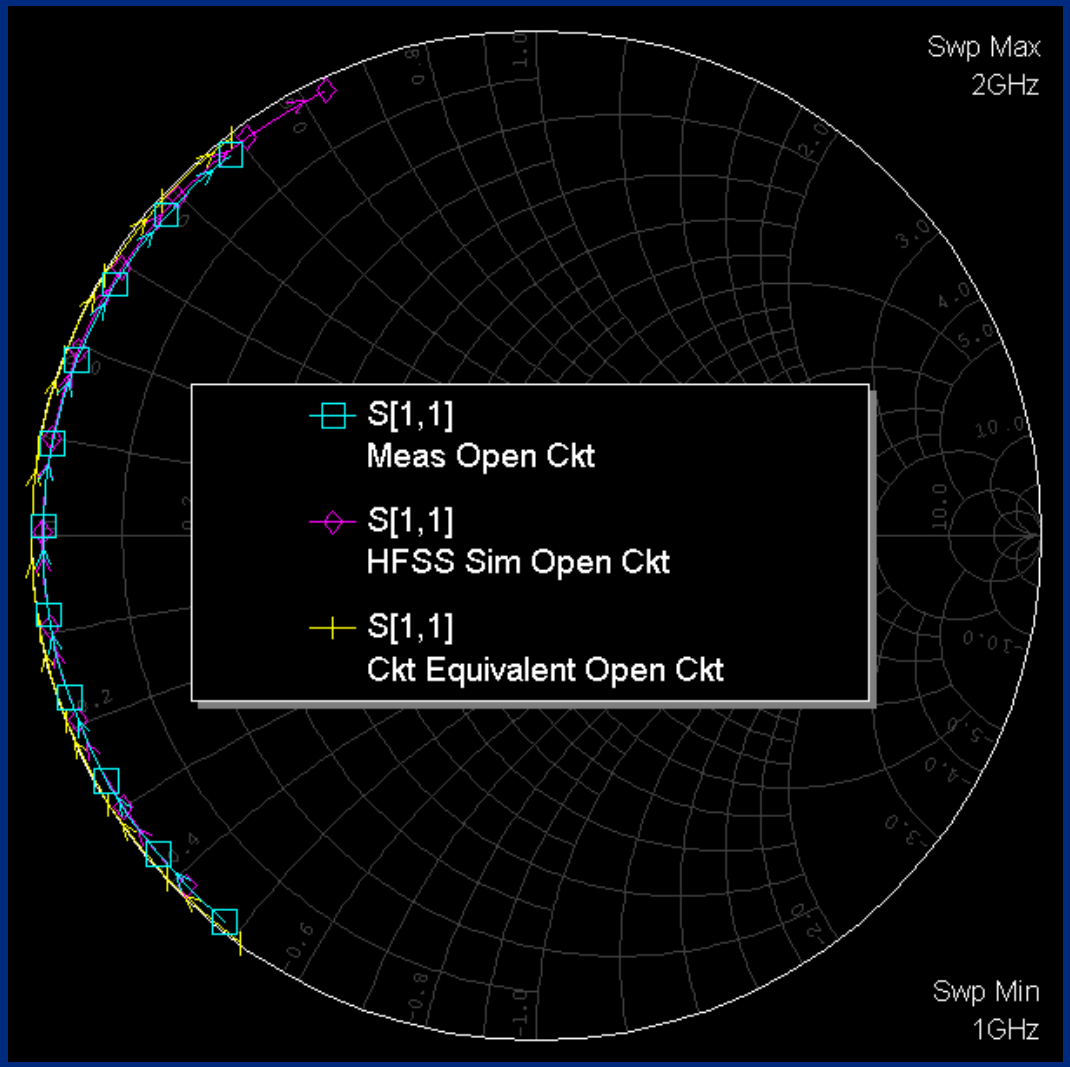
Return Loss for Matched Load – Meas v. Model



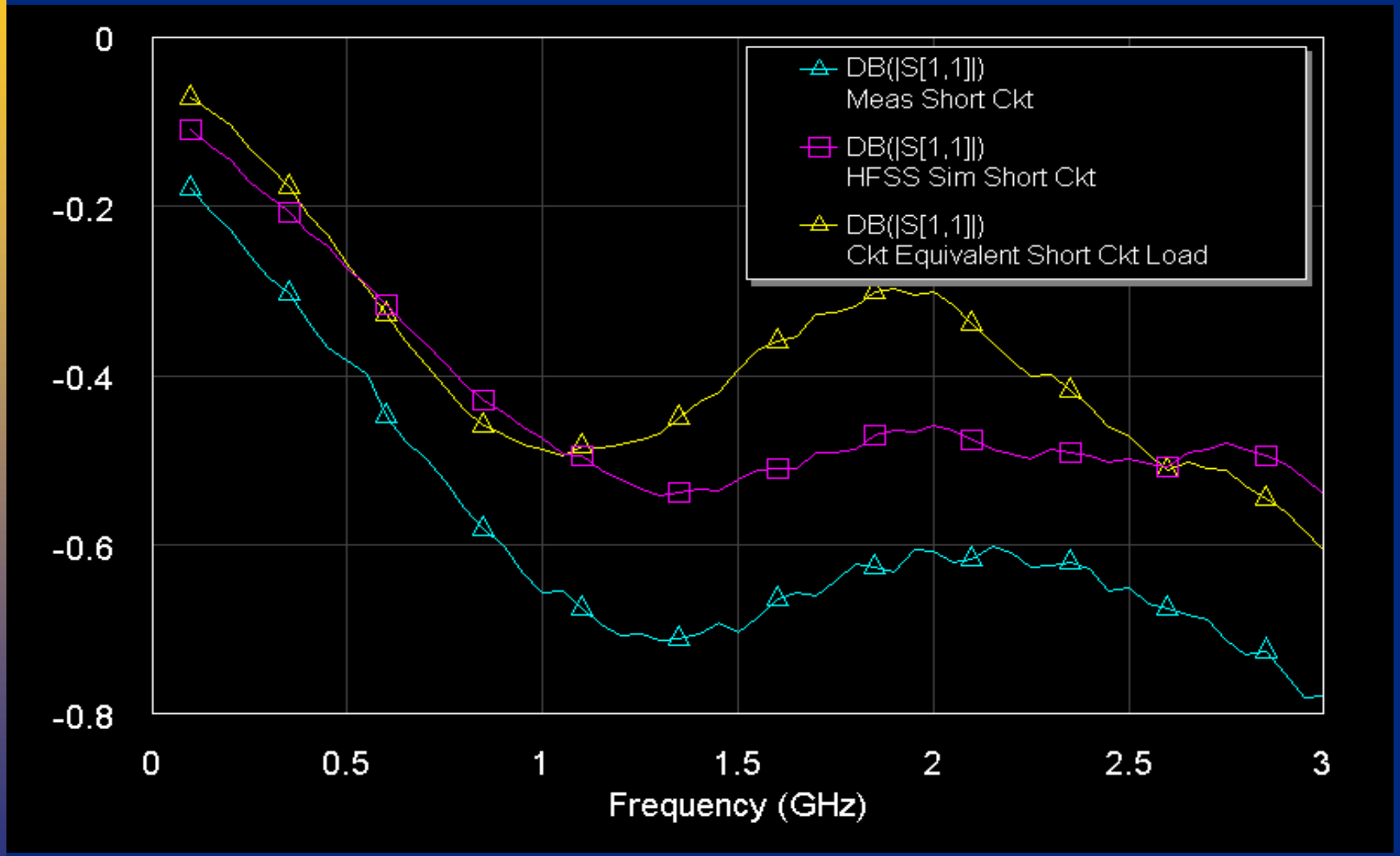
Return Loss for Open Circuit Load – Meas v. Model



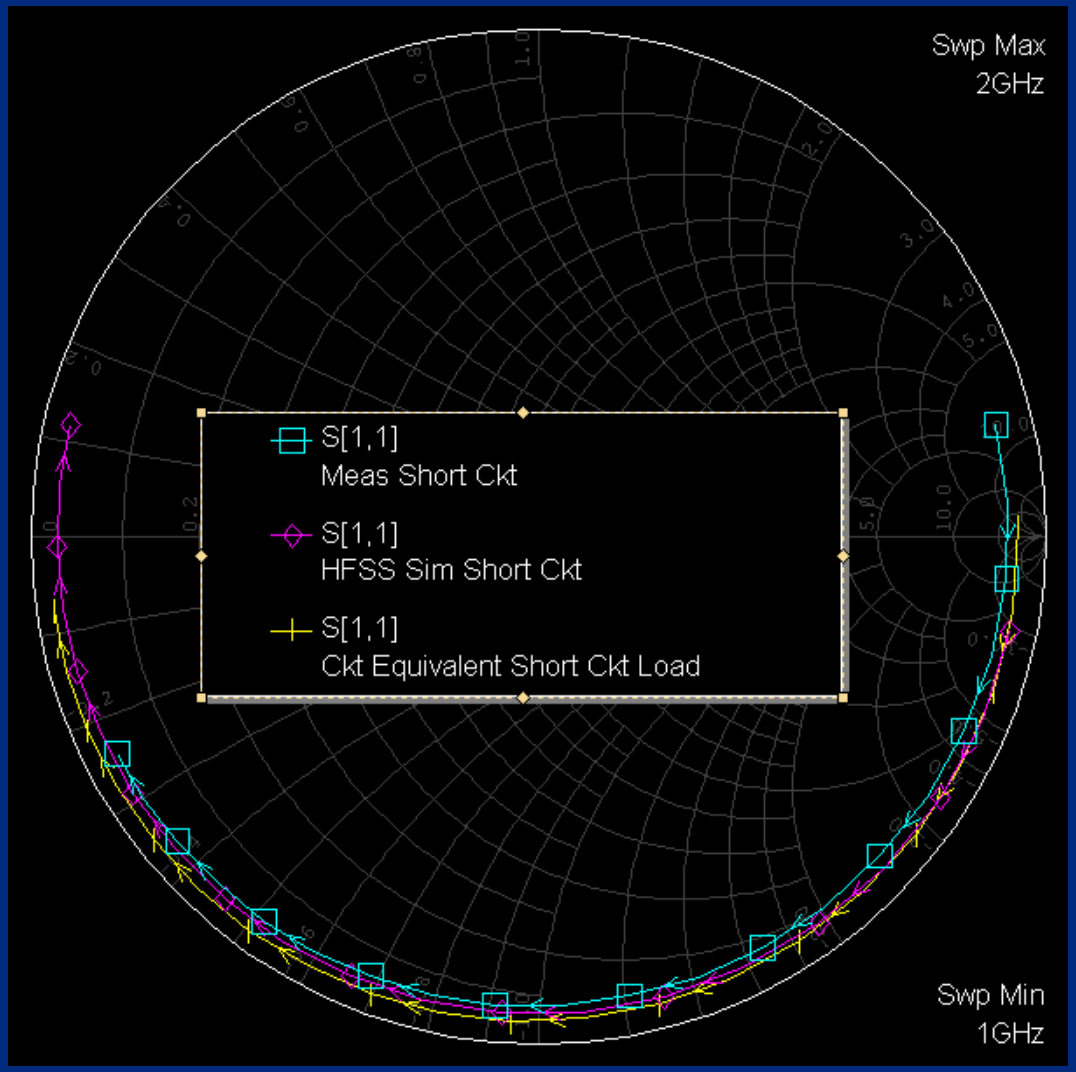
Return Loss for Open Circuit Load – Meas v. Model



Return Loss for Short Circuit Load – Meas v. Model



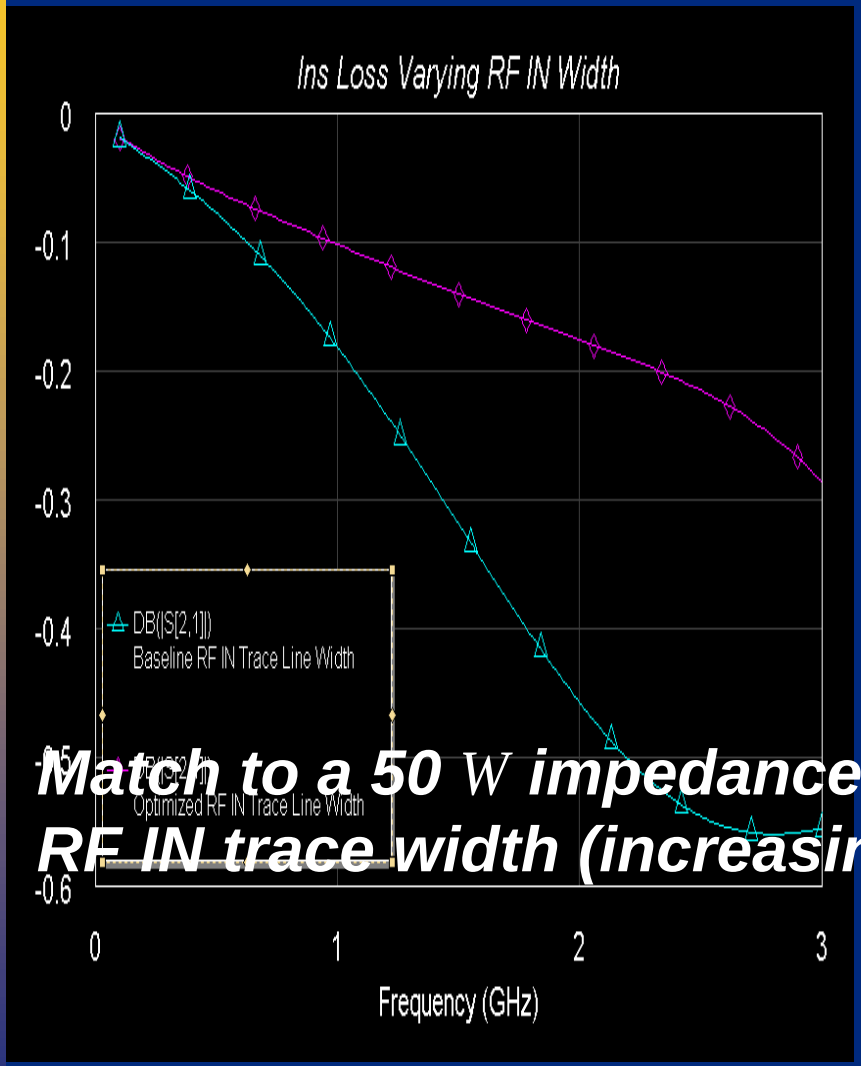
Return Loss for Short Circuit Load – Meas v. Model

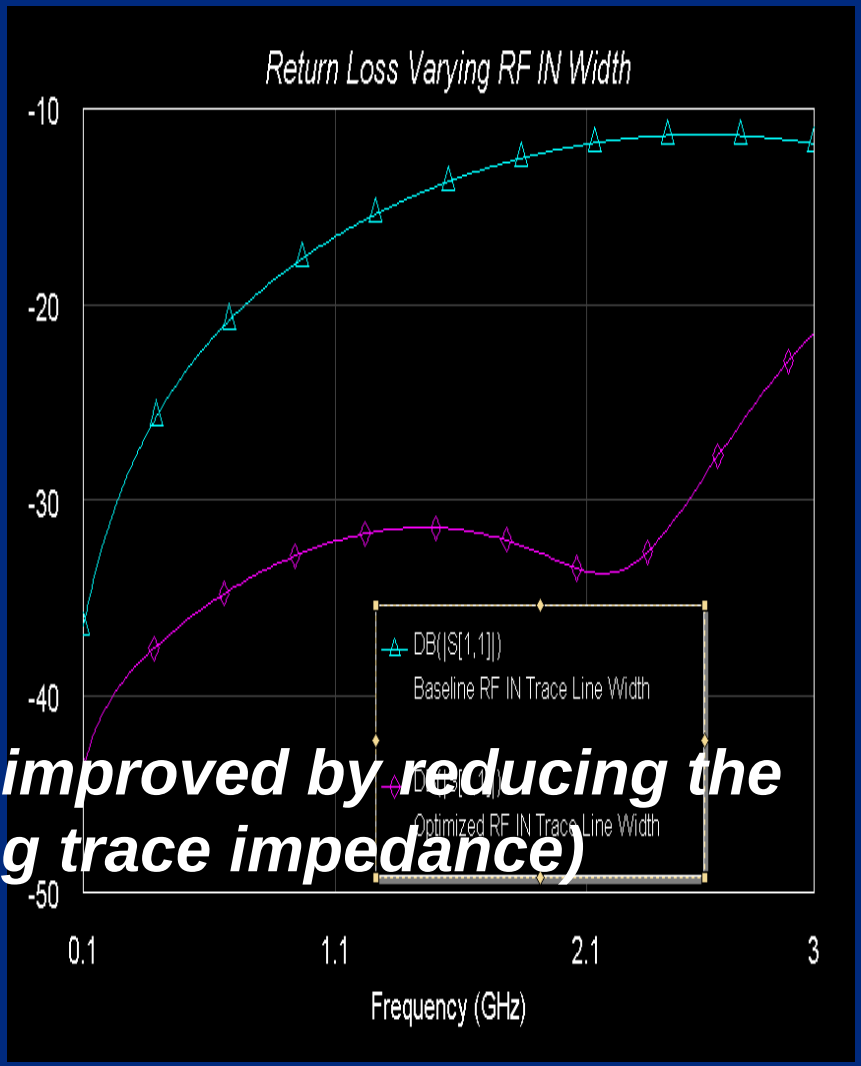


Issues

- **Board impedance in design**
  - **Board and socket provide an imperfect match to 50 Ω load**
  - **Simple board RF IN trace width change recommended based on HFSS analysis**
- **Phase error in simulation needs to be improved**

Board Improvement





Match to a 50 W impedance improved by reducing the RF IN trace width (increasing trace impedance)

Conclusion

- Model of test board & socket presented
- Lumped element equivalent circuit failed
  - Air interface below SMA never considered
  - Inadequate model of the socket pins from the manufacturer's generalized circuit equivalent
  - Failure to account for impact of socket material above the RF trace on the trace impedance
  - No socket pin-board trace coupling considered
- HFSS-based simulation provides good model
  - Improves SiP modeling effort
  - Lower cost and less time to develop than a calibration substrate
  - Good agreement between measured and model data when evaluating Ditrans' product module packaging
  - Basic geometry used to evaluate customer reference board and set future module interface

Questions?