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# Examples of HFSS Modeling for High Speed IC Design

Weimin Sun, PhD  
Vitesse Semiconductor

**HFSS 2003 User Workshop**  
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making **connections**  
better and faster



## Outlines

### I) Interconnect Models

- RLC Lumped
- Full-wave (S-parameter based)
- Full-wave (Hspice G & F elements)

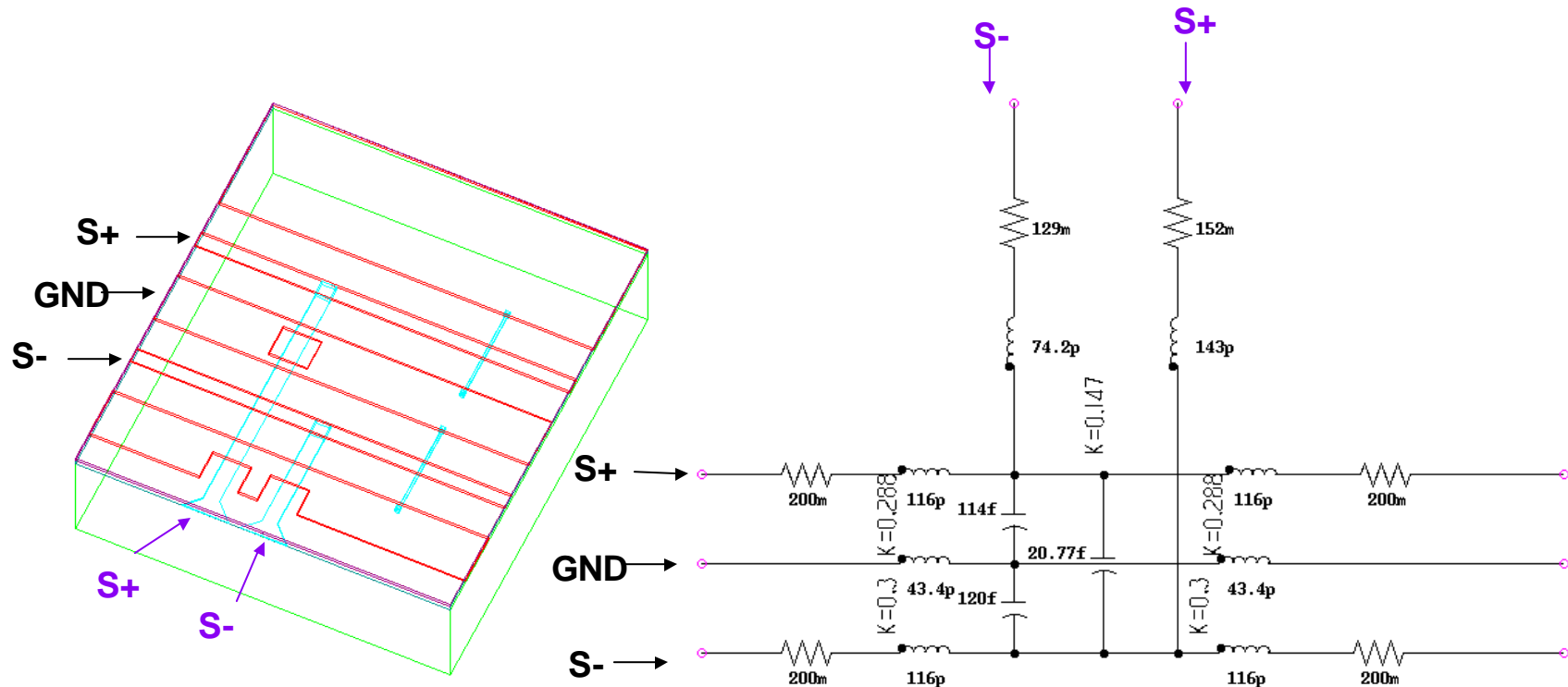
### II) HFSS Modeling Examples

- On-Die 40G Transmission Lines
- DA Stage to Stage Interconnects
- A FcMLF Package
- A BGA Package High Speed Channel
- On-Wafer Probe Calibration Elements
- A 10G Optical and Electrical Module

# Interconnect Models -- RLC Lumped

## RLC Model

- **Simple, easy and efficient**
- **Mutual coupling handling could be very tedious as pin number grows**
- **Not accurate for high speed rate (LC cut-off)**
- **Can't account dispersive loss ( skin-depth loss and loss tangent)**



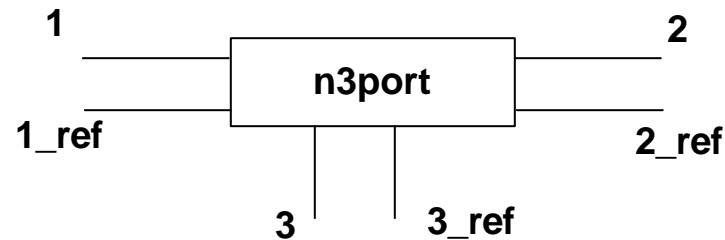
# Interconnect Models -- Full-Wave Model (S-Parameter Based)

## Full wave (S-parameter file based) Model

- *Accurate*
- *Time consuming (modeling and simulation)*
- *Difficult to connect active device to net inside*

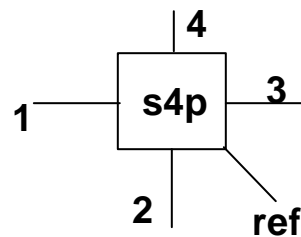
Spectre: **nport** instance -- S parameter file based net ( similar to \*.nmf format)

- Define CDF first



ADS: **SnP** element -- S, Y or Z-parameter file based net (touchstone format)

- Common port ref
- S, Y or Z

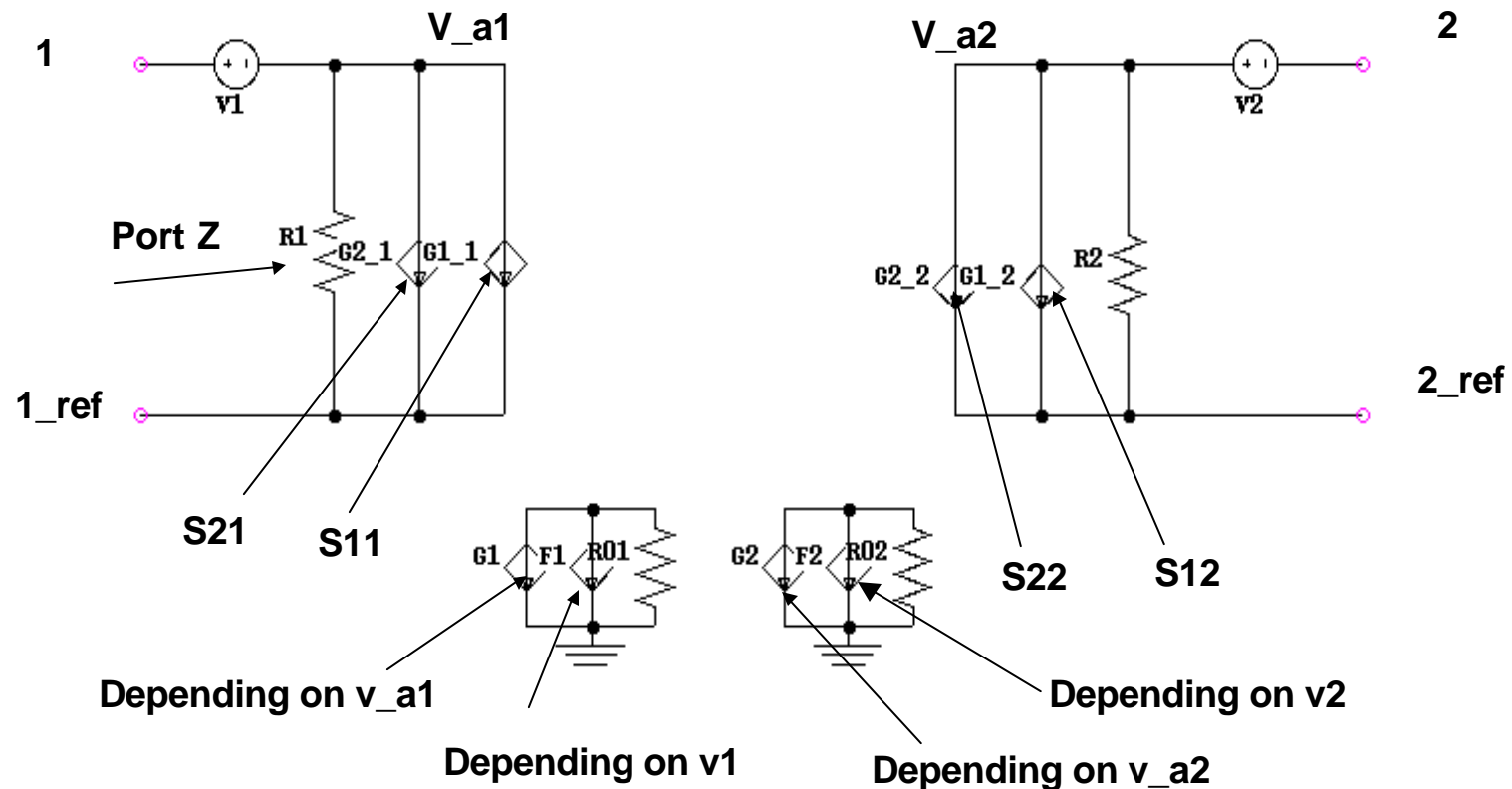


Maxwell Spice: **Full-wave N-port**

# Interconnect Models -- Full-Wave Model (Hspice G & F)

Hspice: **G & F** elements -- Frequency tabulated G, F elements net

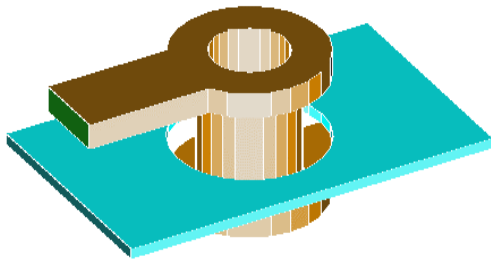
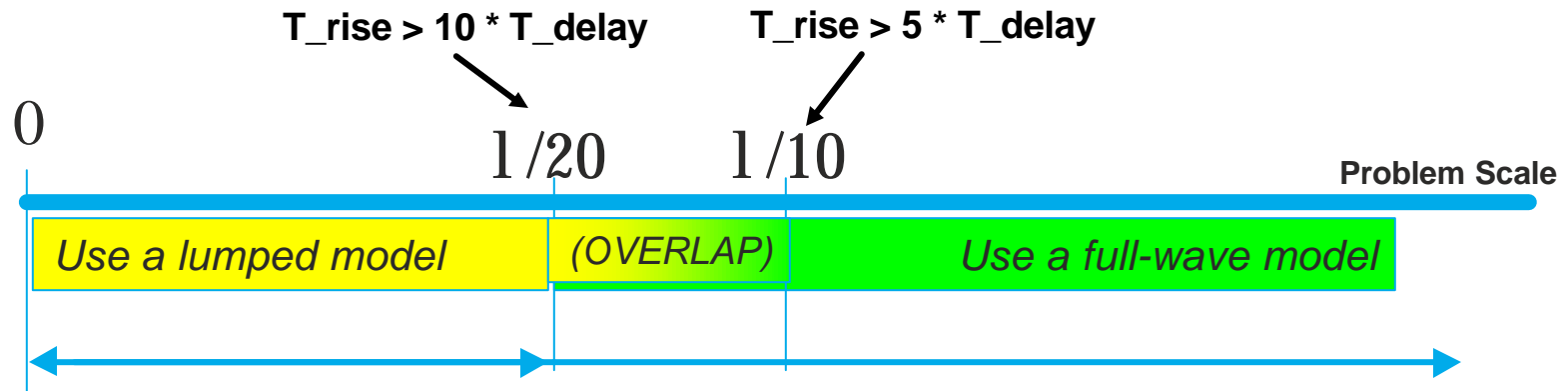
- *Subcircuit netlist accounts for loss and coupling*
- *Nesty for more than 2 ports*
- *May experience problem for transient analysis*



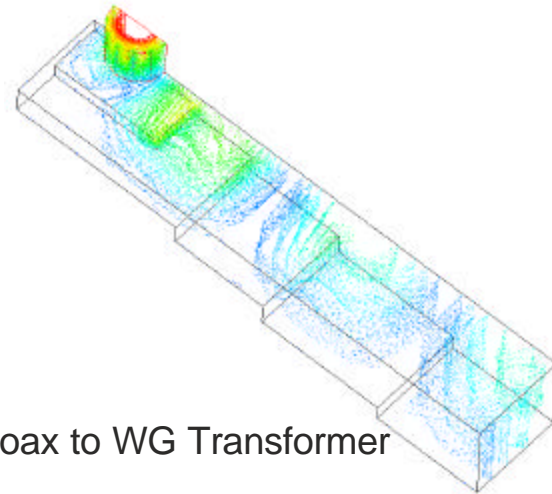
# Interconnect Models -- When to Use Lumped or Full-wave

## Rule of Thumb

$$BW = (0.35 \sim 0.5) * T_{rise}$$



Example: Finding Signal Integrity impacts of a Via in the signal path



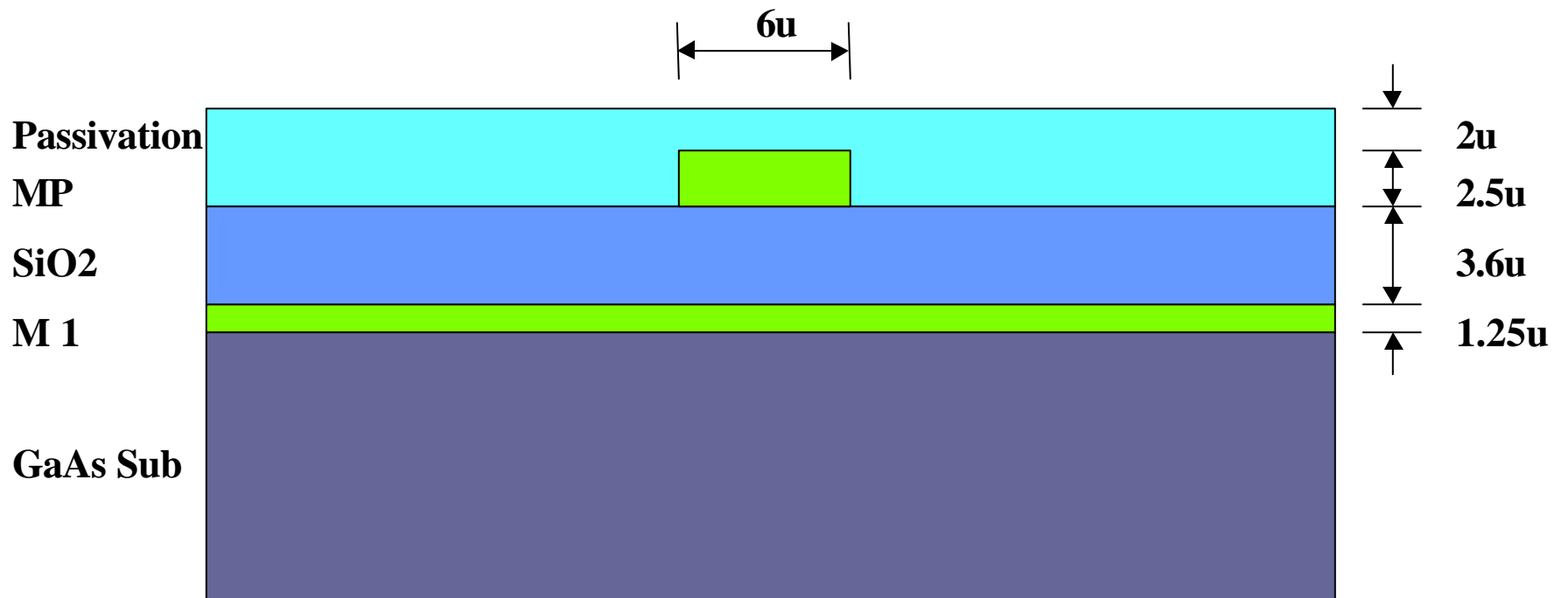
Example: Coax to WG Transformer

## II) HFSS Modeling Examples

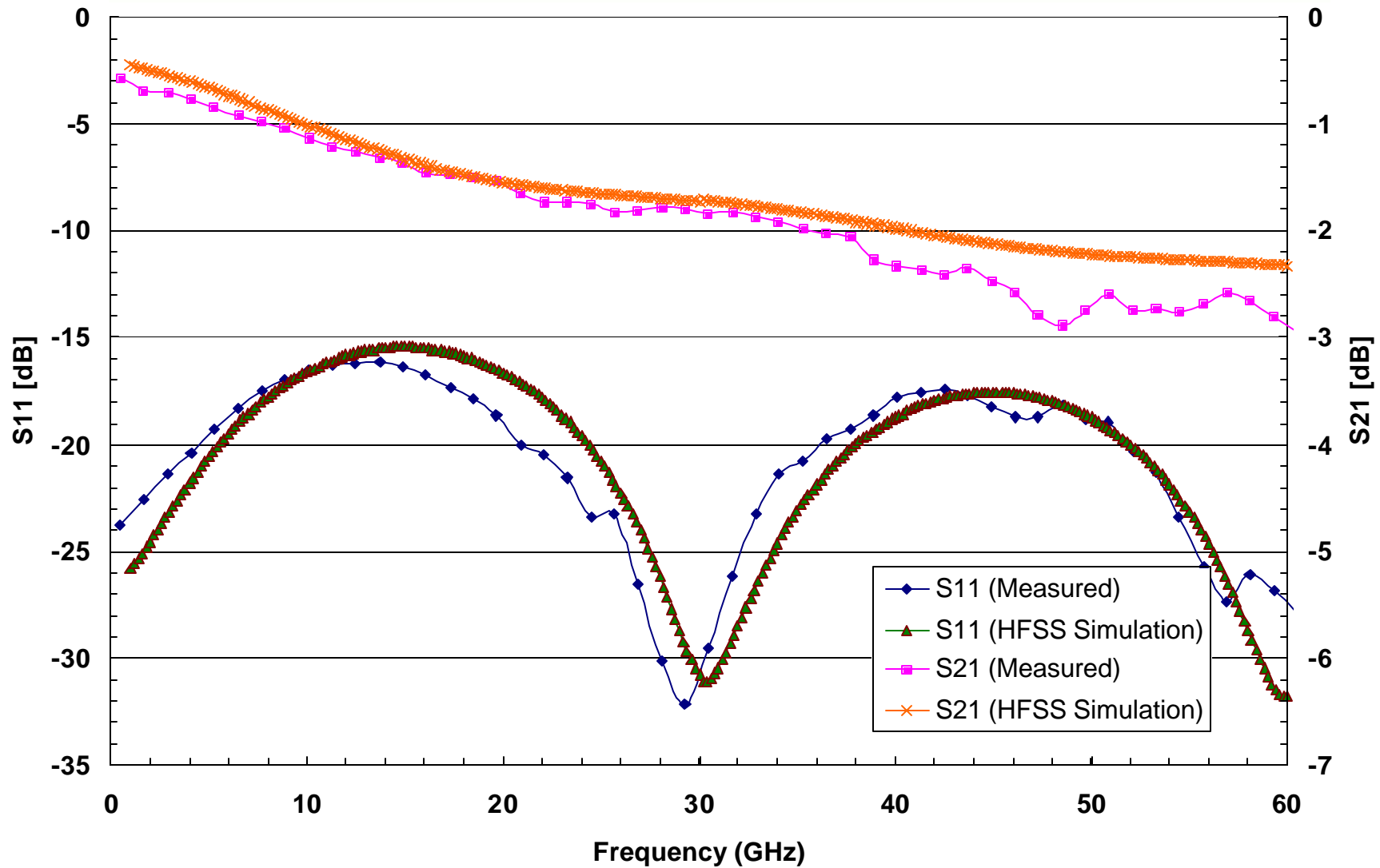
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# HFSS Modeling Examples -- 40G Microstrip line design (2.5mm long)

## Vitesse 40G Microstrip Line Design

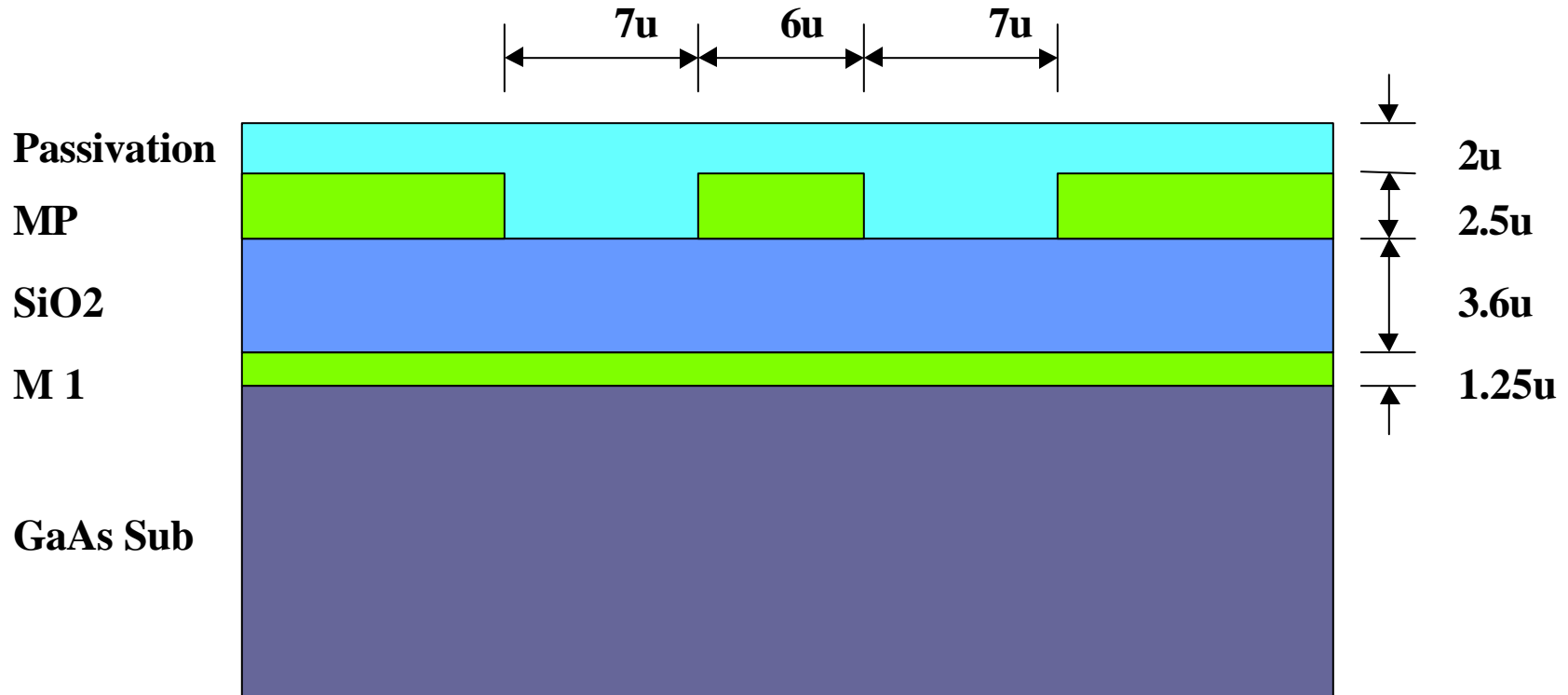


# HFSS Modeling Examples -- 40G Microstrip line design (2.5mm long)

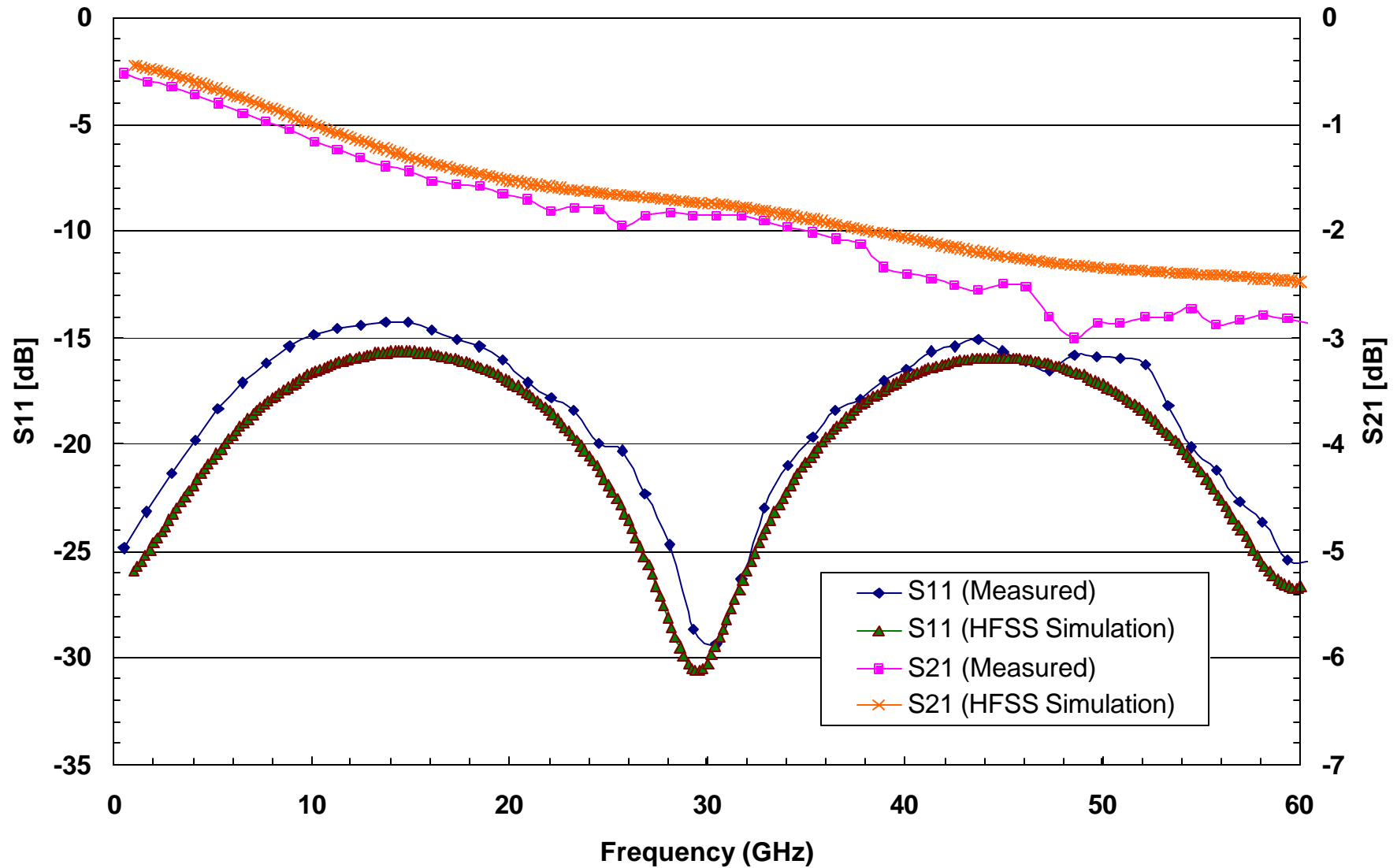


# HFSS Modeling Examples -- 40G CPW line design (2.5mm long)

## Vitesse 40G Coplanar Waveguide (CPW) Design



# HFSS Modeling Examples -- 40G CPW line design (2.5mm long)



## II) HFSS Modeling Examples

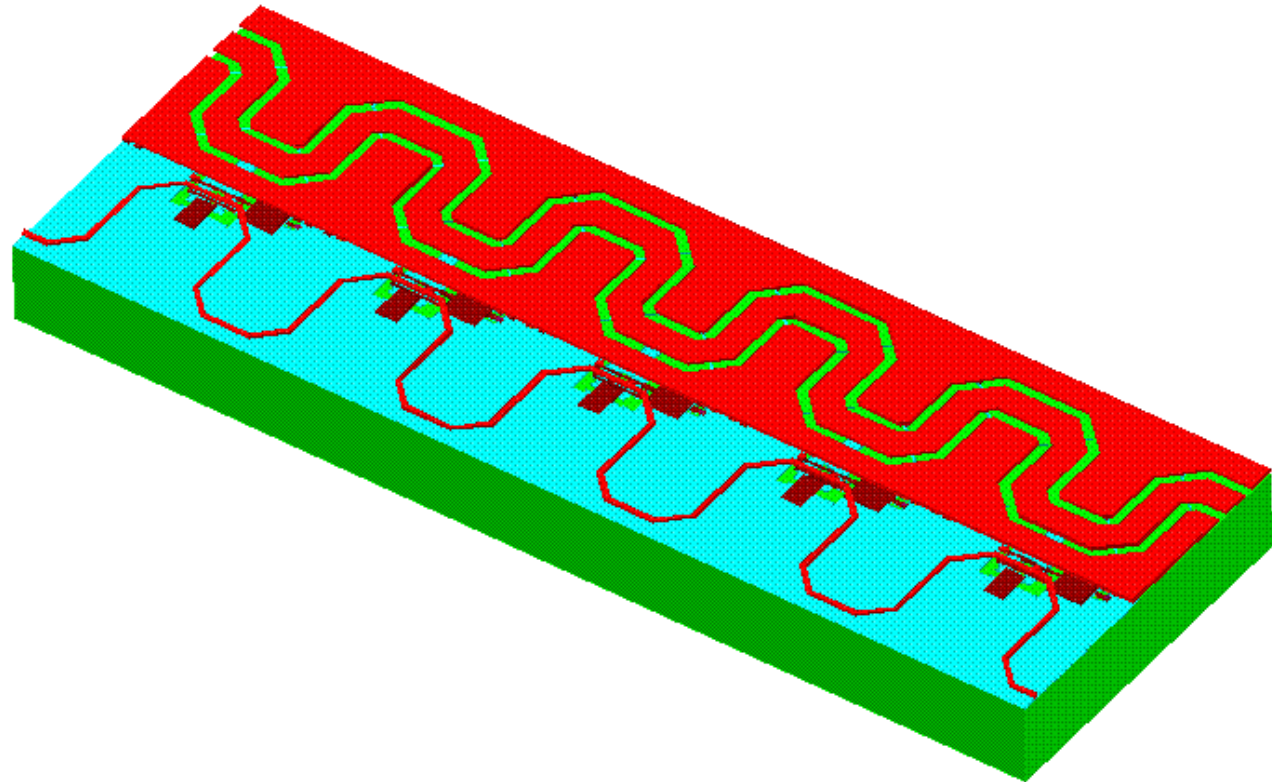
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# HFSS Modeling Examples -- DA Interconnects

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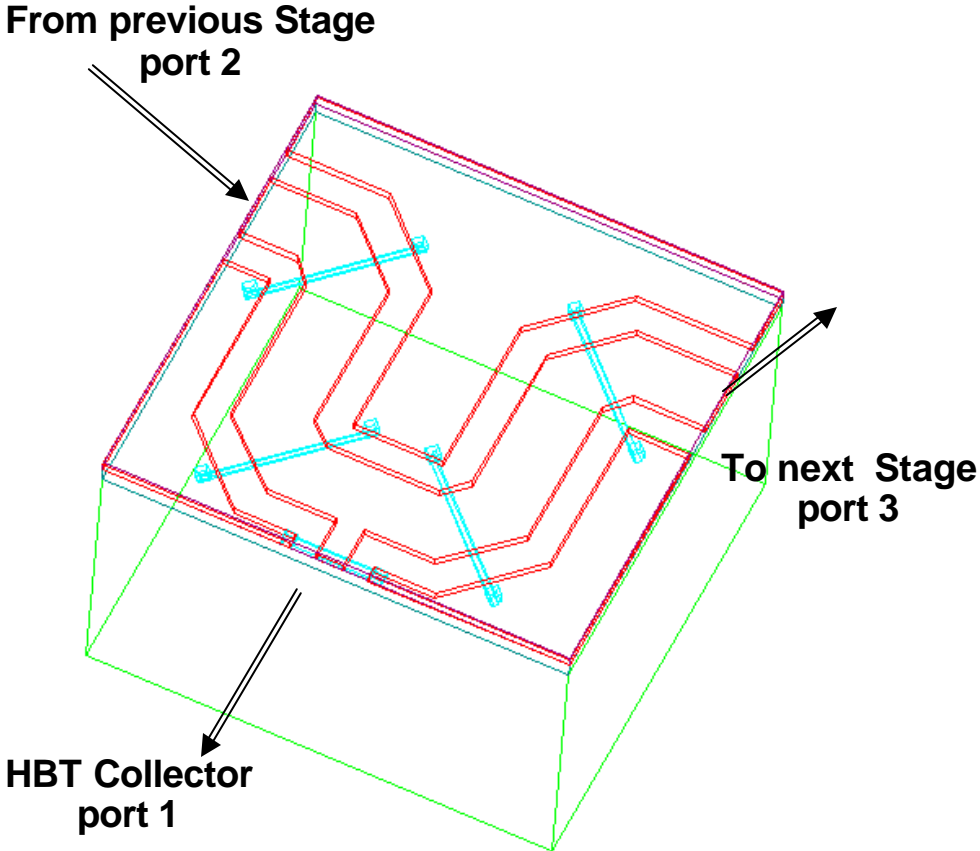
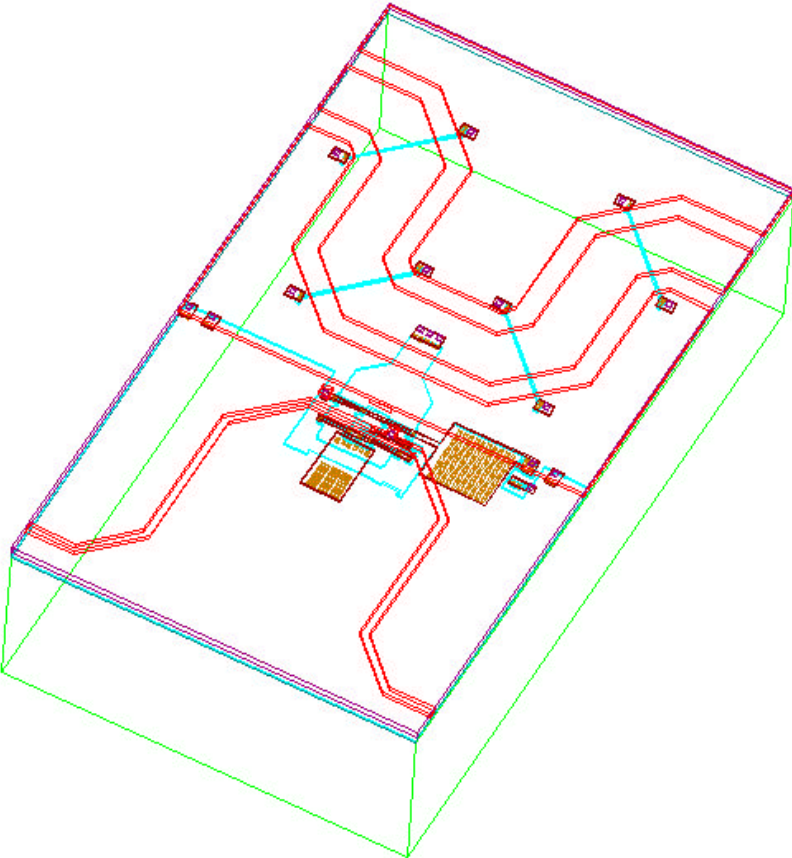
## A 5 Stage 40G Distributed Amplifier

- Interconnect Loss and Matching Characteristics
- Bandwidth
- $t_{\text{rise}}$  degradation
- Scattering fields by Caps



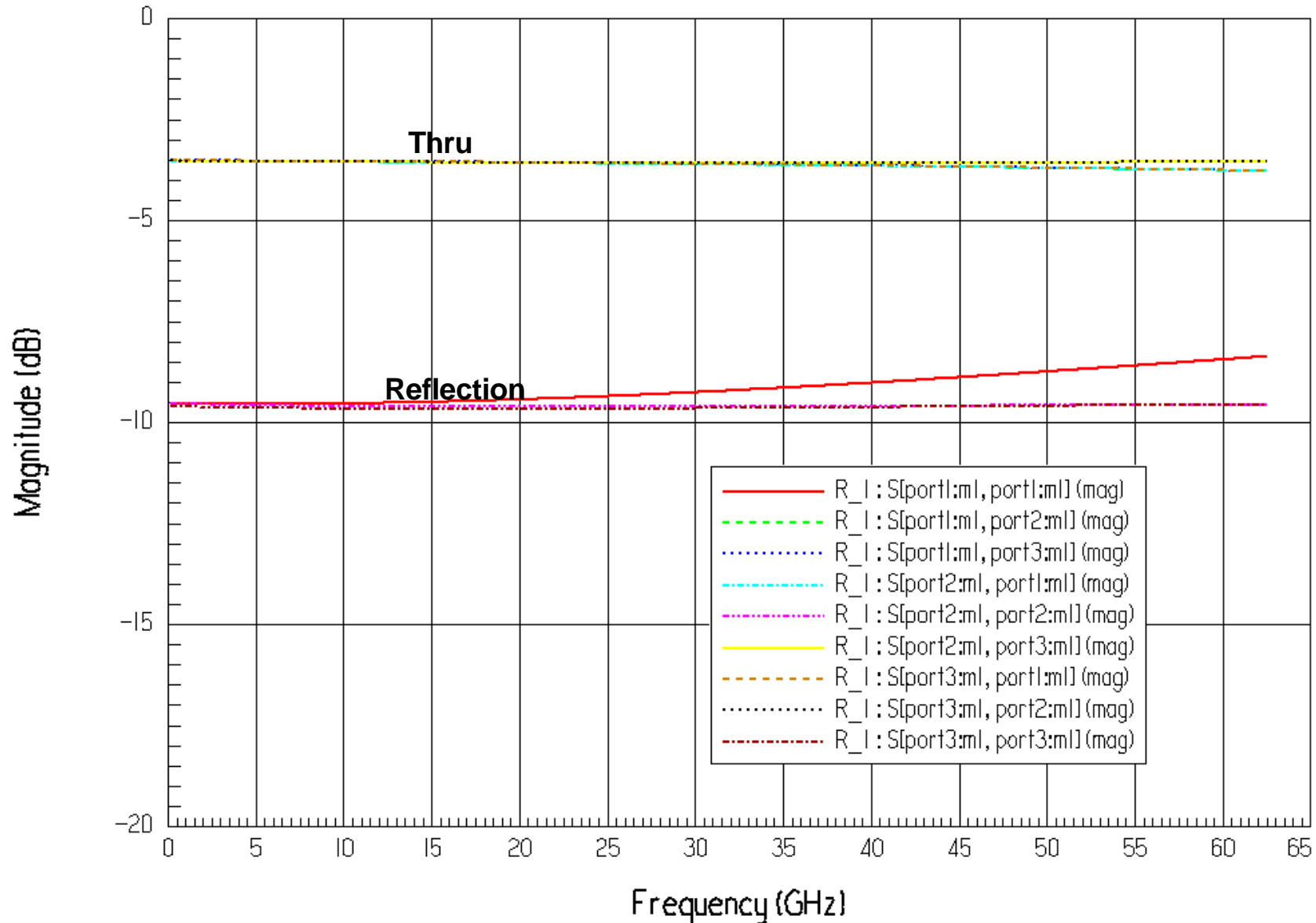
# HFSS Modeling Examples -- DA Interconnects

Modeling Single Stage of either or both  
**In** and **Out** Interconnect



# HFSS Modeling Examples -- DA Interconnects

## Output Stage to Stage Interconnect Characteristics

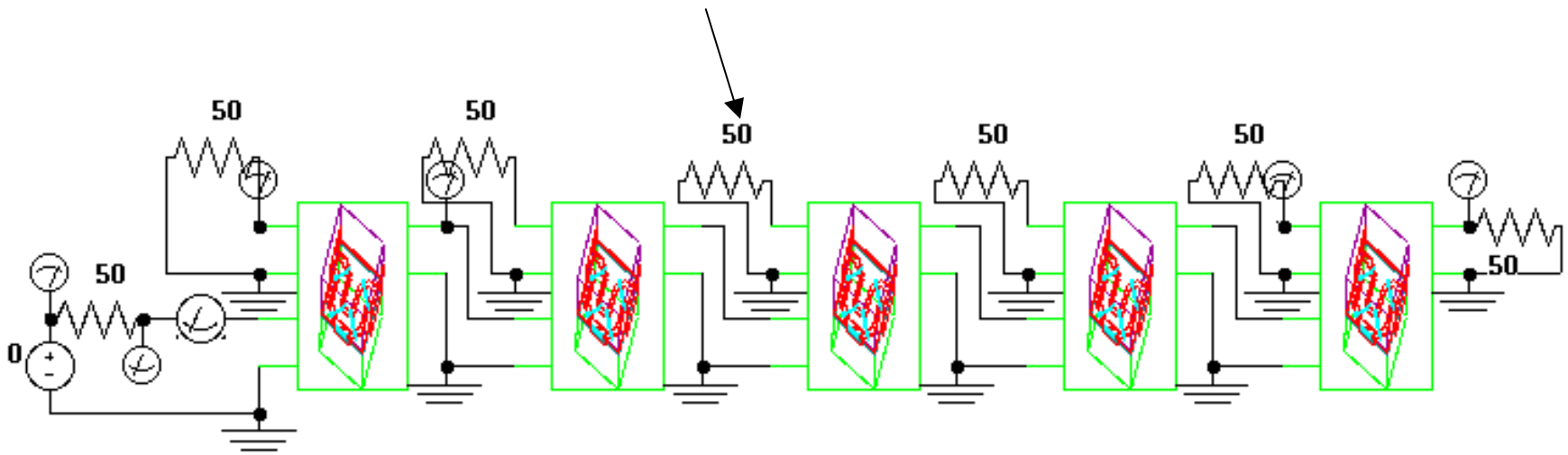


# HFSS Modeling Examples -- DA Interconnects

## Schematic of 5-cascaded interconnects

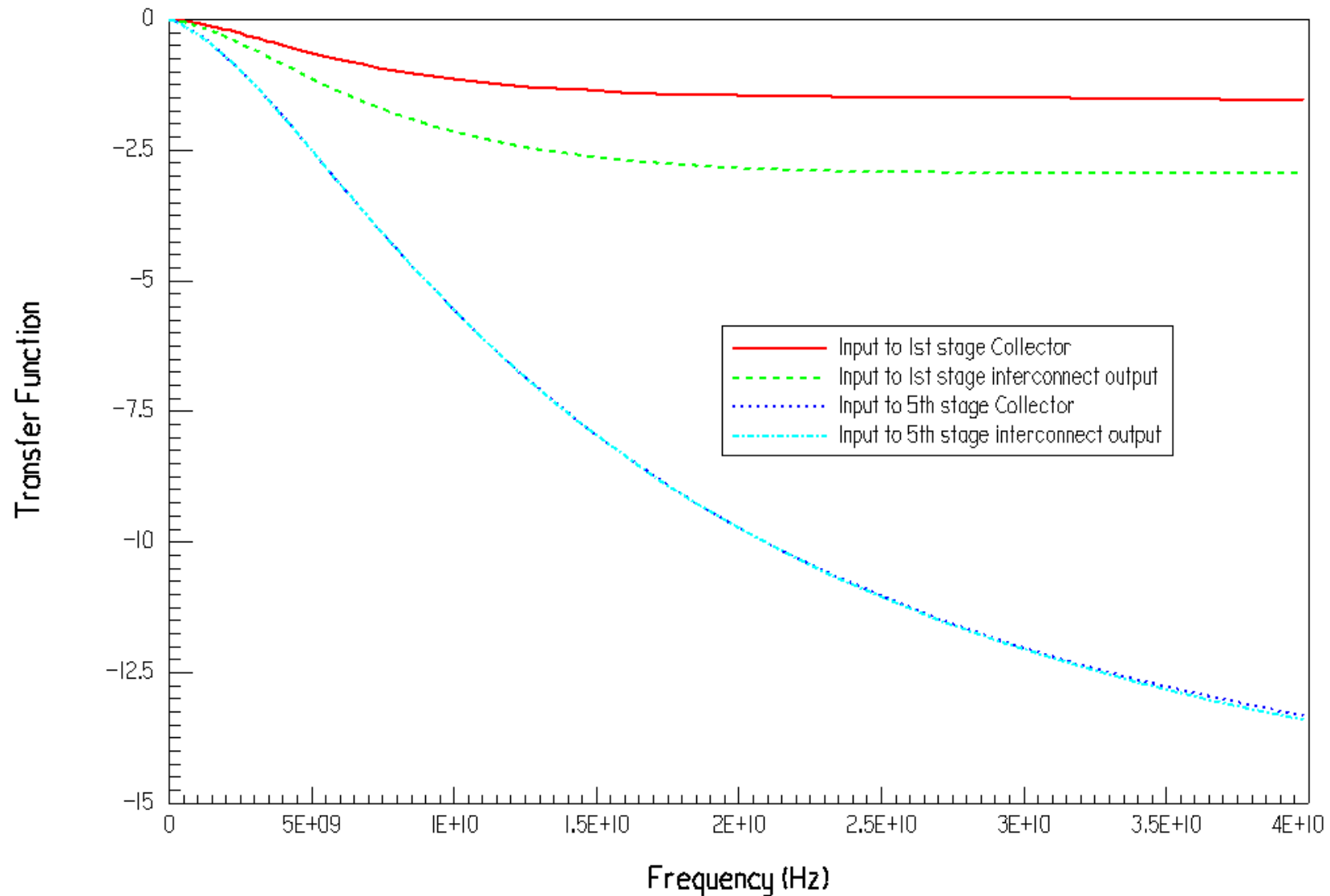
-- Simulation of an input pulse through one stage and 5 stages

*Assume 50 ohm load from HBT connection*



# HFSS Modeling Examples -- DA Interconnects

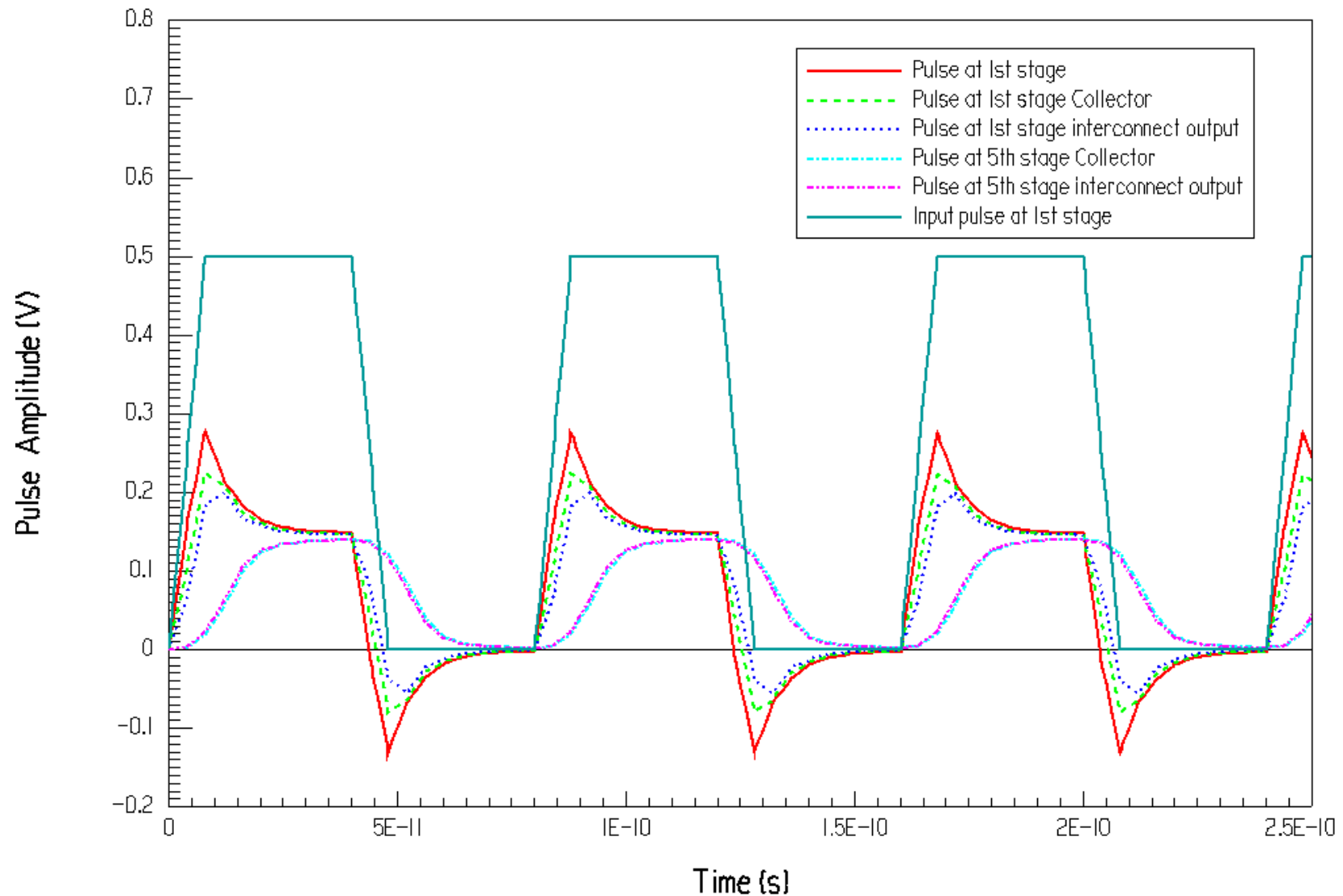
Transfer Function of DA\_CPW Interconnects (50 Ohm load @ each stage)



# HFSS Modeling Examples -- DA Interconnects

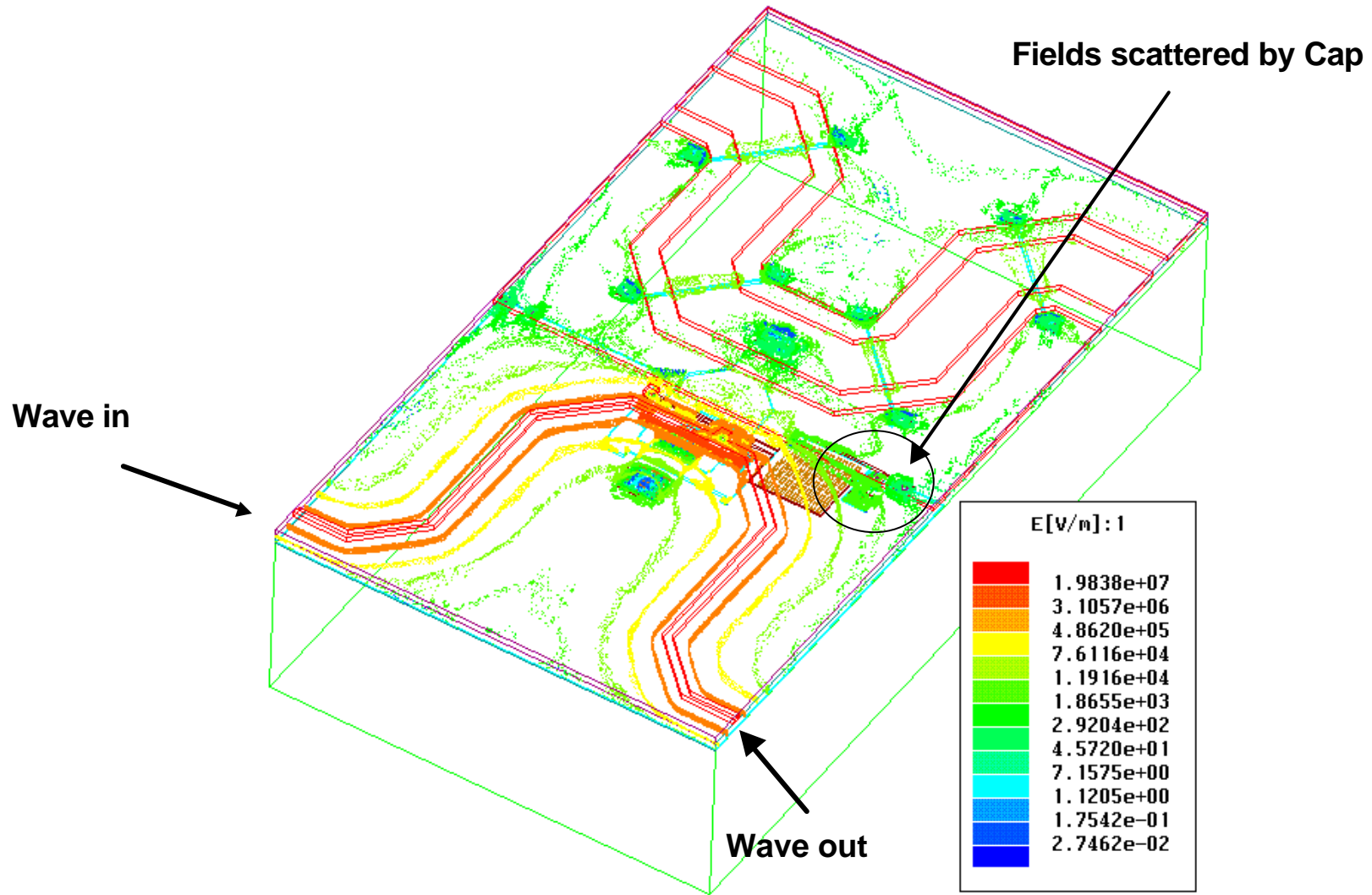
## Pulses of 8ps $t_{rise}$ through interconnects stage by stage

DA\_CPW Interconnects (50 Ohm load at each stage)



# HFSS Modeling Examples -- DA Interconnects

## On-wafer E-fields Scattering at 40G



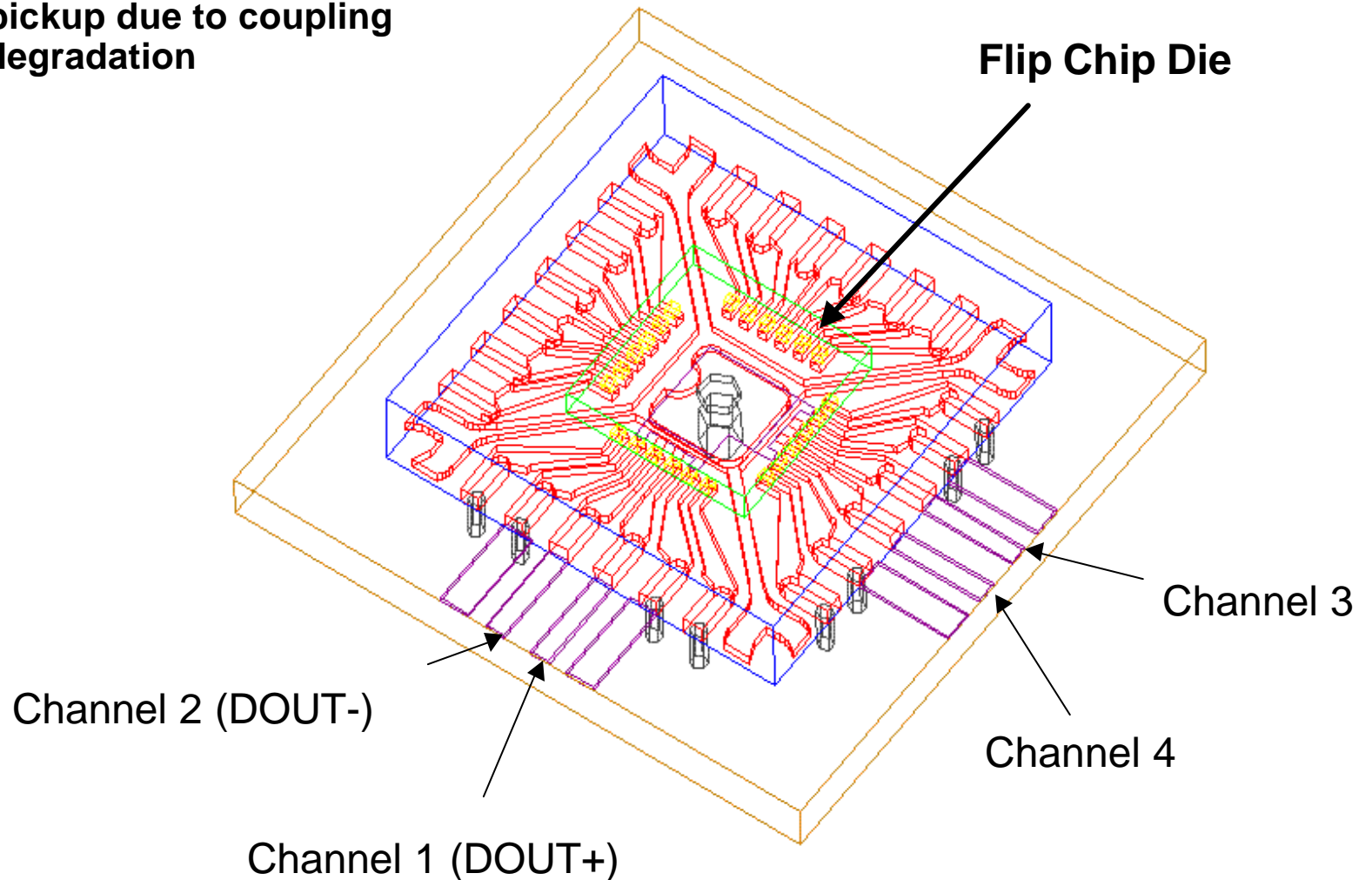
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# HFSS Modeling Examples -- A fcMLF Package

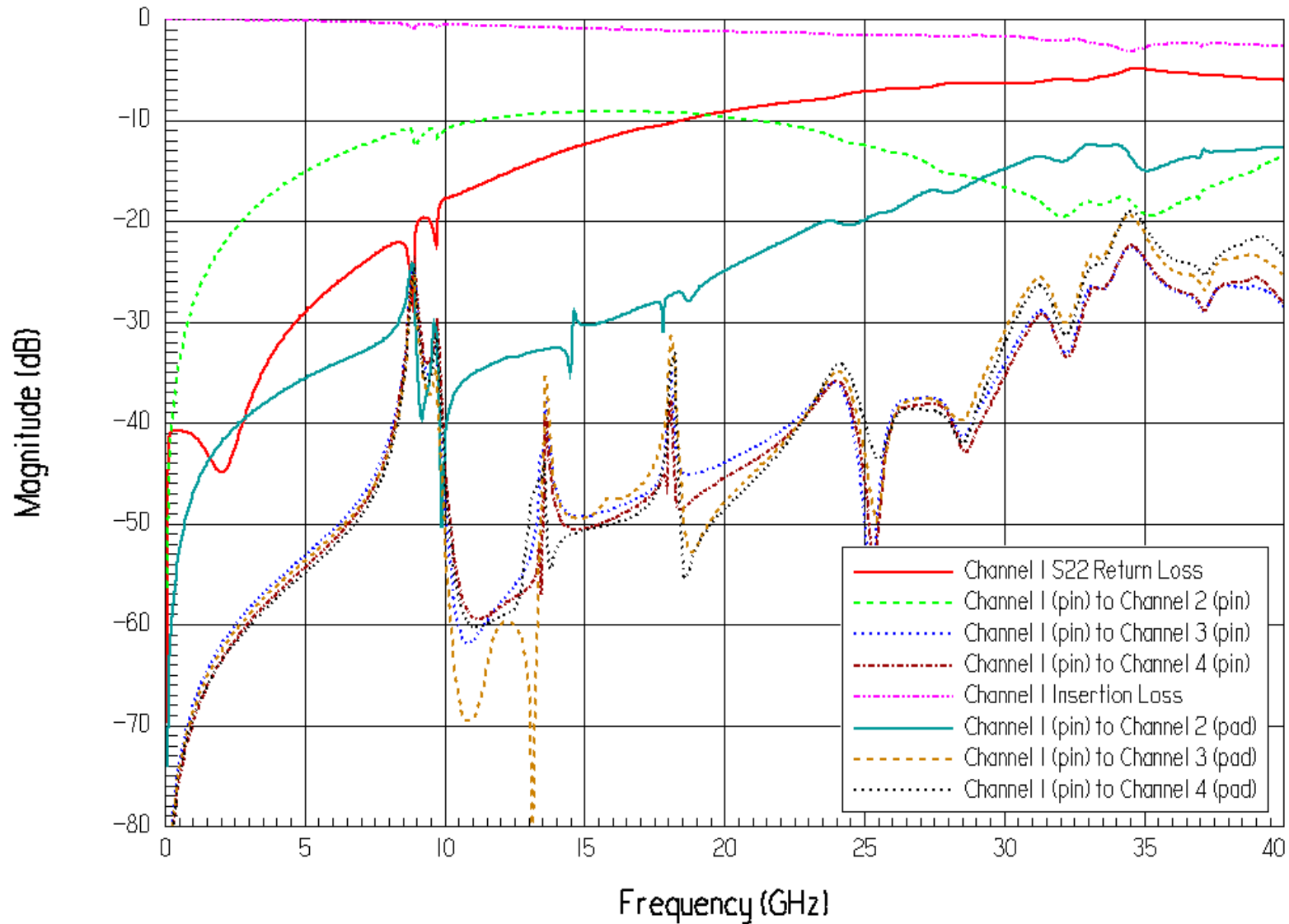
## A Flip-Chip Micro-leadframe (fcMLF) Package

- Lead-frame Z matching
- Noise pickup due to coupling
- $t_{\text{rise}}$  degradation



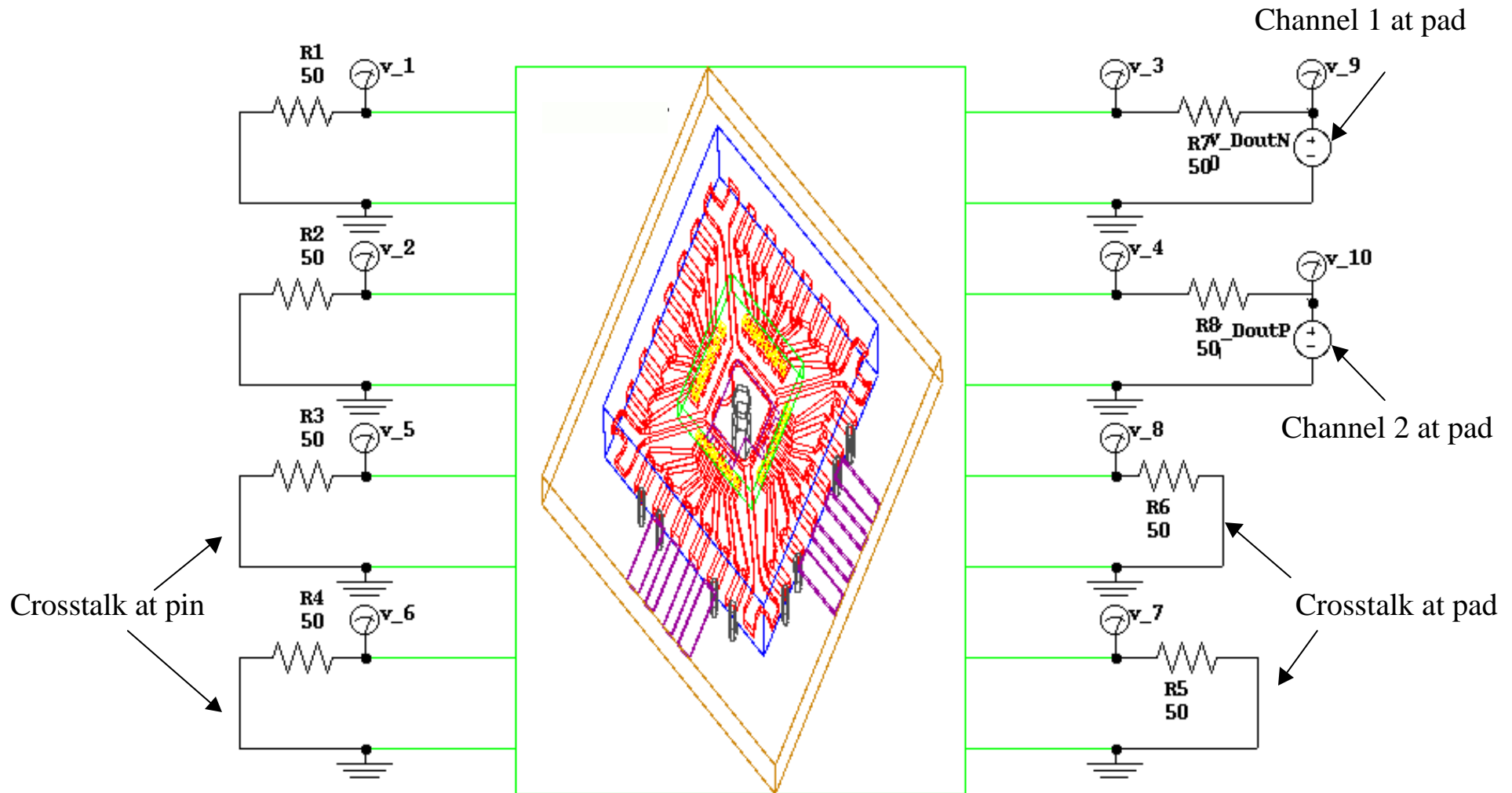
# HFSS Modeling Examples -- A fcMLF Package

## S-Parameters of Channel 1



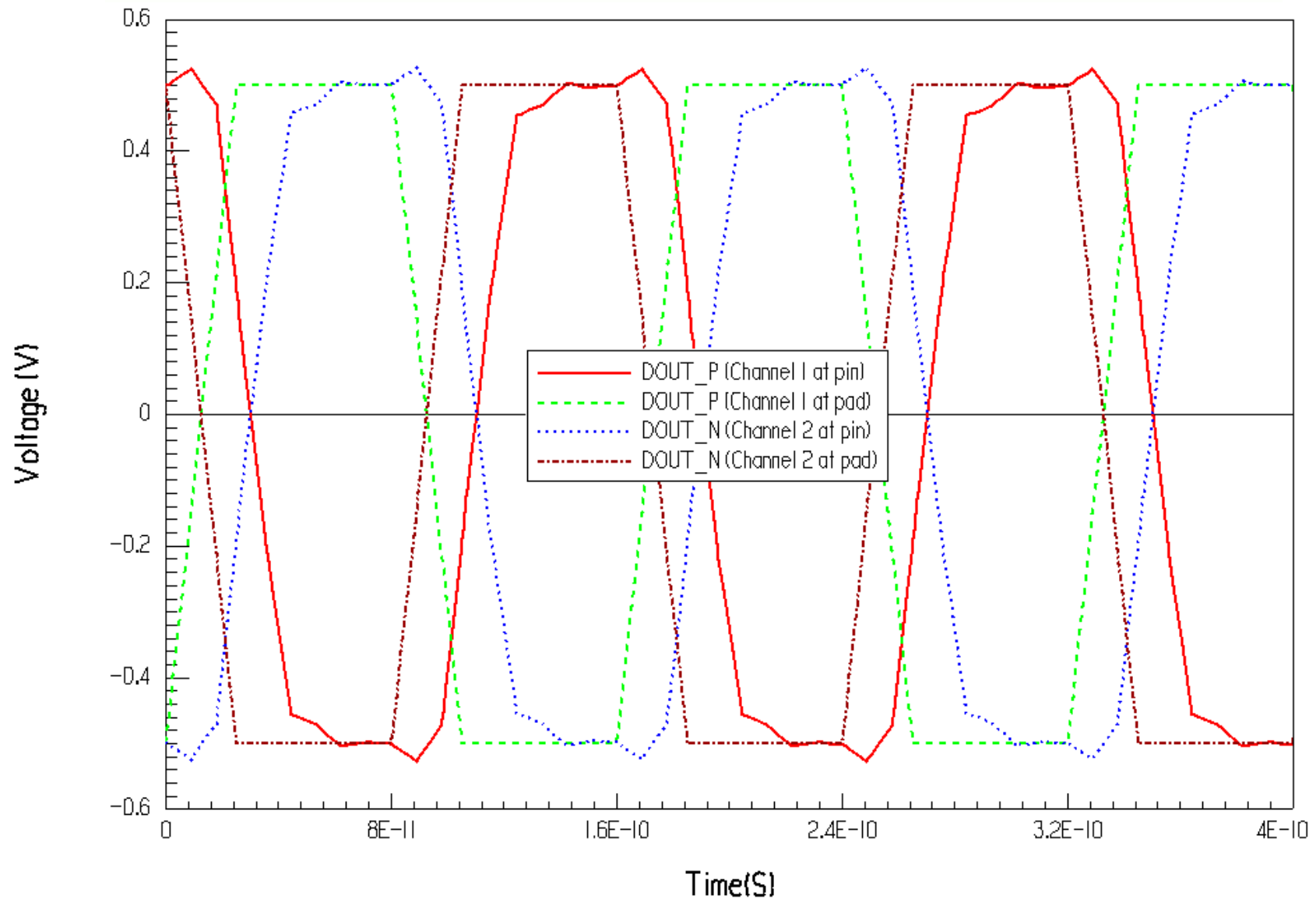
# HFSS Modeling Examples -- A fcMLF Package

## Spice Schematic for Crosstalk Simulation



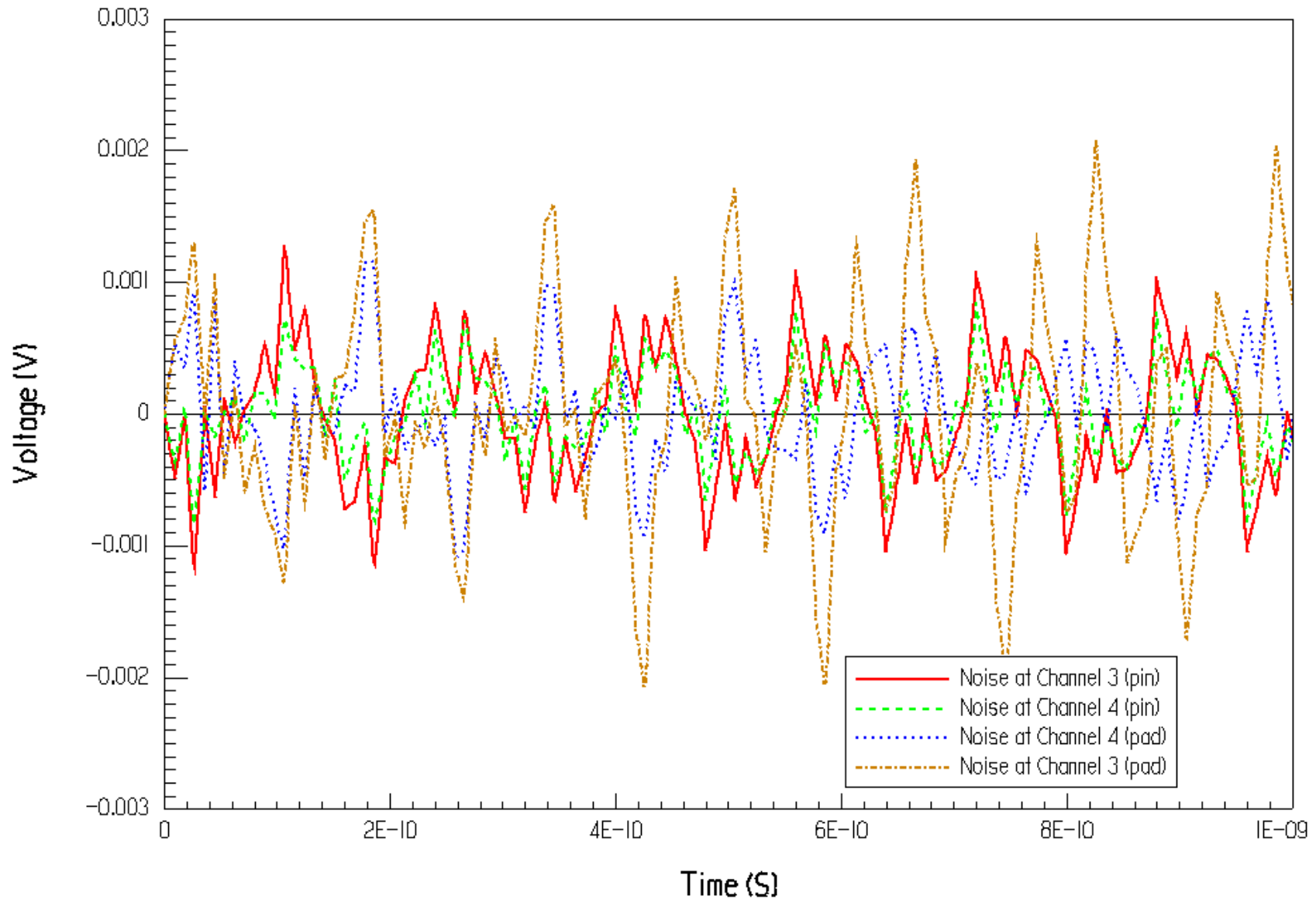
# HFSS Modeling Examples -- A fcMLF Package

## fcMLF Dout Waveform of Channel 1 and 2



# HFSS Modeling Examples -- A fcMLF Package

## Noise Pickup at Differential Data Output



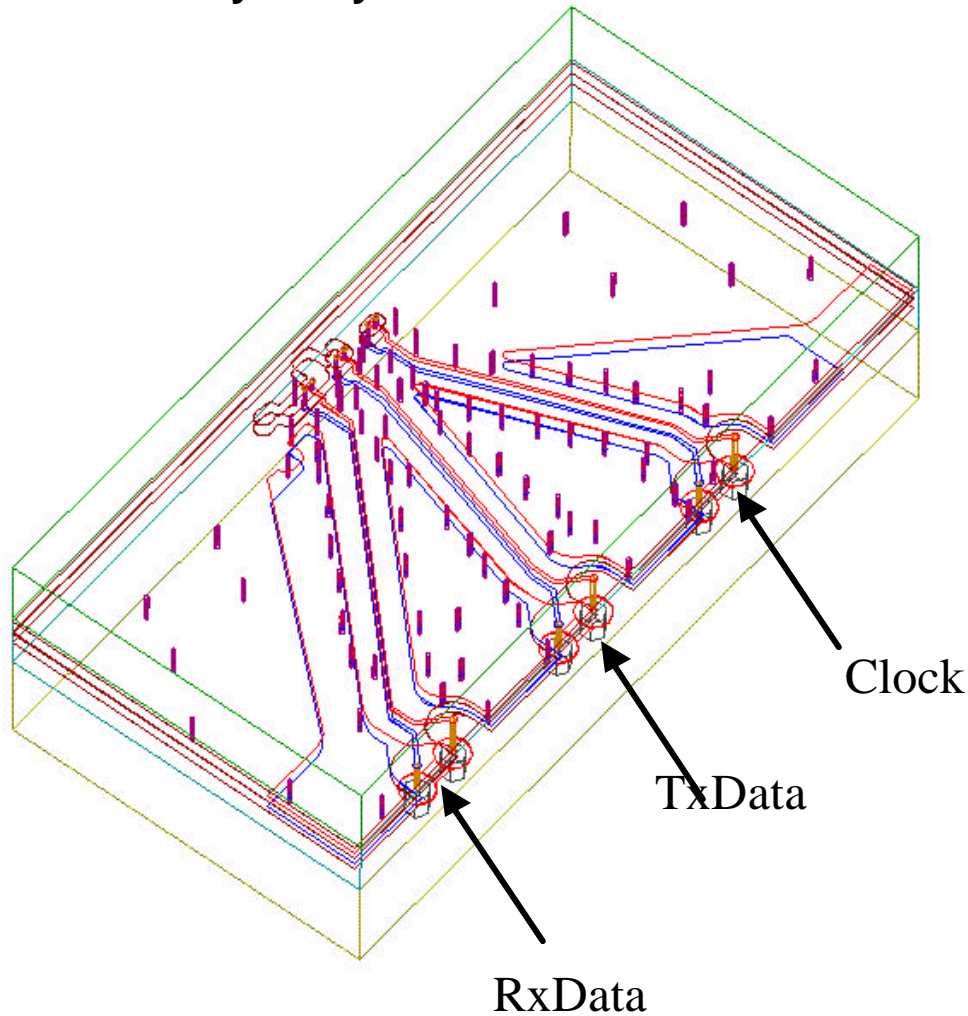
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- **A BGA Package High Speed Channel**
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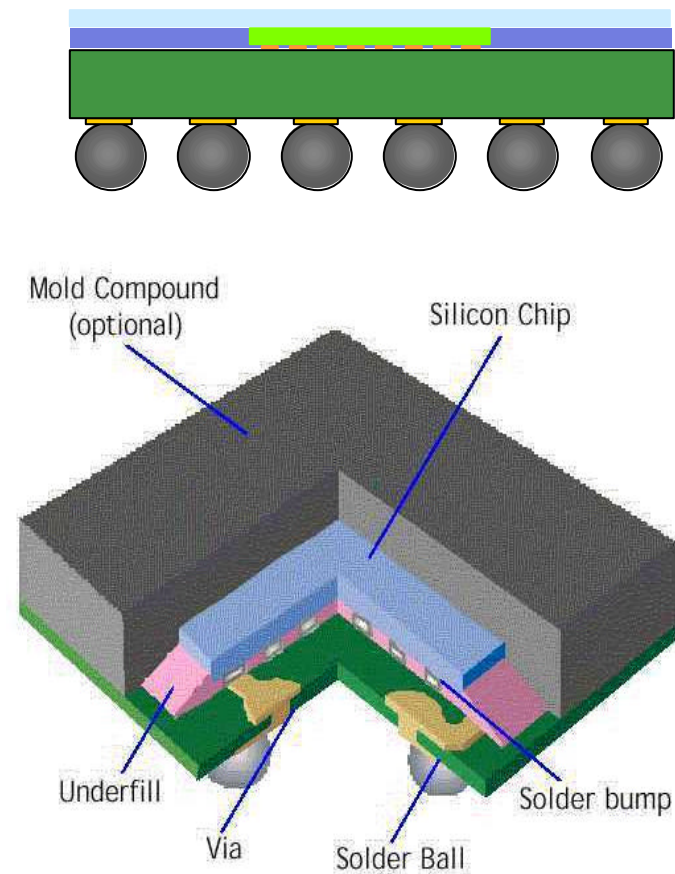
# HFSS Modeling Examples -- A BGA Package HS Channels

## A High Speed Channel BAG Package Model

- TDR simulation
- Sensitivity analysis

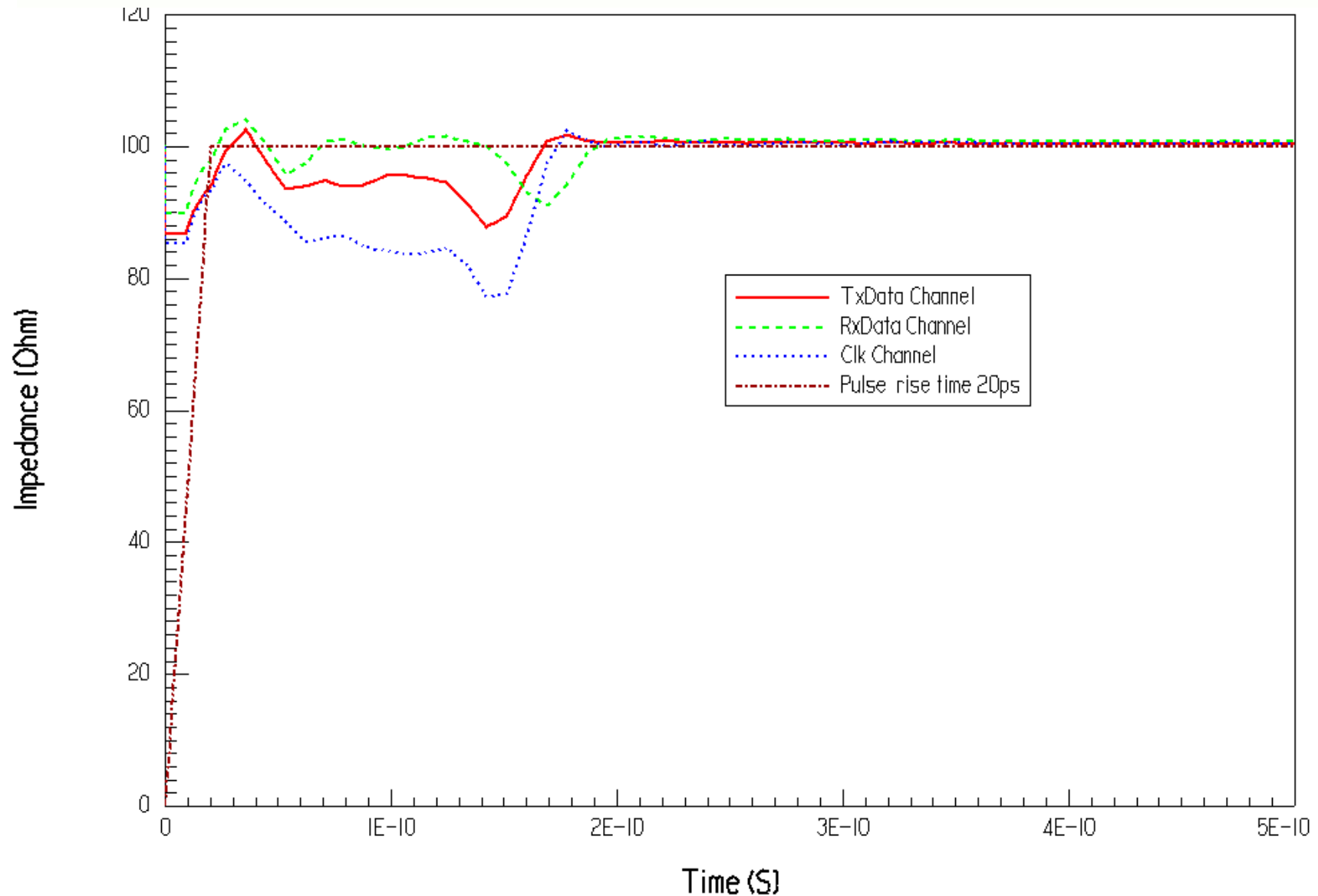


## A 17x17mm FC BGA Package



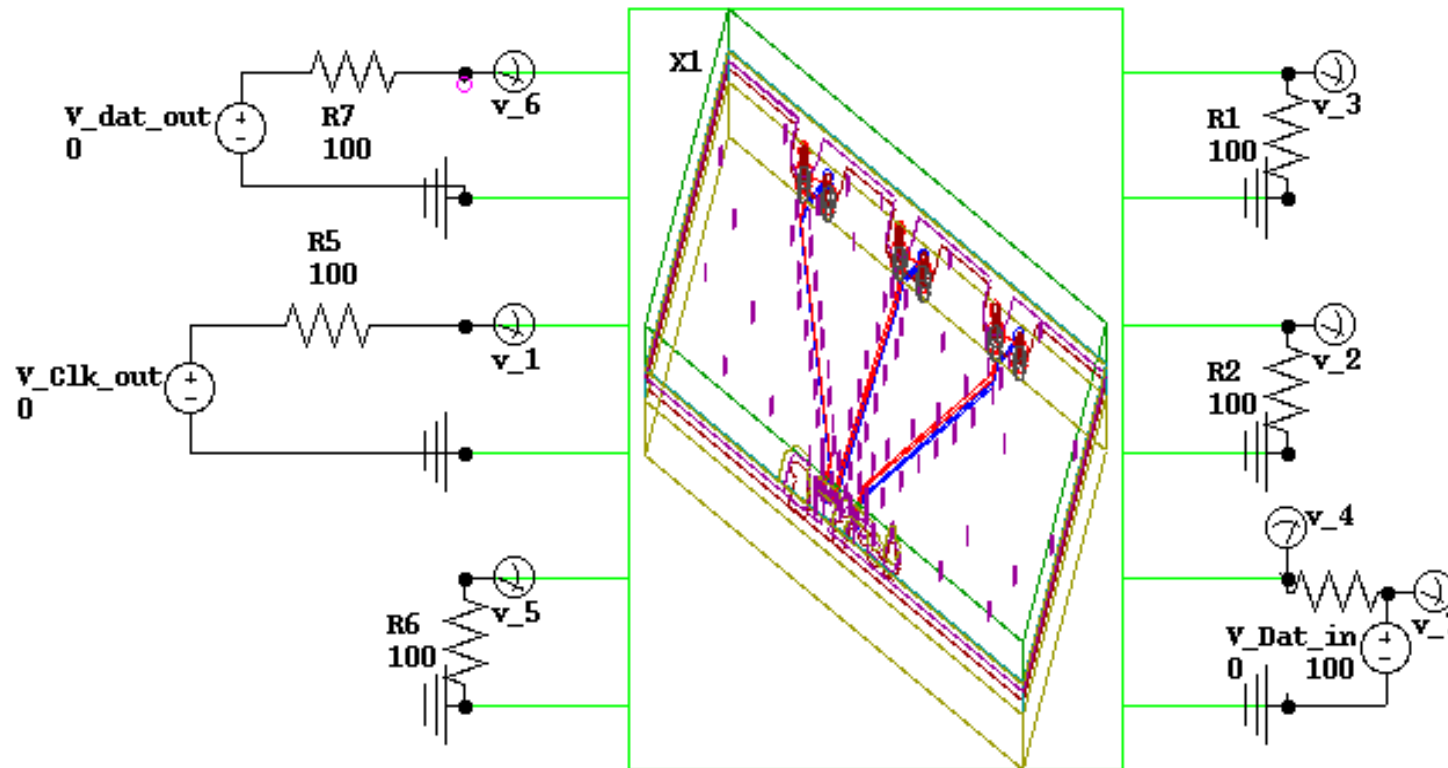
# HFSS Modeling Examples -- A BGA Package HS Channels

## Differential TDR with T<sub>rise</sub> 20ps

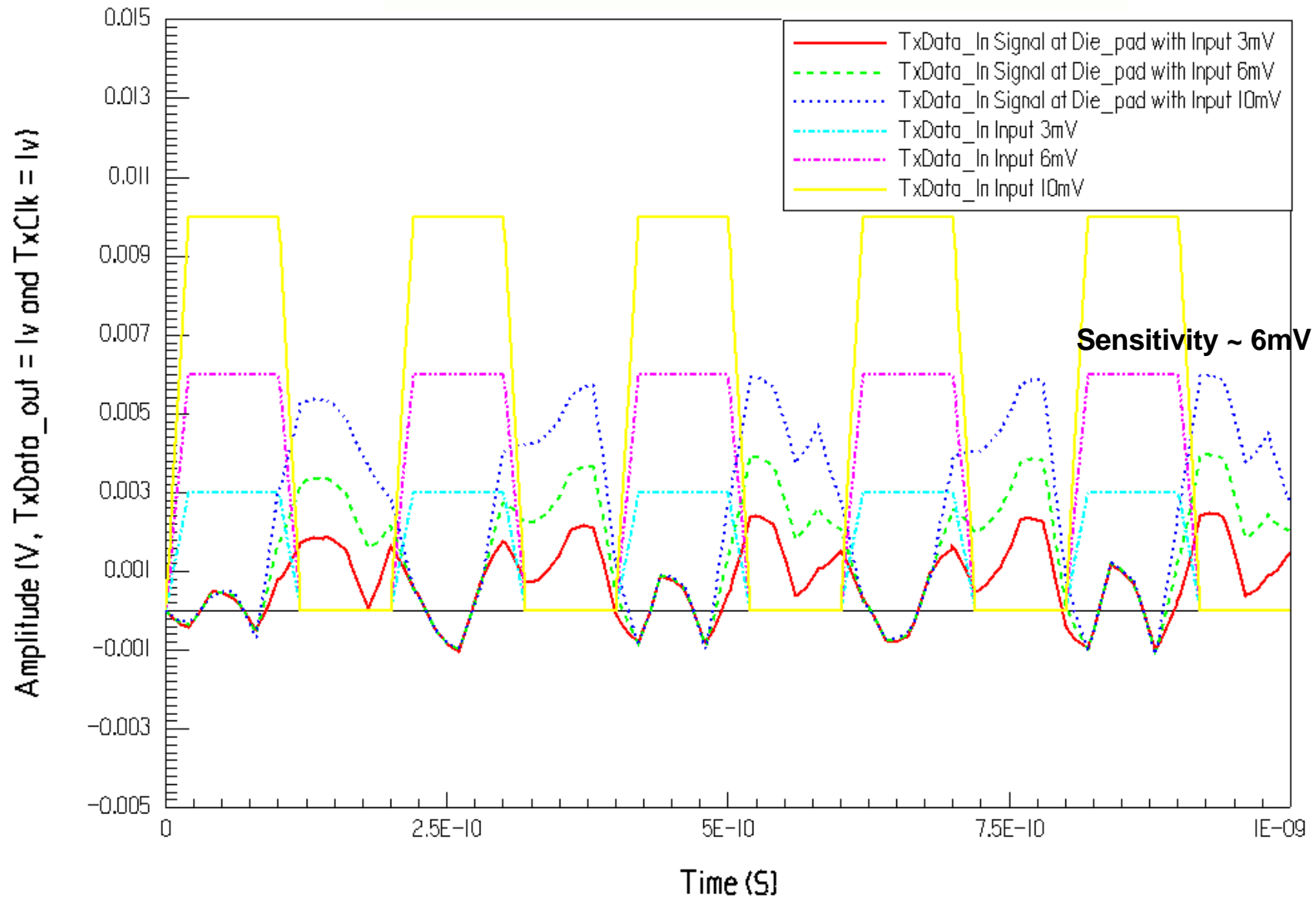


# HFSS Modeling Examples -- A BGA Package HS Channels

## Sensitivity Simulation



# HFSS Modeling Examples -- A BGA Package HS Channels



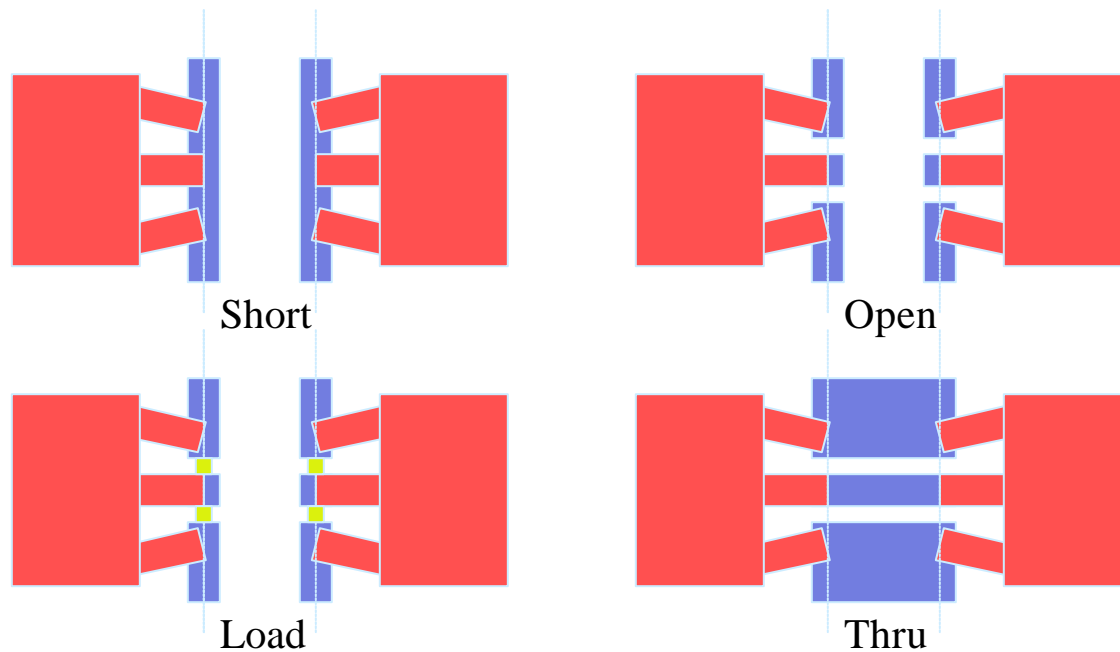
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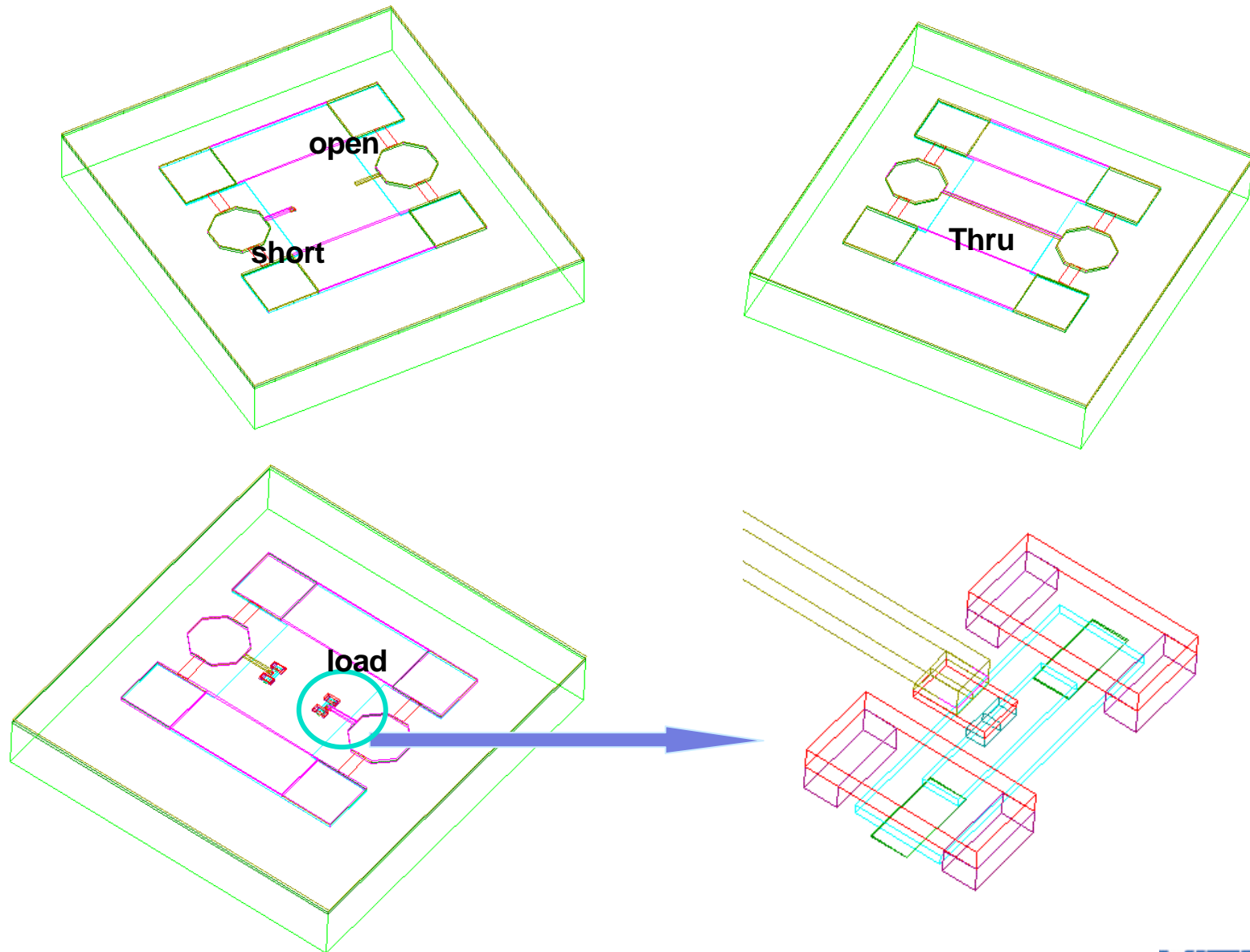
# HFSS Modeling Examples -- Probe Calibration Elements

## On-Wafer Calibration Techniques

- ◆ SOLT (Short-Open-Load-Thru)
- ◆ TRL (Thru-Reflect-Line)
- ◆ LRM (Line-Reflect-Match)
- ◆ LRRM (Line-Reflect-Reflect-Match)

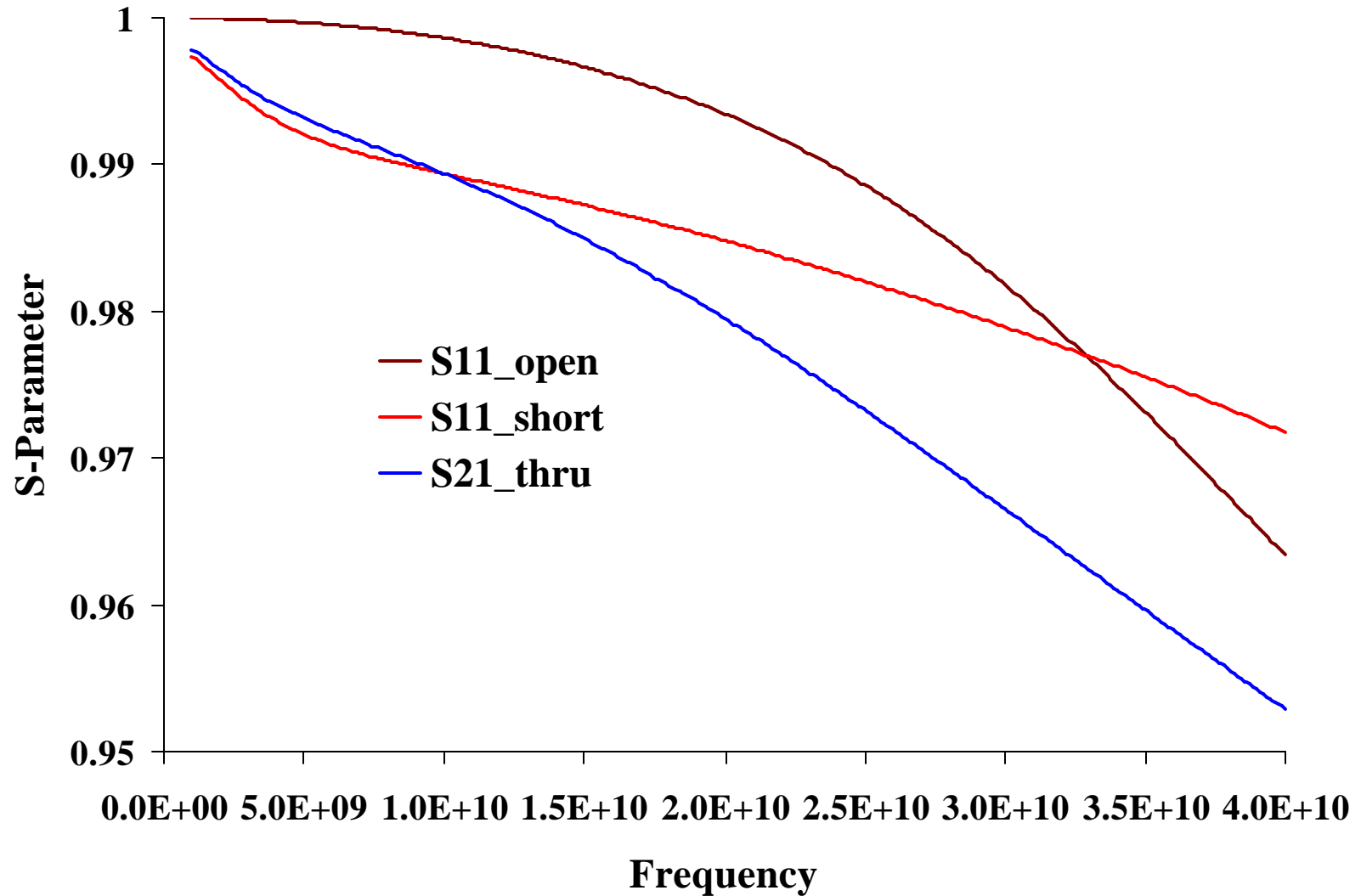


# HFSS Modeling Examples -- Probe Calibration Elements



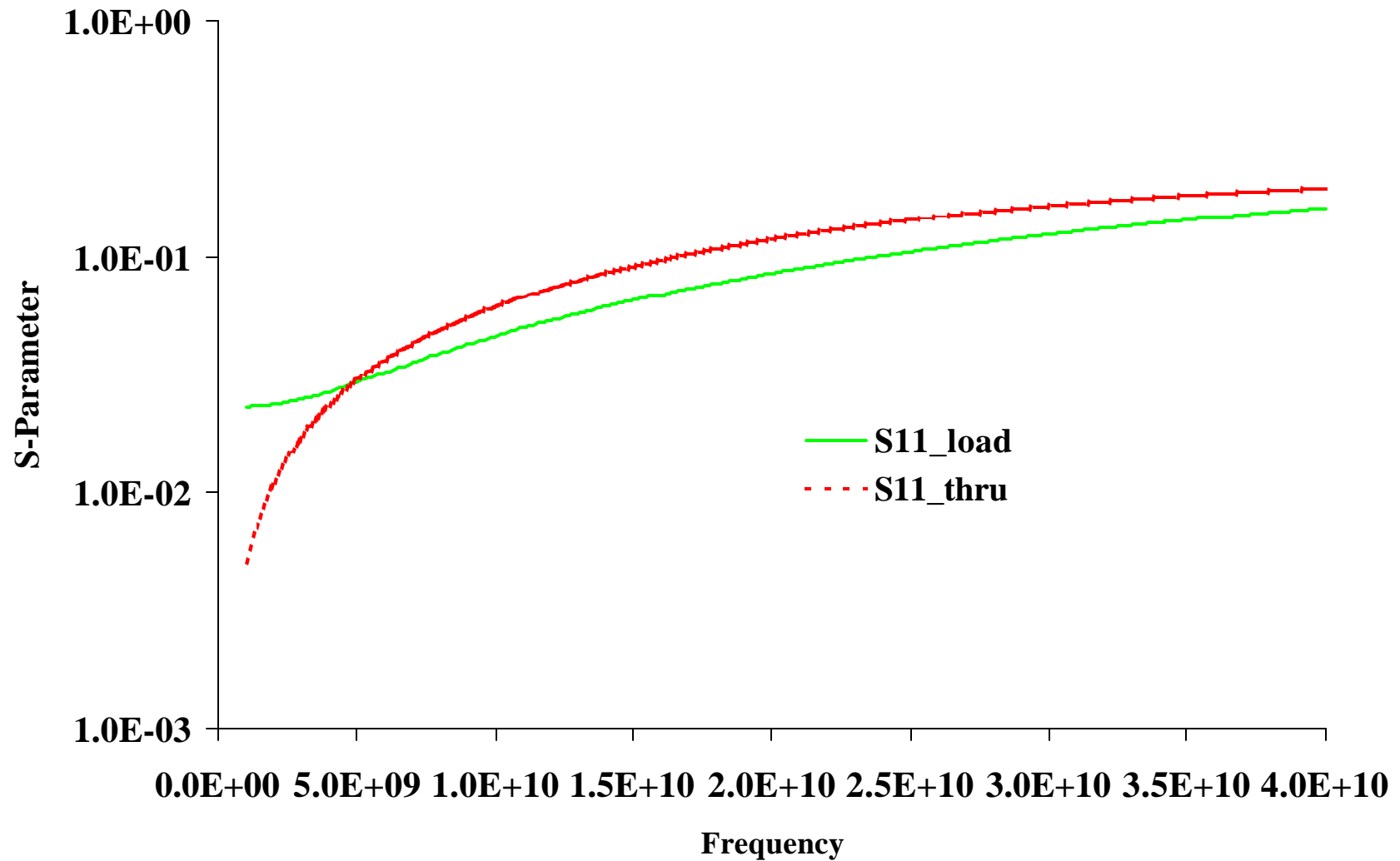
# HFSS Modeling Examples -- Probe Calibration Elements

## S-Parameters of Calibration Kit



# HFSS Modeling Examples -- Probe Calibration Elements

## S11 of Calibration Pads



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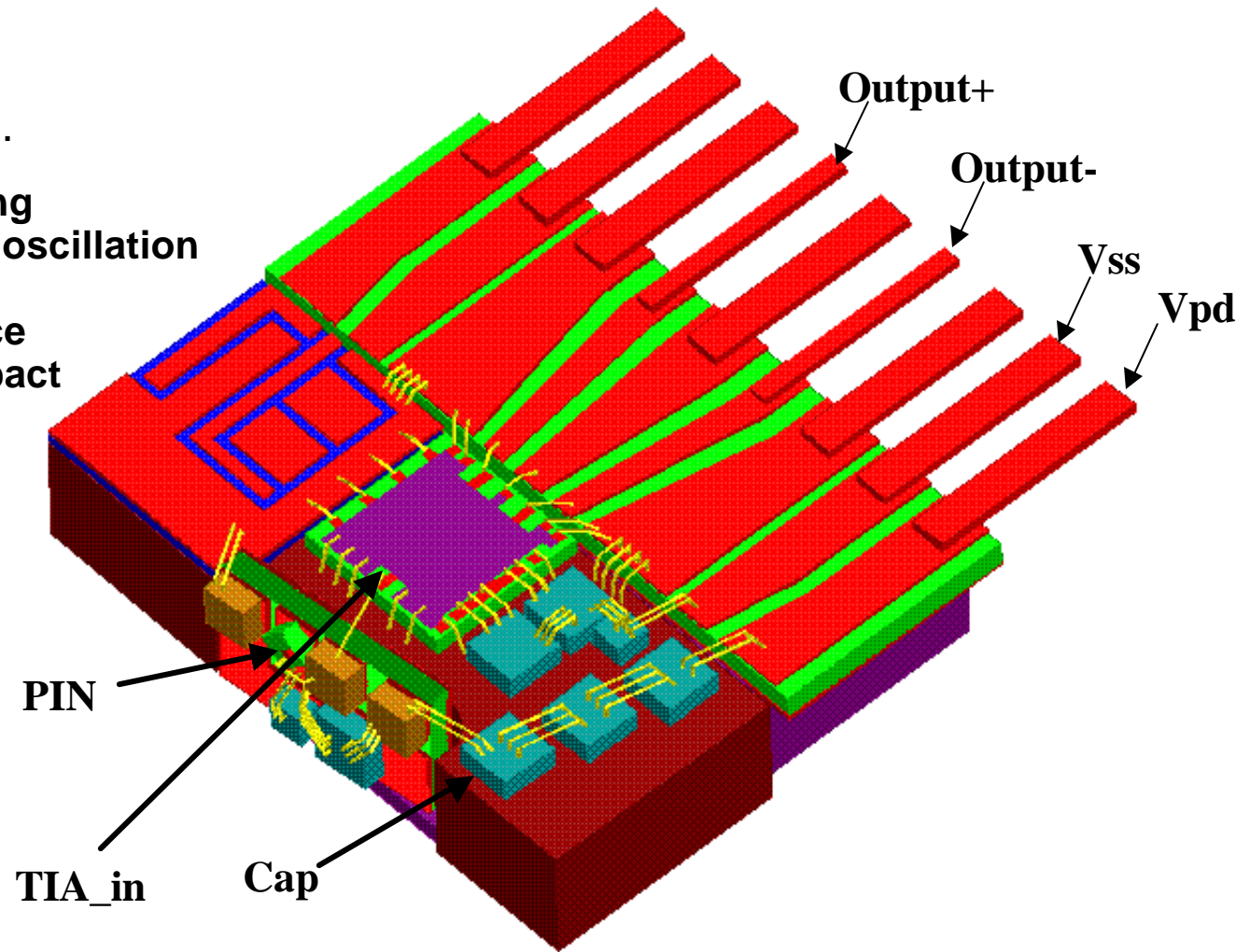
# HFSS Modeling Examples -- An Optical and Electrical Module

## Fully Hybridized 10G Optical Module

- Gain bandwidth

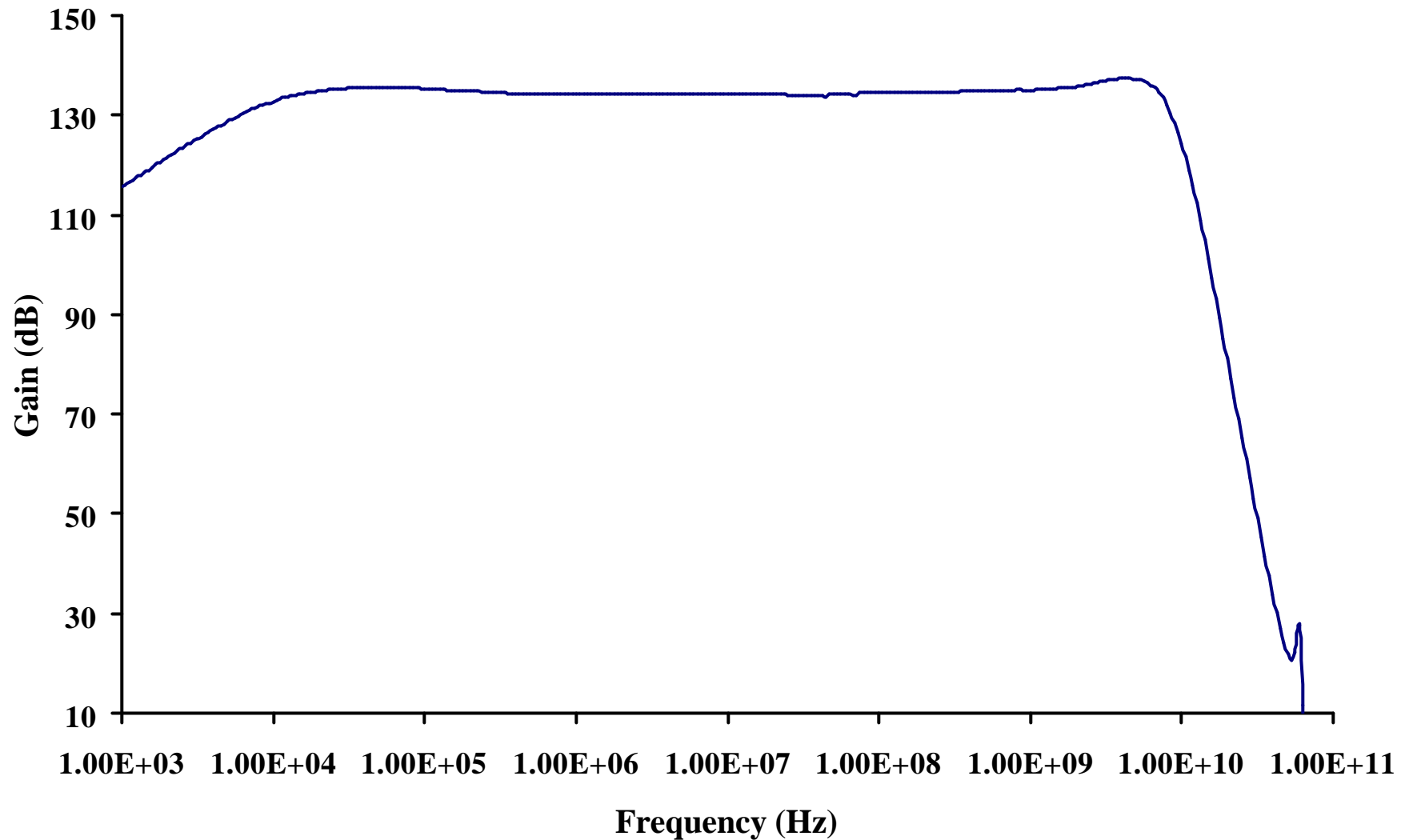
More Can Be Done ...

- PIN to TIA matching
- Coupling induced oscillation
- Bandwidth
- Possible resonance
- Power IR drop impact



# HFSS Modeling Examples -- An Optical and Electrical Module

Pin + TIA Simulation Bandwidth



# HFSS Modeling for High Speed IC -- Some Tips

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When working on full wave interconnect models, need to know

- Lumped or full wave model? (upon rise time or frequency range)
- How many ports defined?
- What is each port's ground reference?
- What is each port's impedance (may be different from 50  $\Omega$ )?
- Is each port polarization aligned?
- What is the upper frequency of a model file ( $F_{max} = 0.35 \sim 0.5/t_{rise}$ )?
- Spice GND and port reference GND
- If RLC model used, what is it's Bragg frequency (cutoff F)?