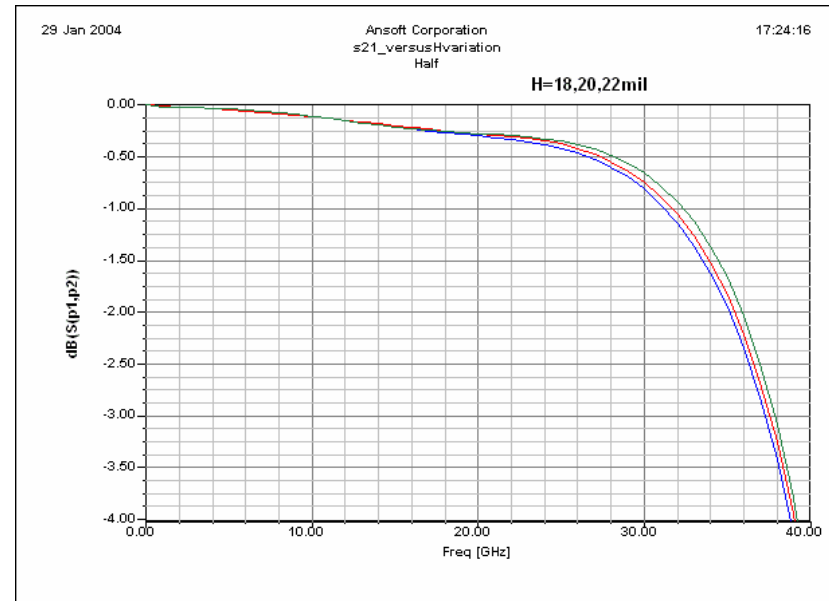
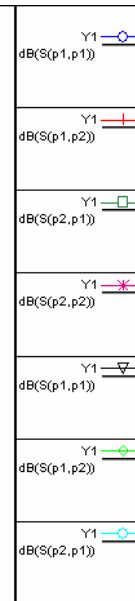
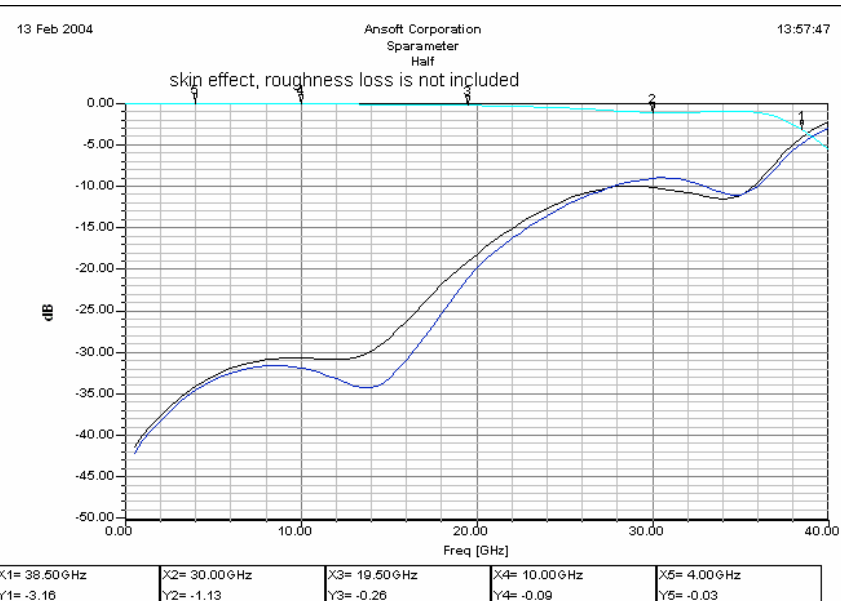
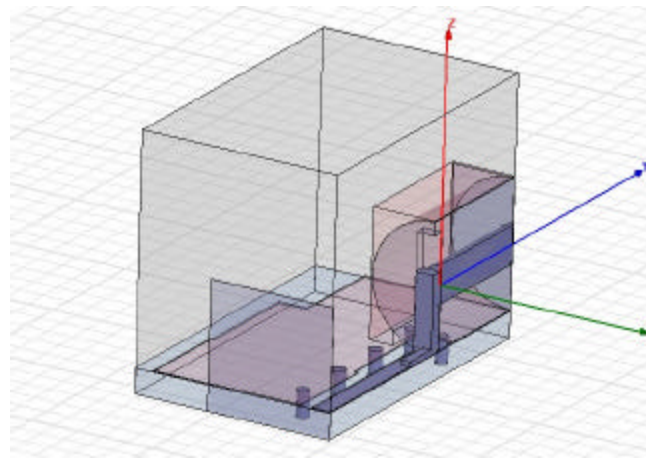
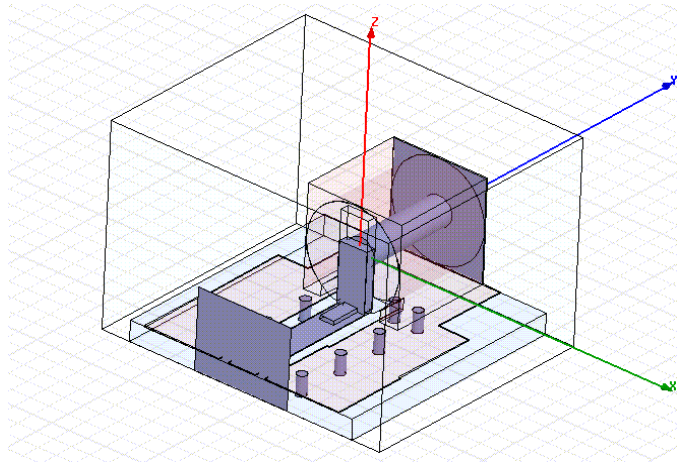


**3 Golden Rules  
for  
High Speed SI in opto-electronics**

**R.Cubillo Feb.2005**

# 10 Gb/s interconnect(HFSSv9):DC-40 GHz

## 3D Coplanar Wave Guide to GPO transition

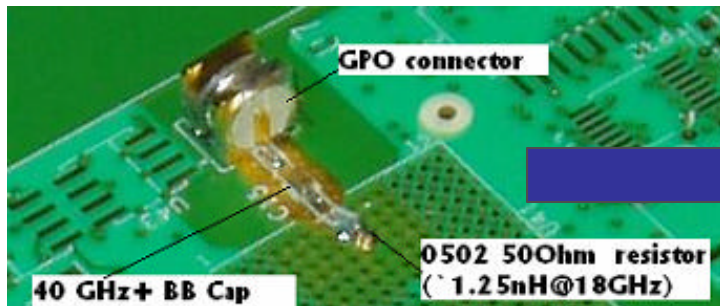


# (HFSS/Lab test)=DC-18 GHz passive RF test

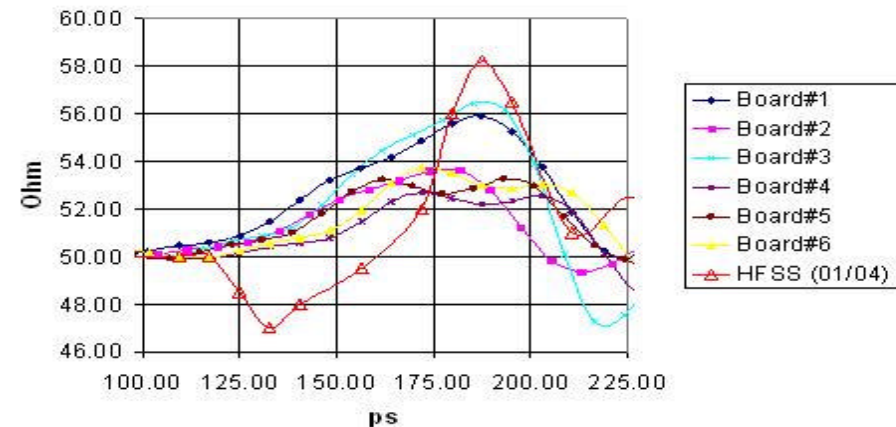
Passive RF test result (TDR ,RL) of 6 PCB\_RF boards

=>fit HFSS sim result

& first spin (proto=production board)

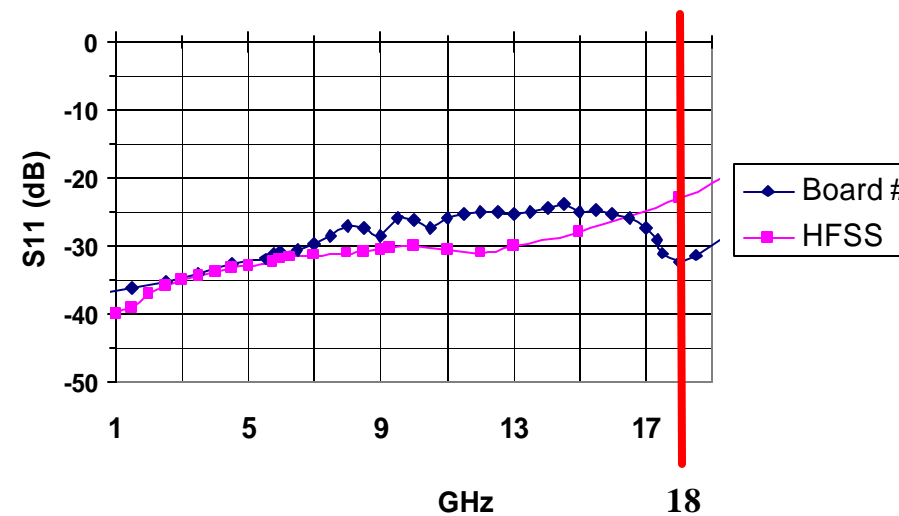


TDR from # Board of the GPO/GCPW section



test result from [30 ps rt] TDR for 6 different PCB\_RF boards

S11 de-embedded from TDR (~30 ps rt)



- TDR result (~30 ps rt) correlate TDR sim result (with 20 ps rt from HFSS)

- TDR De-embedded S11 results correlate HFSS sim result

(best PCB\_RF board matches HFSS sim result within 5 dB

between -25 to -35 dB up to 17 GHz)

•S11 De-embedded test result from [30 ps rt] TDR for best PCB\_RF

# Final test result after CPW/GPO Transition between RF driver and Optical Modulator=> 10 Gb/s optical eye

## Optical eye @ optical output after CPW/GPO transition

1. Unfilter > 48% mask margin, ESNR > 29dB
2. < 18 ps rise/fall time, < 8 ps min jitter pk2pk
3. SONET jitter pk2pk (50KHz\_80MHZ) < 4.5 ps [GR253 Max=10 ps]

## 10 Gb/s Optical eye @ optical output

**Rule of thumb math for RL (S11&S22), rise time, jitter pk2pk matches lab test result (RL between RF Driver & optics < -10 dB up to 10 GHz)**

