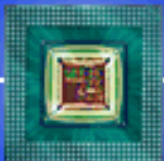


High-Speed Channel Simulation Methodology

Ashraf Badawi
ICG – M&T



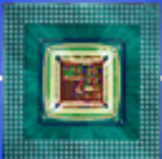
Intel Communications Group

Slide 1

M&T / SI&P • intel

Acknowledgments

- ◆ Members of GHz-SI team
 - ◇ William R. Peters
 - ◇ Kinger Cai
 - ◇ Tony Wu
- ◆ STTD
 - ◇ Alaa El-Rouby



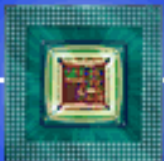
GHz-SI Channel Simulation Flow

- ◆ Agenda

- ◇ Key Message
- ◇ Objectives
- ◇ Package Design and Optimization
- ◇ Channel Simulation Flow(s)

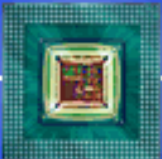
- ◆ Key Message

- ◇ GHZ-SI team is adopting simulation and measurement flows suitable for high speed (Gb/s) channels, and packages.



Objectives

- ◆ Present the design and validation methodologies adopted by GHz-SI.
- ◆ Discuss different simulation flows.
- ◆ Solicit feedback and comments



High Frequency Modeling Tools

- ◆ Electromagnetic simulations:

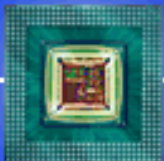
- ◇ HFSS
- ◇ IE3D
- ◇ Ensemble
- ◇ Sonnet
- ◇ FWS
- ◇ Q2D / Q3D
- ◇ TPA
- ◇ CST microwave studio

- ◆ System simulations:

- ◇ ADS
- ◇ Ansoft Designer (under evaluation)

- ◆ Time domain simulations:

- ◇ Eldo
- ◇ H-Spice
- ◇ Cadance
- ◇ Cougar



Package Design and Optimization

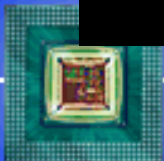
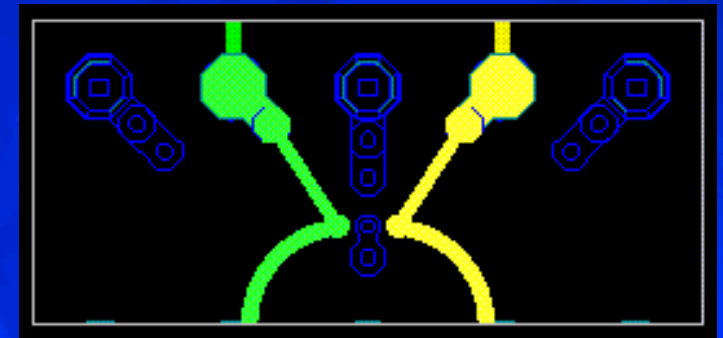
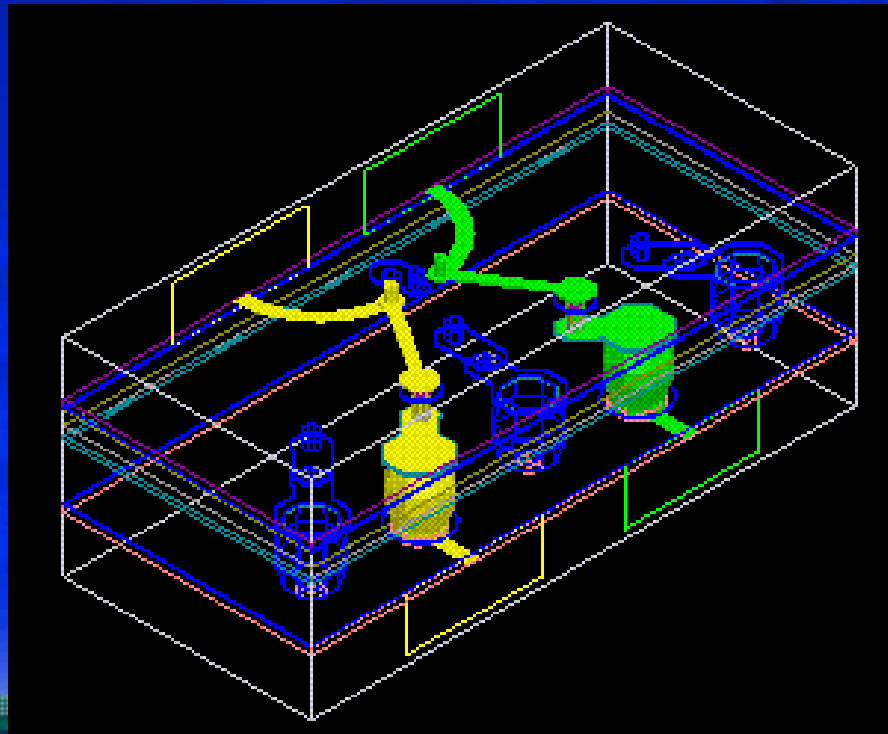
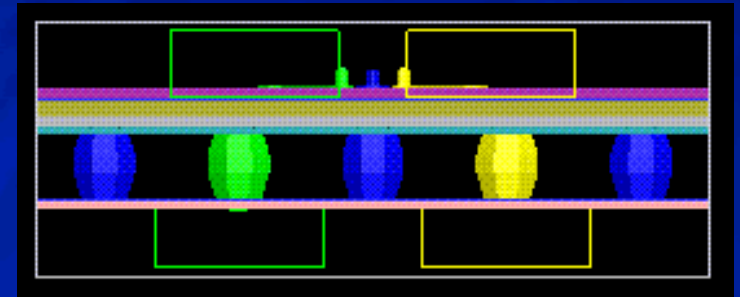
Simulation Setup

1. Solder ball side of the package to be connected to a 50Ω TL ports.
2. Solder ball side interconnect to the PCB is the same for both with-ball and without-ball cases.
3. Die side setup/structure/interconnect is fixed.



With Solder Ball

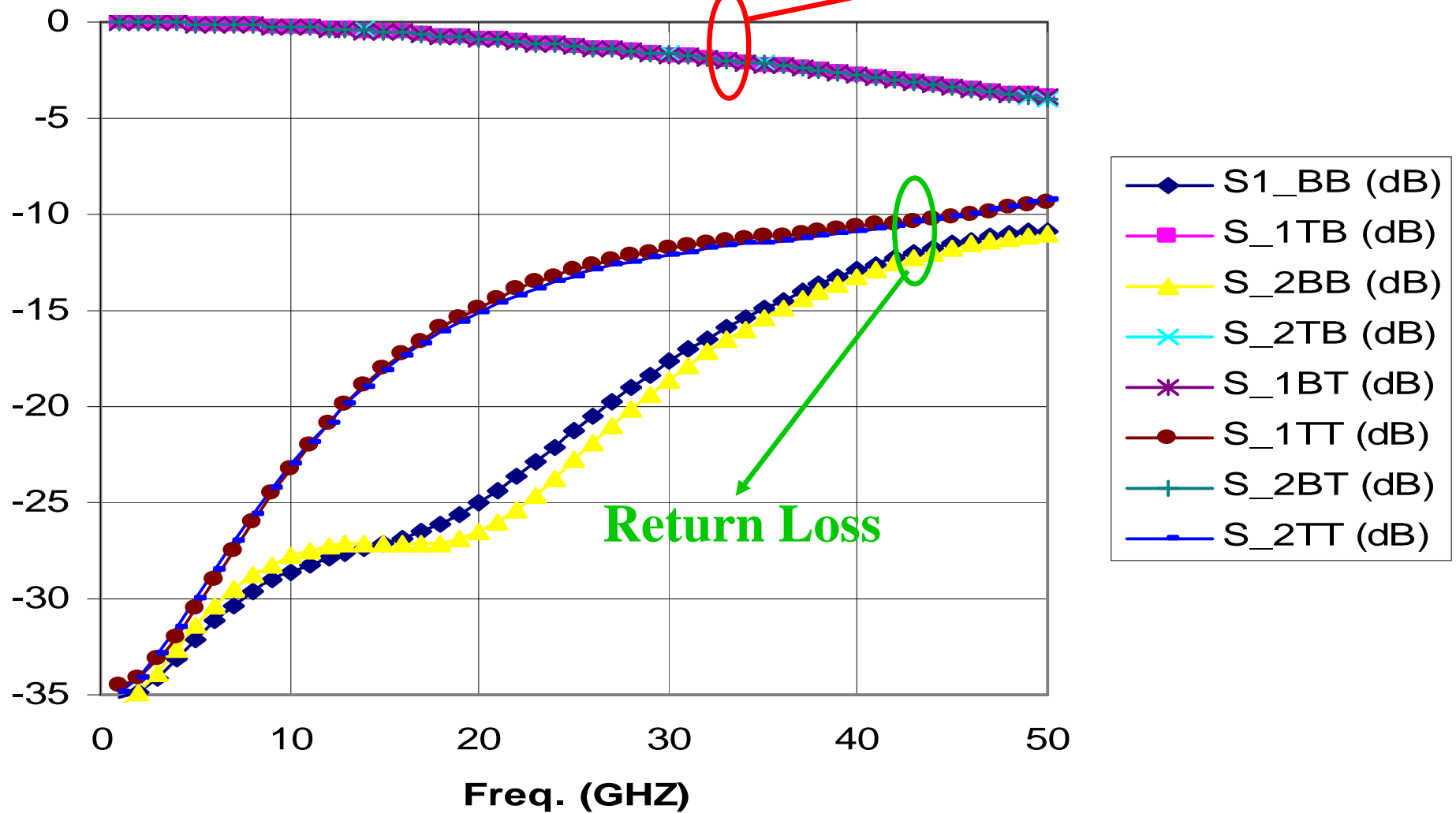
- Lowest Layer is Dielectric
- Signal Via $R=150\ \mu$, $H=70\ \mu$
- GND Pad $R=100\ \mu$, $H=10\ \mu$



Simulated S-Parameters

With Solder Ball

Insertion Loss



With Solder Ball

4-Port |S|-Matrix (dB) @ 30 GHz

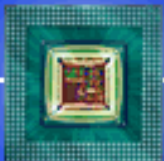
	BP1	BP2	TP1	TP2
BP1	-17.6	-22.3	-1.7	-24
BP2	-22.3	-18.5	-24.0	-1.7
TP1	-1.7	-24.0	-11.8	-26.7
TP2	-24.0	-1.7	-26.7	-12.1

Return Loss

Insertion Loss

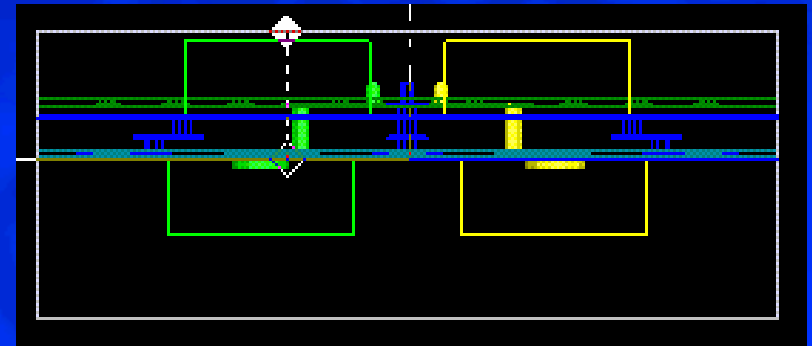
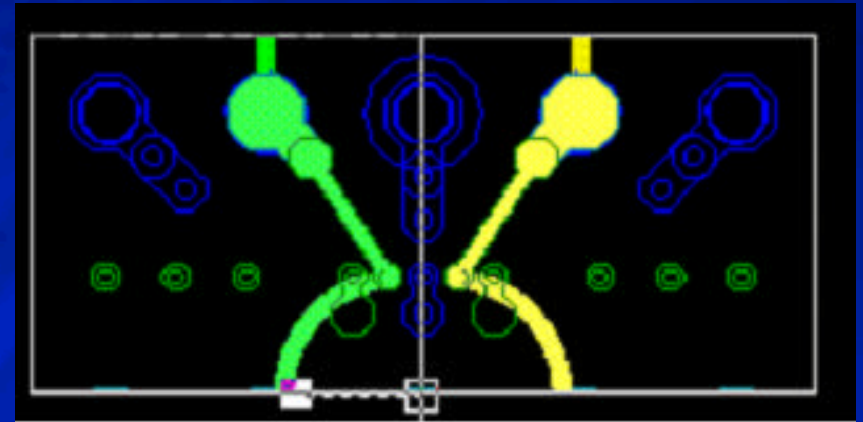
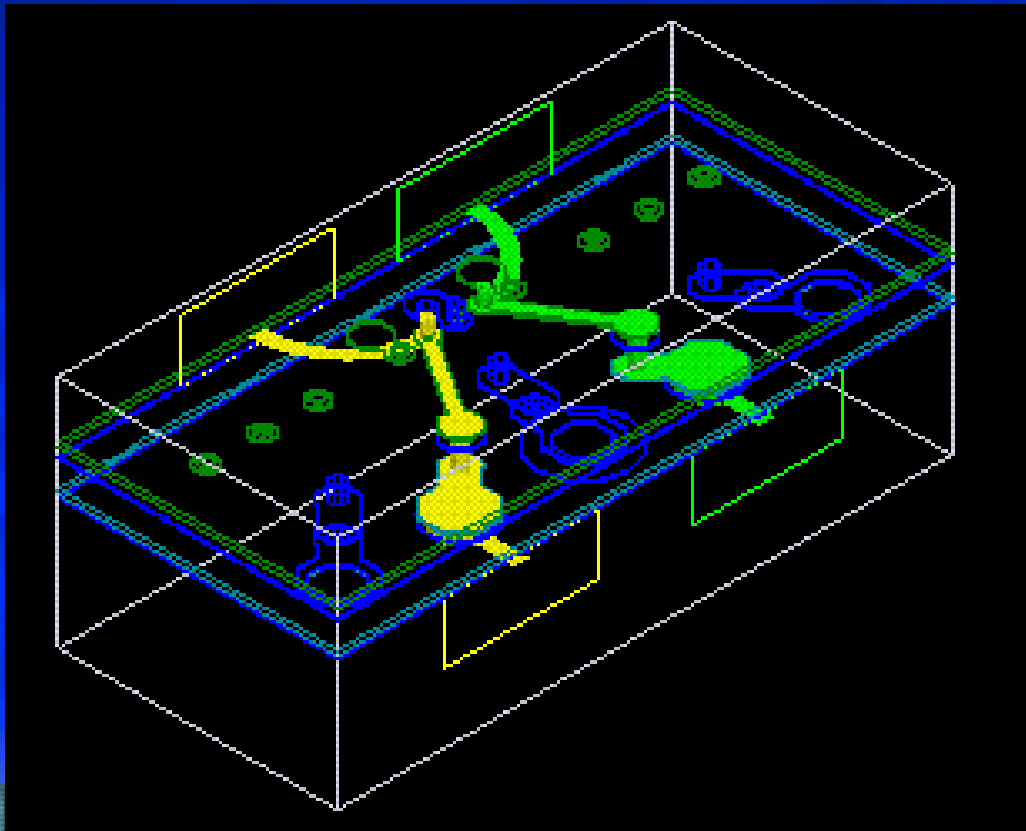
Near Port Coupling

Far Port Coupling



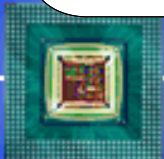
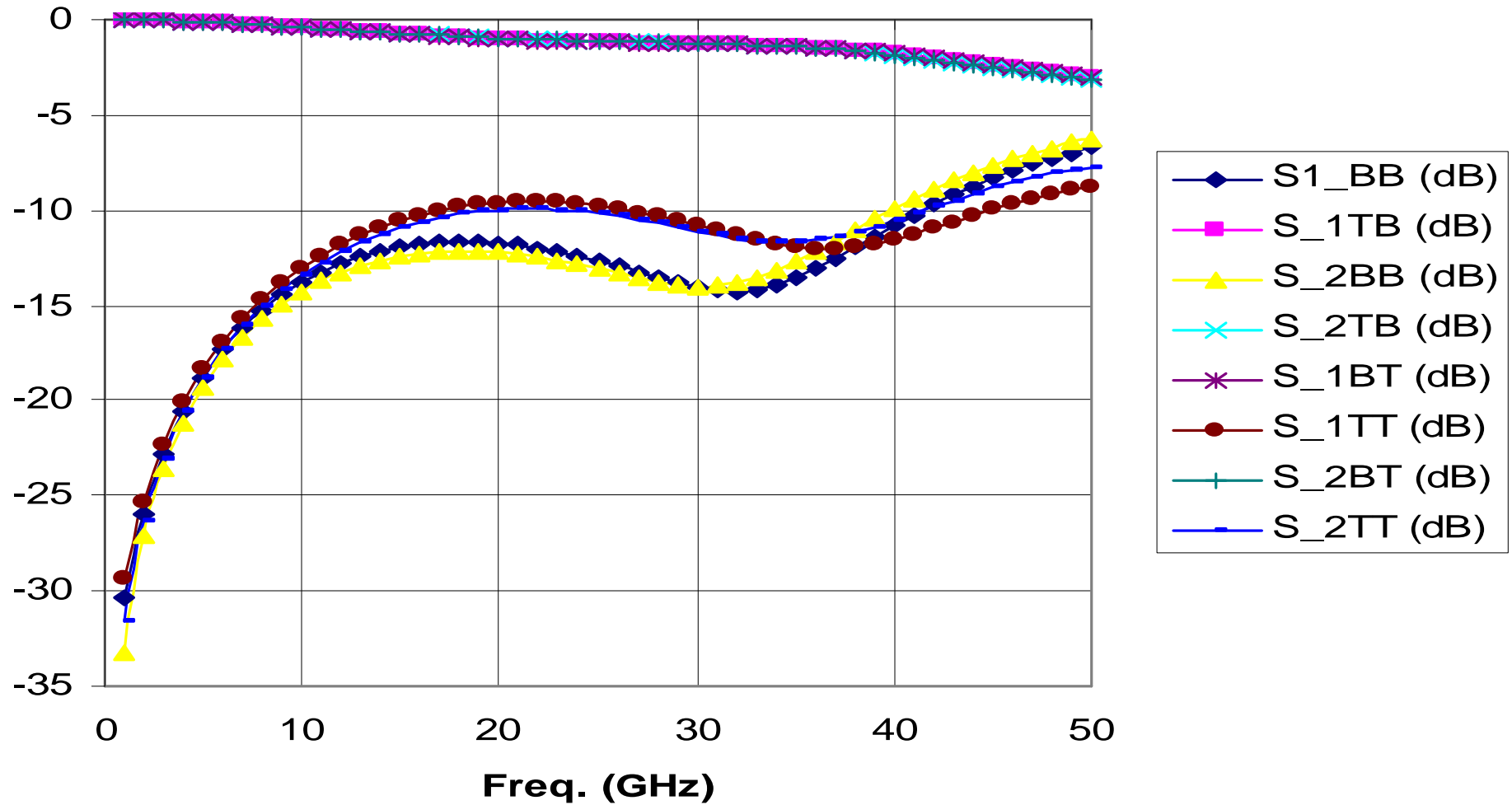
Without Solder Ball

- Lowest Layer is Dielectric
- Signal Via $R=50\ \mu$, $H=70\ \mu$
- GND Pad $R=50\ \mu$, $H=10\ \mu$



Without Solder Ball

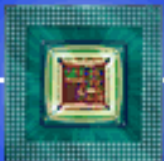
No Solder Ball



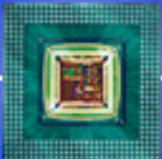
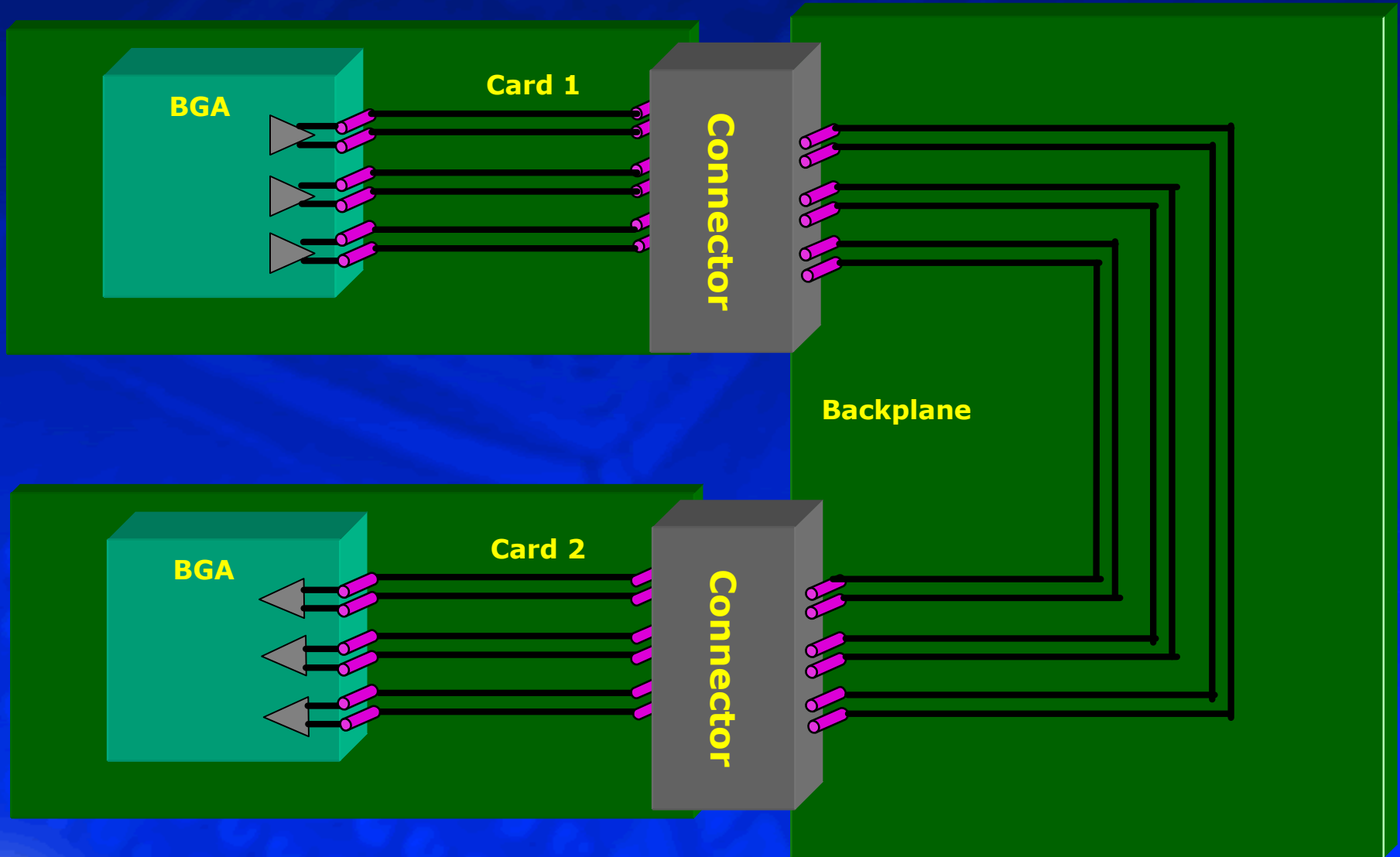
Without Solder Ball

4-Port |S|-Matrix (dB) @ 30 GHz

	BP1	BP2	TP1	TP2
BP1	-14.1	-25.9	-1.2	-28.4
BP2	-25.9	-14.0	-28.5	-1.3
TP1	-1.3	-28.5	-10.8	-34
TP2	-28.4	-1.2	-34.0	-11.1



Simulated Channel Topology



Channel Simulation and Measurements

◆ Frequency Domain Analysis

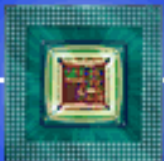
- ◆ Verify channel frequency specs, Identify corner cases
- ◆ Optimize trace configuration
- ◆ Study length effects
- ◆ High frequency modeling

◆ Time domain Analysis

- ◆ Jitter analysis
- ◆ Signal quality assessment
- ◆ Sweep corner cases

◆ Measurements

- ◆ TDR, VNA measurements
- ◆ Jitter and BER measurements



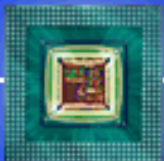
FD vs. TD Parameters

Frequency domain parameters

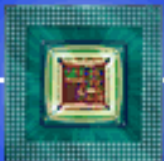
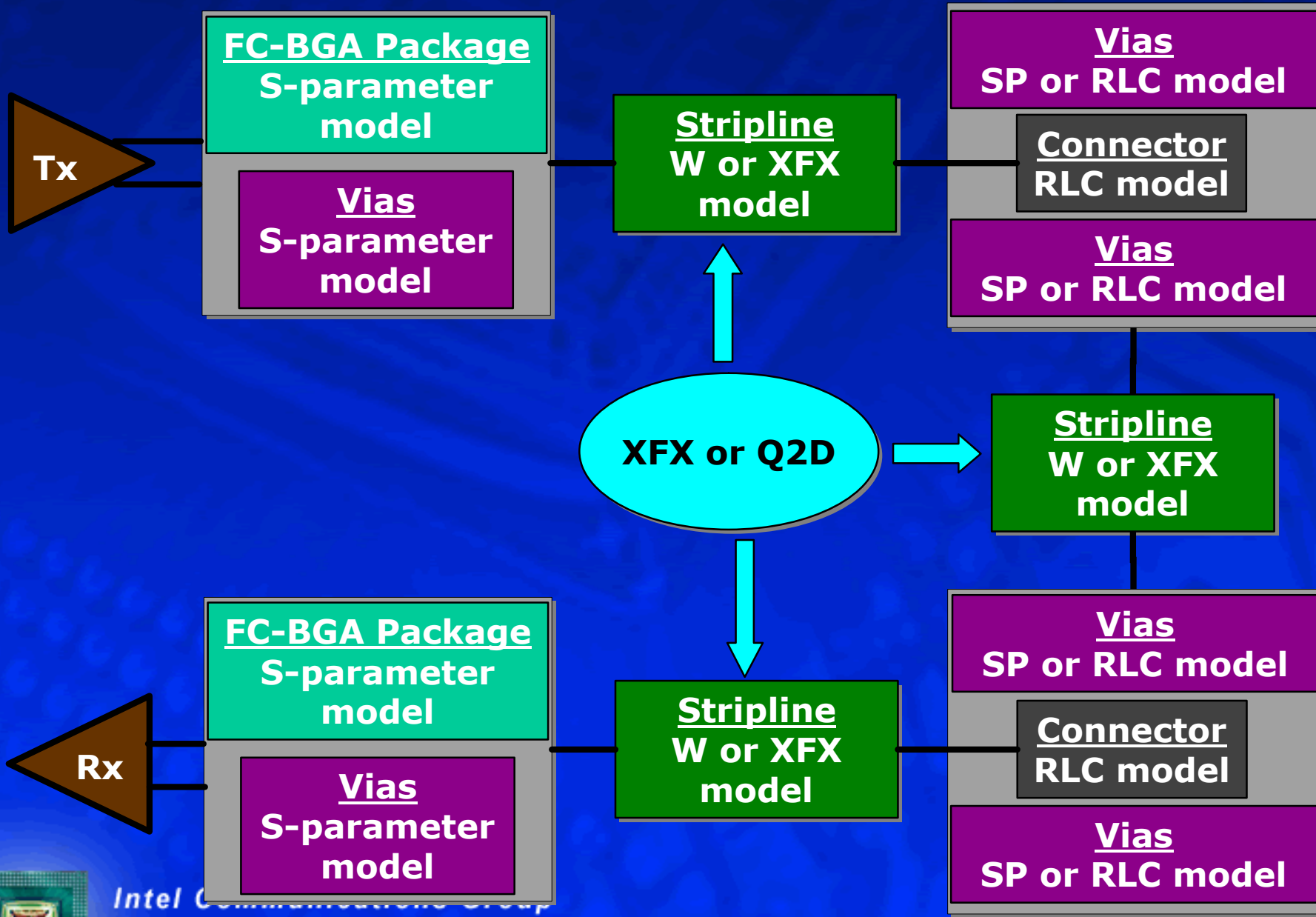
- ◆ Channel:
 - ◇ Reflection (S_{11}).
 - ◇ Transmission (S_{12}).
 - ◇ Coupling (S_{ij})
- ◆ Max/Min impedance variation
- ◆ Resonances

Time domain parameters

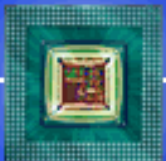
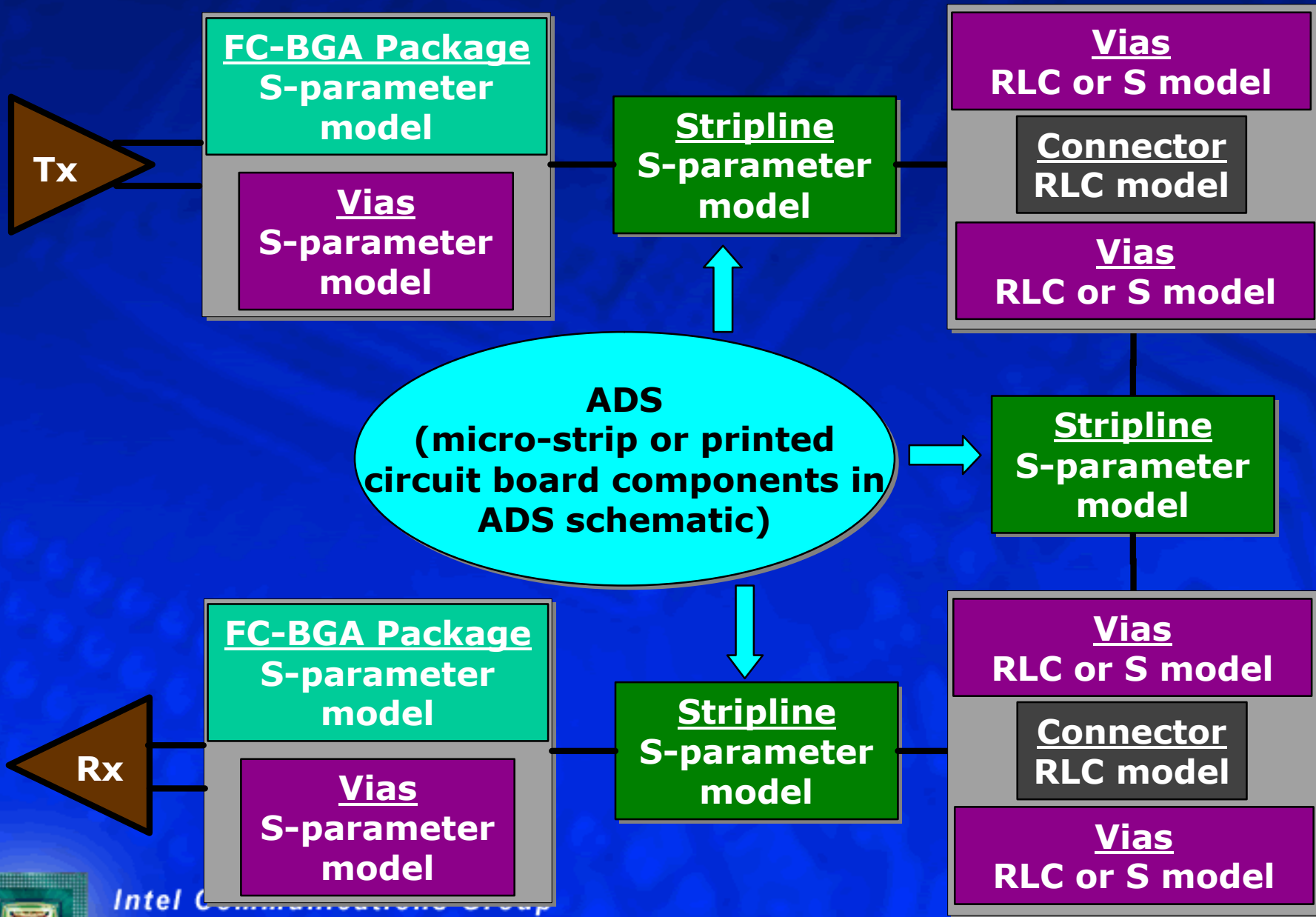
- ◆ Signal Quality:
 - ◇ Over/Undershoot
 - ◇ Ring back
 - ◇ Rise/Fall time
 - ◇ Monotonicity
- ◆ Timing
 - ◇ Jitter
 - ◇ Skew (between diff pairs)
 - ◇ Duty cycle distortion



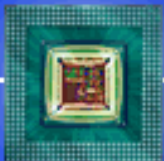
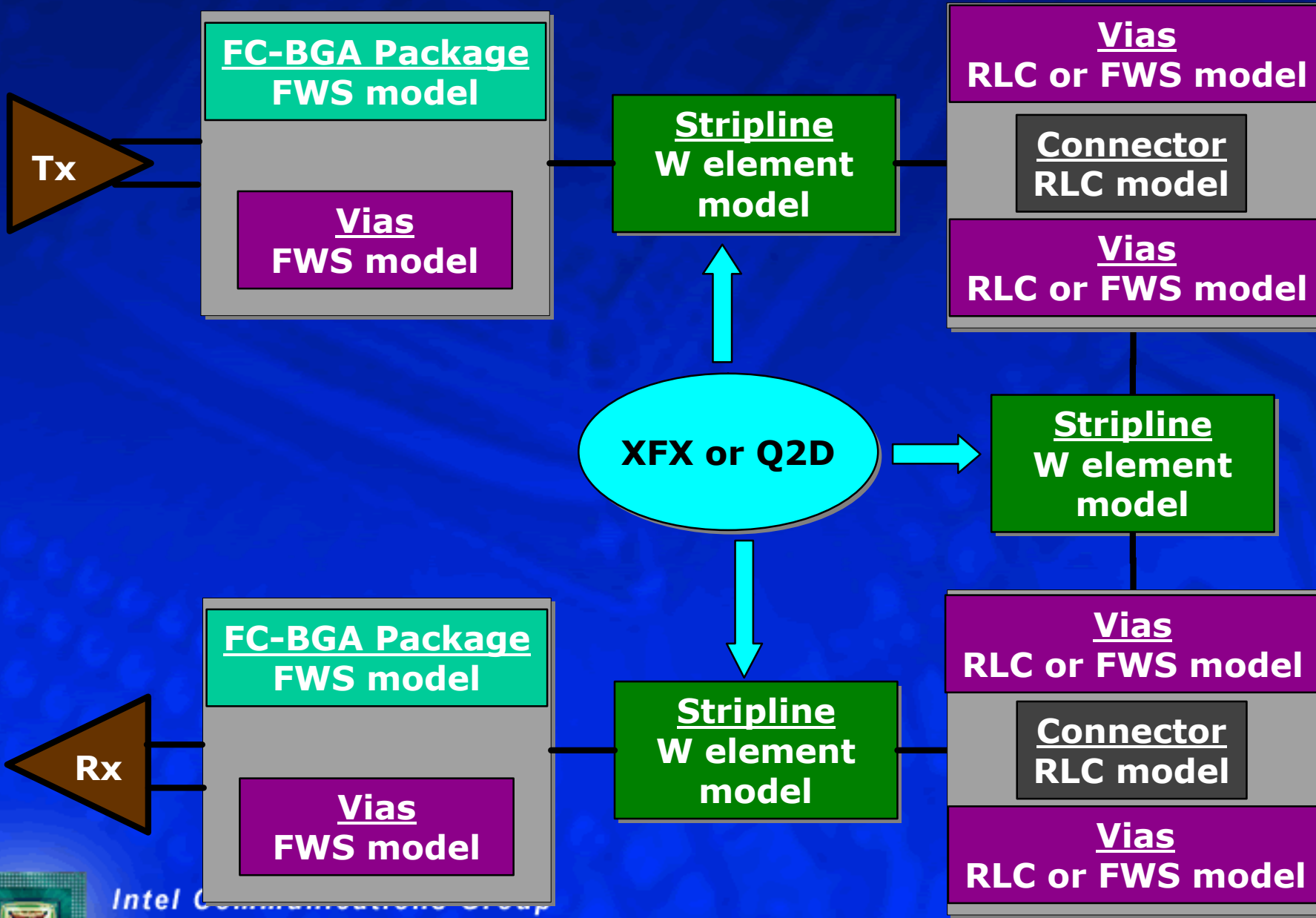
Channel Simulation Flow



Alternate Simulation Flow (Dispersion analysis)

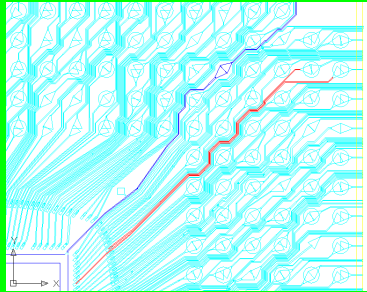


FWS / Hspice Flow

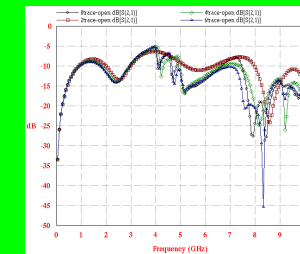


Full wave spice model creation and simulation process

Physical model of the package



Fullwave EM Field Solver

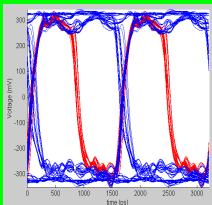


S-parameters

Ansoft HFSS Full Wave SPICE Conversion

Models for the rest of the channel

Package performance in the time domain



Hspice transient simulation

Hspice model (frequency look-up table)

```
* BEGIN ANSOFT HEADER
* node 1 port1_model
* node 2 port1_model_ref
* node 3 port2_model
* node 4 port2_model_ref
* Format: Star-HSPICE
* Model: Full-wave Spice
* Type: Sparam
* Project: p:/maxwell/config/partsub/filter20g.sp
* Notes: Created by Ansoft
* Left: 1 2
* Right: 3 4
* END ANSOFT HEADER

.subckt filter20g 1 2 3 4

Ginc1 0 b1 a1 2 0 02
Finc1 0 b1 Uam1 1.0
Rt1 b1 0 1.0

Ginc2 0 b2 a2 4 0 02
Finc2 0 b2 Uam2 1.0
Rt2 b2 0 1.0

Uam1 1 a1 dc 0.0
Rref1 a1 2 50
```

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