

ELECTRICAL MODELING FOR HIGH FREQUENCY IC PACKAGE DESIGNS

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ELECTRICAL DESIGN NEEDS

- Package Electrical Information needed by the Die Designer:
 - Parasitic parameters: Inductance, Capacitance, Resistance
 - Spice equivalent circuit
 - Crosstalk information (Signal-to-Signal and Power-plane-to-Signal)
 - Power-supply bump/collapse (Ground-bounce, Voltage droop)
 - Package Resonant frequencies
 - Signal Reflections
- Package Electrical Information needed by the Board/Card Designer:
 - Same as Die Designer
 - Include Die Electrical Information (e.g., combined Spice model)
- The Information needed can be determined by either Building/Testing the Package or by 3D Computer Simulation of the Package

SKIN-DEPTH

in Copper as a Function of Frequency

Table 1

<u>Frequency</u>	<u>Skin Depth</u>
1 MHz	67
100 MHz	6.7
500 MHz	2.9
1 GHz	2.1
5 GHz	1.3
10 GHz	0.9
	microns

SKIN-EFFECT

on Copper Trace 10 x 0.05 x 0.02 mm in Air

Table 2

<u>Frequency</u>	<u>Inductance</u>	<u>Resistance</u>
1 MHz	12.3	0.17
100 MHz	12.1	0.25
500 MHz	12.0	0.47
1 GHz	11.9	0.72
5 GHz	11.9	3.62
10 GHz	11.9	5.96
	nH	Ohm

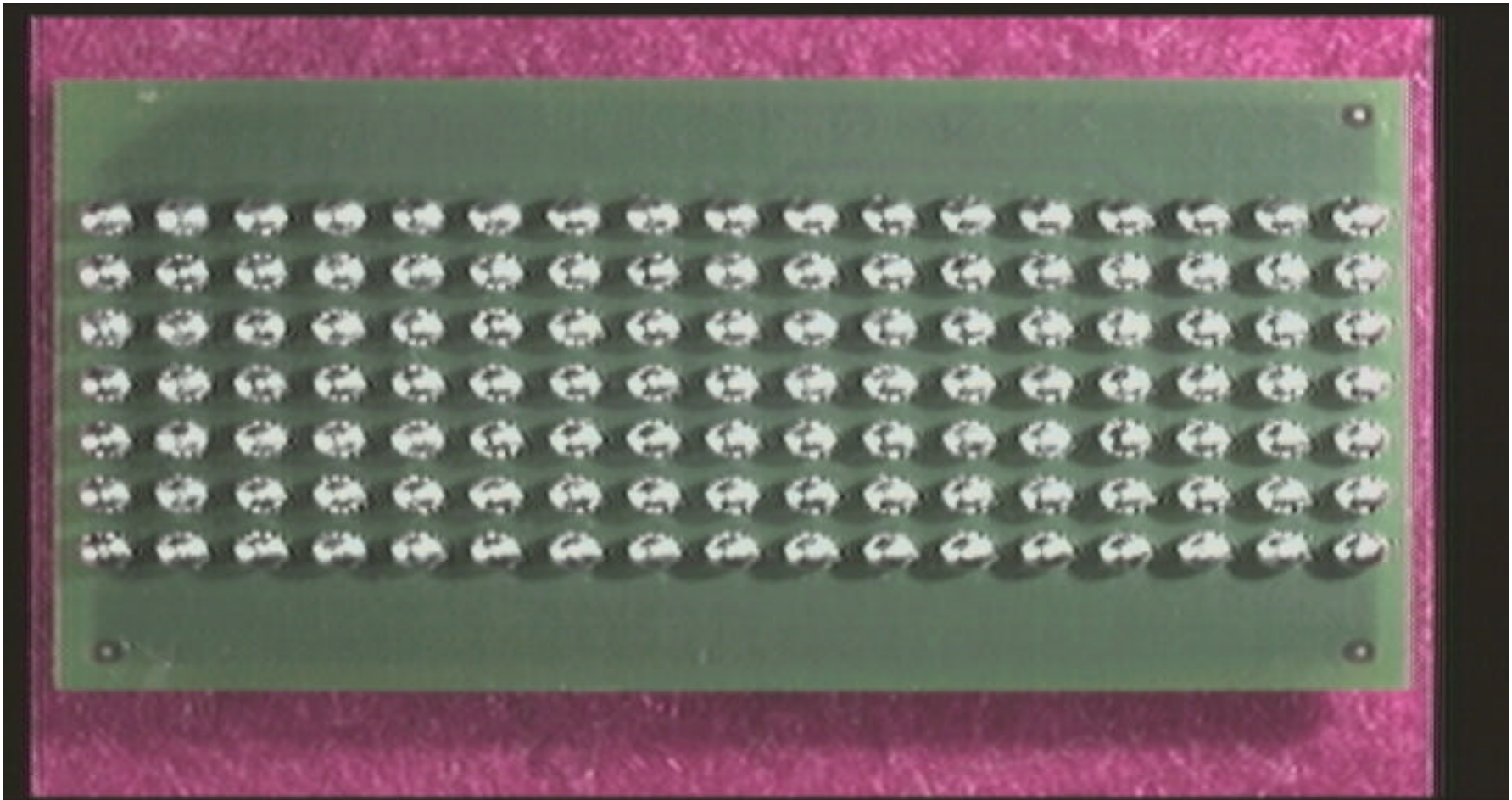
256KX36 SRAM PINOUT

-- Top-half only --

Table 3

	A	B	C	D	E	F	G	H
1	VDDQ	NC	NC	DQ21	DQ24	VDDQ	DQ19	DQ25
2	SA14	NC	SA15	DQ20	DQ22	DQ23	DQ18	DQ26
3	SA11	SA13	SA12	VSS	VSS	VSS	SBWc	VSS
4	NC	NC	VDD	ZQ	SS	G	NC	NC
5	SA10	SA9	SA8	VSS	VSS	VSS	SBWb	VSS
6	SA7	SA6	SA5	DQ15	DQ13	DQ12	DQ17	DQ9
7	VDDQ	NC	NC	DQ14	DQ11	VDDQ	DQ16	DQ10

119 PINS IBM PBGA



--- INDUCTANCE --- SIMULATION VS TEST

Table 4a

PIN	NAME	MicroBGA Simulation	MicroBGA Test	PBGA Simulation	PBGA Test
A2	SA14	4.4	4.5	4.2	4.2
A3	SA13	4.3	-	4.2	-
A5	SA10	4.4	4.1	4.2	4.1
A6	SA7	4.2	-	4.1	-
B3	SA13	3.5	-	4.0	-
B5	SA9	3.3	3.0	4.0	3.8
B6	SA6	3.4	-	3.8	-

--- INDUCTANCE --- SIMULATION VS TEST

Table 4b

PIN	NAME	MicroBGA Simulation	MicroBGA Test	PBGA Simulation	PBGA Test
C2	SA15	2.7	2.5	2.8	2.5
C3	SA12	3.4	-	3.0	-
C5	SA8	3.3	-	3.0	-
C6	SA5	3.2	-	3.1	-
D1	DQ21	3.9	4.1	3.3	3.3
D2	DQ20	3.7	3.4	3.1	2.9
D6	DQ15	3.5	-	3.3	-

--- INDUCTANCE --- SIMULATION VS TEST

Table 4c

PIN	NAME	MicroBGA Simulation	MicroBGA Test	PBGA Simulation	PBGA Test
G2	DQ18	3.1	-	3.3	-
G6	DQ17	3.0	-	3.4	-
G7	DQ16	3.2	-	3.3	-
H1	DQ25	3.0	-	3.1	-
H2	DQ26	2.9	-	3.1	-
H6	DQ9	2.9	2.9	3.0	2.9
H7	DQ10	2.8	2.7	3.0	3.0

MY NEXT ASSIGNMENT

- I have been working on Memory-Device Package Analysis
- I will be working on ASIC, Logic, Microprocessor Package Analysis:
 - Larger Die (2-3X larger)
 - Larger number of Metal Planes (typically 2-5, instead of 1-2)
 - Larger Pin-counts (typically 500 – 2000, instead of <100)
 - Higher Frequency (>5 GHz, instead of <1 GHz)
- I will need:
 - Package Design Tool input (e.g., **Cadence Package Designer**, APD file)
 - Distributed Model PEEC Tool (**TPA**) for analysis of Signal conductors
 - Full-wave Analysis Tool (**Ensemble, HFSS, SI Wave**) for analysis of Signal conductors at 5 GHz and higher
 - Full-wave Analysis Tool (**SI Wave**) for analysis of Power-plane conductors and high frequencies

GREATER HIGH FREQUENCY CONCERNS

- As Wave-lengths reduce to package pattern dimensions (@ 5 GHz , $\lambda/10 = 5 \text{ mm}$), each trace becomes a radiating antenna :
 - Radiated energy = **signal loss**
 - Radiated energy = **interference on other electric conductors**
 - Radiated energy = **damage to living organisms**
- Alternative means of conduction will have to be used, when these factors become dangerous:
 - Shielded conductors (conductor surrounded by Ground conductor)
 - Wave-guides
 - **Light strands**
- **Full-wave Analysis will become absolutely necessary**

SUMMARY

- IC Package ***Electric Characteristics*** are becoming more important as Frequency increases
- ***Computer Simulation*** of these electric characteristics will save money and more importantly time for delivery of High Performance parts
- Package pin counts require ***Package-Design System Input***
- ***Ansoft TPA*** has proven to be a ***Good***, distributed-model, electric, parasitic parameters, ***Analysis Tool***
- As frequencies reach farther into the GHz range, ***Full-wave Analysis*** will become necessary