

High-Frequency Simultaneous Switching Output Noise (SSO) Simulation Methodology For a DDR333/400 Data Interface

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Abstract: As interface data rate increases, SSO prediction becomes a crucial issue for high-speed system signal integrity design. This paper describes a noise simulation methodology based on a DDR333/400 data interface. For increased accuracy, a convolution simulation methodology is proposed and discussed, which uses transistor-level SDRAM buffer model, lumped on-die power bus model, non-ideal ground/power S-parameter TSOP2 package model extracted by Ansoft HFSS, DIMM power distribution model measured by VNA, and a lumped DIMM connector model. The results show good correlation with Time Domain (TD) measurement. Noise sensitivity analysis and impact on system signal integrity is included. Through the analysis, optimum on-die decoupling capacitance and DIMM power distribution design are suggested.

Introduction

As system bandwidth increases, power and ground distribution for high-speed systems becomes critical. In particular, minimizing simultaneous switching noise output (SSO) from chips and maximizing decoupling between power planes becomes crucial for achieving maximum system bandwidth. As the data rate exceeds a few hundred MHz, high-frequency system SSO simulation is one of the major factors to predict system signal integrity. To date, many studies on power delivery modeling in system-level have been done [1][2]. However, an accurate and efficient high-frequency system SSO simulation methodology has not been reported because of the complexity of the system power distribution and the difficulty to generate accurate high-frequency models including buffer, package, board, and connector.

This paper describes a high-frequency, above 1GHz bandwidth, SSO noise simulation methodology for a DDR333/400 Data Interface. For greater accuracy, a transistor-level buffer model, a lumped on-die power bus model, a non-ideal ground and power S-parameter package and a DIMM power distribution model, and a lumped DIMM connector model are used. In addition, an S-parameter convolution simulation methodology is proposed and discussed to improve simulation accuracy and efficiency. The non-ideal power and ground S-parameter model of a TSOP2 package is generated by Ansoft HFSS up to 1GHz. The S-parameter model of DIMM power

delivery system is measured by HP8753ES Vector Network Analyzer (VNA) up to 1GHz. Consequently, the methodology is demonstrated by comparing with SSO measurement on a DDR333 DIMM.

Based on the proposed methodology using S-parameter and transistor-level models and convolution simulation, we discuss noise sensitivity through time-domain SSO simulation. In addition, SSO impacts on propagation delay and signal quality are demonstrated by using eye-diagram simulation of electronic design automation (EDA) software. Considering SSO impacts on system signal integrity, optimum on-die decoupling capacitance and DIMM power distribution design are suggested for a DDR400 Data Interface.

Figure 1 represents current SSO issues on DDR333 SDRAM x8SS DIMMs during read cycle. Three types of DIMM are measured by using the Tektronix TDS 649C with 3-GHz bandwidth. The SSO noise is measured at Vddq (data bus power) to Vssq (data bus ground) TSOP2 package pin nearby DQ58. As can be seen from Figure 1, as the number of buffers on x-axis increases, the peak-to-peak SSO noise on y-axis increases. For 9-bits toggling including 8-bits data signal (DQ) and 1-bit strobe signal (DQS), the peak-to-peak noise exceeds 400mV in the case of DIMM A, generating the worst SSO. DIMMs B and C provide relatively smaller SSO noise because of relatively lower inductive ground and power plane and/or better decoupling capacitor placement on the DIMMs. The x8SS

DIMM B has ground flooding on layer 6. On the other hand, DIMM C x8SS has power plane flooding on layer 6. Moreover, as can be expected, 64bits toggling becomes worse. Based on time-domain noise measurement, we can expect that the maximum Vddq to Vssq noise is more than 600mV.

Signal integrity is greatly affected by the SSO noise as shown in Figure 2. The figure shows SSO noise impacts on propagation delay and signal quality. This is a case of DDR400 DIMM (type A), TSOP2 package, and without on-die decoupling capacitor. The data signal is corrupted, which has 576ps propagation changes for eye diagram simulation.

When a driver at a chip is switching, SSO noise appears on the power plane as shown in equation 1. SSO noise is a function of effective inductance (L_{eff}), switching voltage (V_{p-p}), slew rate (SR), switching frequency (F_{sw}), and interconnection capacitance (C_{int}). As L_{eff} , V_{p-p} , SR, F_{sw} , and C_{int} increase, SSO noise increases, and vice versa.

$$\begin{aligned} \Delta V &= L_{eff} \frac{\Delta i}{\Delta t} = L_{eff} \frac{\Delta(C_{int} \cdot V_{p-p} \cdot F_{sw})}{\Delta t} \\ &= L_{eff} \cdot C_{int} \cdot F_{sw} \frac{\Delta V_{p-p}}{\Delta t} \\ &\approx L_{eff} \cdot C_{int} \cdot F_{sw} \cdot SR \end{aligned} \quad (1)$$

$$\Theta i = C_{int} \cdot V_{p-p} \cdot F_{sw} \text{ with capacitive load}$$

Where, L_{eff} : Effective Inductance
 C_{int} : Interconnect Capacitance
 V_{p-p} : Switching Voltage
 F_{sw} : Switching Frequency
SR : Slew Rate
 ΔV : SSO Noise
 i : Switching Current
 Δt : Time Period

Based on the basic theory, two possible ways to reduce SSO noise are as follows. The first is to reduce L_{eff} by using decoupling capacitor. In this case, obtaining the optimized number of decoupling capacitors and their placement is very important. In addition, the usage of on-PCB and on-die decoupling capacitors should be applied for efficient noise reduction. For example, the on-die decoupling capacitor is effective for high-frequency noise because of the low parasitic inductance. By contrast, for

mid- and low-band frequency noise, an off-die decoupling capacitor is better because of the relatively high value and large parasitics, especially ESL. The second method is to reduce slew rate (SR) of a buffer output signal. The SR can be controlled by changing the transistor size of pre-drivers.

Models and Simulation Methodology

The simulation procedure to investigate high-frequency noise is as follows:

1. Decide the target frequency bandwidth considering noise frequency;
2. Generate frequency-dependent accurate models such as S-parameter model obtained with 3-D full wave EM simulator (HFSS) or VNA measurement;
3. Finally, simulate the time domain noise at Vddq to Vssq based on convolution simulation using EDA software. For this simulation, low-frequency S-parameter models have to be considered carefully, especially the DC value.

We used transistor-level SDRAM buffer model with BSIM 3 process parameters, lumped on-die power bus model, non-ideal ground/power S-parameter TSOP2 package model extracted by Ansoft HFSS, DIMM power distribution model measured by HP8753ES VNA, and lumped DIMM connector model as depicted in Figure 3. For increasing simulation accuracy over 1 GHz bandwidth, S-parameter model based convolution simulation is recommended. S-parameter model provides frequency-dependent characteristics including skin effect and dielectric conductance effect. Compared to lumped PI-network model and N-section ladder, as frequency increases, the S-parameter model becomes even more accurate. In addition, the S-parameter-based convolution simulation method is easy to apply for SSO noise prediction contrary to plane modeling based simulation through Partial Element Equivalent Circuit (PEEC) method or FDTD. Moreover, for high-frequency SSO simulation, transistor-level buffer model gives more accurate result compared to IBIS 3.2 model.

As can be seen from Figure 4, the SSO result through S-parameters based convolution simulation (thicker line in Figure 4a) shows good correlation with TD measurement

(Figure 4b). This shows DQS switching case with DIMM B. The noise waveform is obtained at package Vddq to Vssq TSOP2 package pin nearby DQ58. In the case of 100pF decoupling capacitor per each buffer, peak-to-peak noise is 61mV. By contrast, 50pF case shows 121-mV peak-to-peak noise. Measured peak-to-peak noise is 84mV. In addition, as on-die decoupling capacitor value increases by 50pF, SSO noise is reduced by 50% as shown in Figure 4 (a).

Sensitivity Analysis

This section describes sensitivity study of read SSO noise for a DDR333 data interface. Table I shows the great importance of having on-die decoupling capacitors per each DQ/DQS buffer on the SDRAM devices since having 50pF can reduce the read SSO noise by 50% as compared to without decoupling capacitor. The sensitivity analysis shows that the predominant parameters are: firstly, on-die decoupling capacitors, secondly, DIMM power distribution, and thirdly, package or on-die power bus inductance per mm. Through this analysis, we can decide this value as the minimum value for DDR400 specification.

Figure 5 (a) shows measured noise of DDR333 and DDR400 for the DIMM A. As can be seen from the graph, as switching frequency of buffer increases 400MHz, SSO is increasing 5% to 10%. For whole byte 7 toggling, SSO noise on DDR 400 is almost 400mV. Figure 5 (b) demonstrates SSO noise spectrum of DDR333 with worst pattern 101010. The major components are 333MHz as the second harmonic of the data signal, 167MHz as the fundamental frequency, 500MHz as the third harmonic, and 666MHz as fourth harmonic. For the DDR400, we could expect that the major components are 400MHz, 200MHz, 600MHz, and 800MHz. In comparison with the dark dotted line of 50-pF decoupling capacitor per each buffer, the light dotted line represents that on-die decoupling capacitor is effective for high-frequency noise reduction as shown in Figure 5 (b).

Figure 6 shows Vddq to Vssq peak-to-peak noise versus slew rate for DDR400. The solid lines are linear trend lines for 50pF, 100pF, and 150pF decoupling capacitor per each buffer, which are generated from simulation results with different slew rate for DDR400. Based on this, we can decide the required minimum on-die decoupling capacitor versus the maximum output slew rate,

the higher the output slew rate into specified test fixture, the higher the required on-die decoupling capacitor value ranging from 50pF per DQ/DQS buffer for below 1V/ns SR up to 200pF per DQ/DQS buffer for more than 4V/ns and less than 5V/ns SR.

Proposed DIMM

SSO noise affects timing and signal quality as can be seen from Figure 9. As discussed in the previous section, DIMM power distribution has a crucial impact on the SSO noise. A design rule to minimize loop inductance is essential. Figure 7 shows a top-view photo of the proposed hybrid x8SS DIMM that is mixed of x8SS DIMM B and x8SS DIMM C. The SSO noise on x8SS DIMM B could be reduced by lowering the plane inductance through ground flooding on layer 6. In addition, x8SS DIMM C has the advantage of power distribution with low loop inductance by placing decoupling capacitors between SDRAM chips as shown in Figure 7. As can be seen from the box, the hybrid DIMM has five 0.1 μ F capacitors at each Vddq to Vssq.

Figure 8 shows simulation result of peak-to-peak SSO noise on the proposed DIMM with 9 buffers toggling. Using the proposed DIMM with 100pF on-die decoupling capacitor per each buffer, we can obtain less than 250mV peak-to-peak noise compared to the DIMM A case.

Signal quality and propagation delay is affected by SSO noise as shown in eye-diagrams of Figures 9 (a) and (b) which are in the case of DIMM A. Figures 9 (c) and (d) are from the proposed hybrid DIMM. Figures 9 (a) and (c) show 100pF on-die decoupling capacitor case, and eye-diagrams of Figures 9 (b) and (d) are the case of 150pF on-die decoupling capacitor. For DIMM A with 100-pF on-die decoupling capacitor, we can see 330ps delay changes and poor signal quality. For 150pF on-die decoupling capacitor, the propagation delay change is 199ps. By contrast, the hybrid DIMM provides much smaller propagation delay and excellent signal quality for 100pF as well as 150pF. The propagation delay changes of 100pF and 150pF-decoupling capacitor per each buffer are showing only 74ps and 59ps, respectively.

Conclusions

S-parameter interconnection model and transistor-level buffer model based SSO convolution simulation has been demonstrated based on a DDR333/400 data interface. The simulation methodology was demonstrated by showing the correlation between simulation and measurement. Through noise sensitivity analysis of a DDR333 interface, on-die decoupling capacitor and DIMM power distribution has been investigated as the most important factor for reducing SSO noise. Noise impacts on system signal integrity have been studied. Consequently, optimum on-die decoupling capacitance versus slew rate and DIMM power distribution design for a DDR400 interface have been suggested.

Acknowledgement

The authors would like to thank Mohammed Mostofa, Paul Yang, and Sam Baer, of Intel Corporation, for their TD SSO noise and VNA measurements.

References

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3. Jaya Bandyopadhyay, "Power Distribution Modeling and Decoupling of Multilayer Printed Circuit Board", *Proc 8th Topical Meeting on Electrical Performance of Electronic Packaging*, 1999, pp. 103-106.

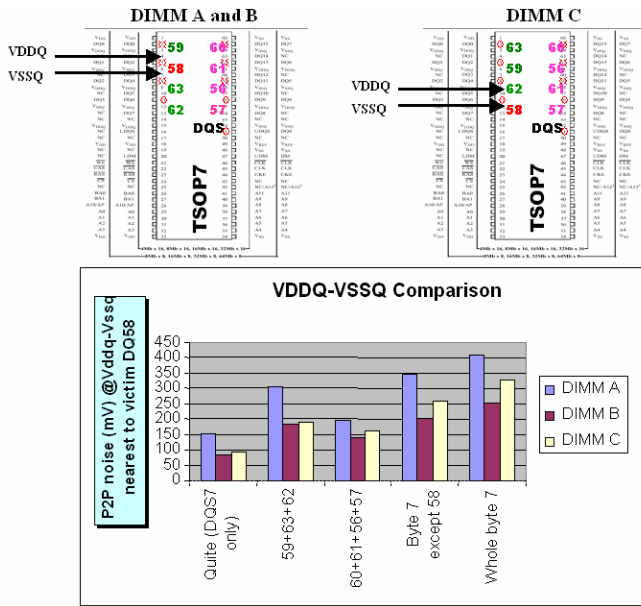


Figure 1. Current noise problem on the DDR SDRAM DIMMs during read cycle.

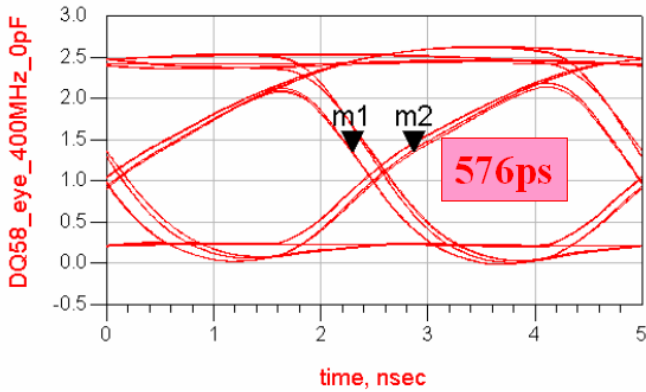


Figure 2. Eye-diagram affected by SSO noise

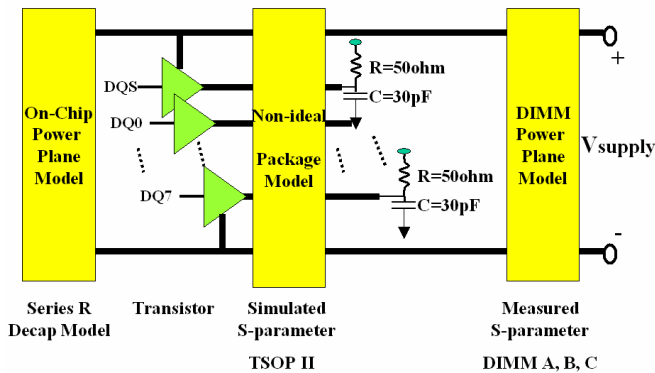


Figure 3. Models for high-frequency SSO simulation.

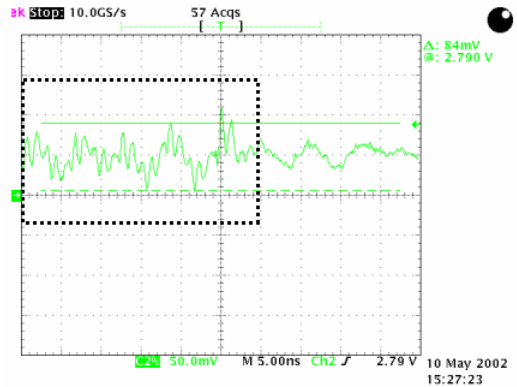
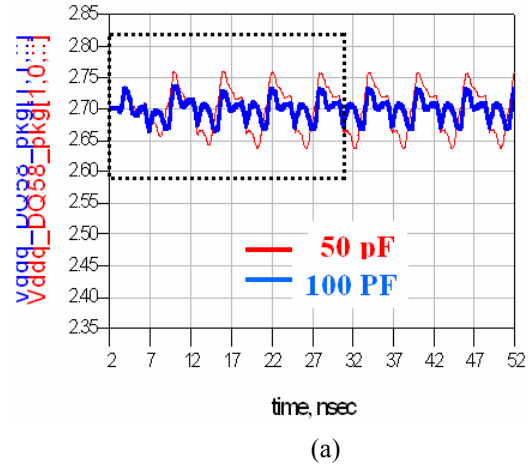
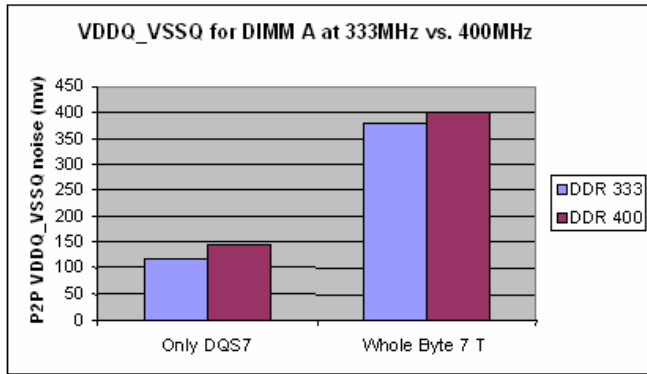


Figure 4. SSO noise correlation between (a) simulation result through S-parameters and transistor buffer model based convolution simulation and (b) time-domain measurement.

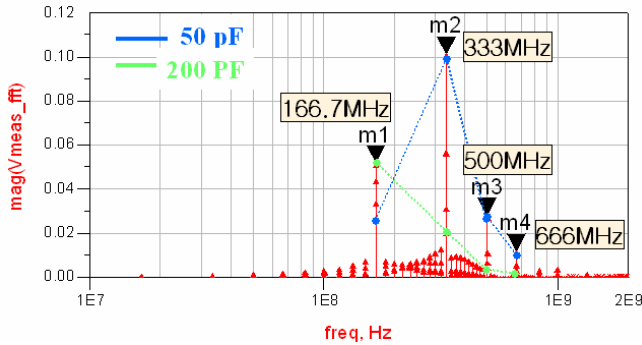
On-Die Cap	On-Die PWR/Inductance	TSOP2 PK/G	DIMM (JEDEC)	DIMM Conn (5rH)	P2P Noise on Die Pad (Vddq-Vssq)
50pF	Non-ideal	Non-ideal	Ideal	Ideal	63mV
50pF	Non-ideal	Non-ideal	Non-ideal	Ideal	168mV
50pF	Non-ideal	Non-ideal	Non-ideal	Non-ideal	165mV
0pF	Non-ideal	Non-ideal	Non-ideal	Non-ideal	310mV
50pF	Ideal	Non-ideal	Non-ideal	Non-ideal	130mV
50pF	Non-ideal	Ideal	Non-ideal	Non-ideal	149mV

1. On-die Decoupling Cap, DIMM Power Distr.: ~150mV
2. DIMM Power/GND Distribution: ~100mV
3. On-Die Inductance of Power Bus: ~30mV
4. Package Effect: ~16mV
5. DIMM Connector: ~3mV

Table I. Sensitivity study of read SSO noise for DQS switching only in a DDR333 data interface.

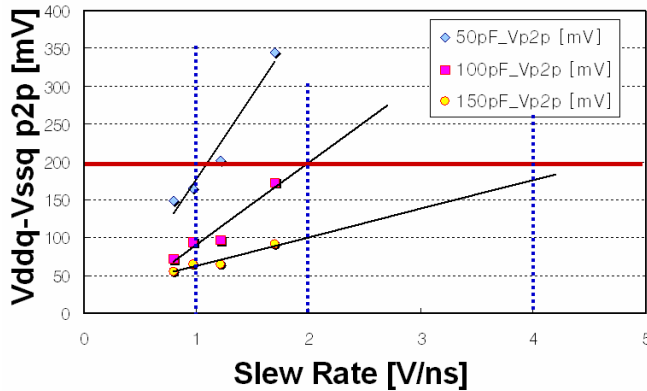


(a)



(b)

Figure 5. (a) Measured noise of DDR333 and DDR400 on the DIMM A. (b) SSO noise spectrum of DDR333 with worst pattern 101010.



MAX OUTPUT SLEW RATE OF DQ/DQS BUFFERS	MIN ON-DIE CAP PER DQ/DQS BUFFER
4~5V/ns	200pF
2~4V/ns	150pF
1~2V/ns	100pF
~1V/ns	50pF

Figure 6. Required minimum on-die decoupling capacitor value versus maximum output slew rate for DDR400.

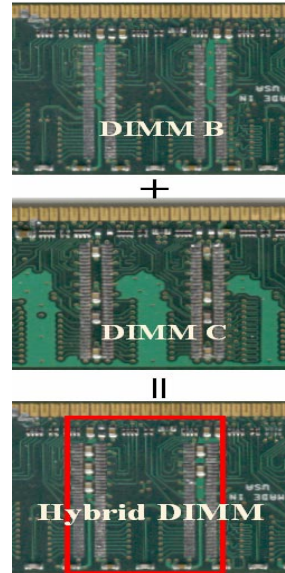


Figure 7. Top-view photo of the proposed hybrid DIMM that is mixed of DIMM B and DIMM C.

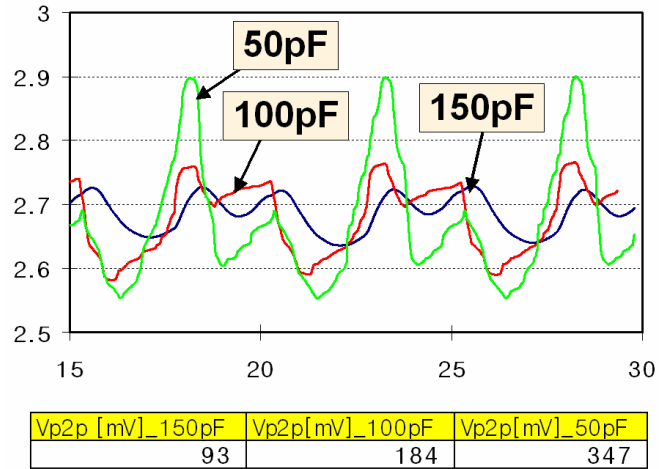


Figure 8. Peak-to-peak SSO noise on the proposed DIMM with 9 buffers toggling.

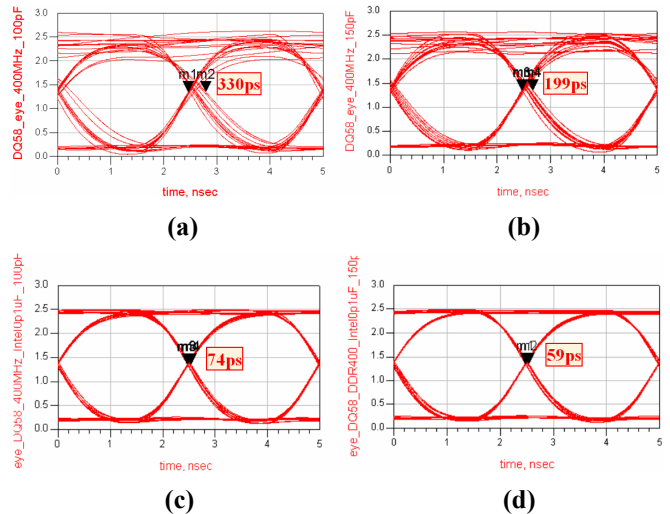


Figure 9. Eye-diagrams affected by SSO noise of DIMM A with (a) 100pF and (b) 150pF and the proposed DIMM with (c) 100pF and (d) 150pF.