

Simulations in Guiding Gpbs PCB Design of Communication Systems

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Abstract

This paper describes how to effectively use CAD tools for SI and EMI analysis at 2.5Gbps to 12.5Gbps, and how different CAD tools to be involved in high speed PCB design process. It discusses providing design rules on board stack-up, predicting loss and its compensation using SpecctraQuest; validating device models and performs power/ground analysis for de-coupling capacitor selection and placement using Hspice; and obtaining accurate geometry parameters of special trace structures using Maxwell 2D and 3D field solver and Spicelink and HFSS. Successful design cases show how design goals are achieved at every stage. The result provides guidance to designers in meeting difficult technical requirements and in reducing testing cycles and part costs.

I. Introduction

As high speed board designs become more and more complicated in communication systems, it has been realized that there is no single CAD tool can complete the entire simulation work with acceptable accuracy. Printed circuit board (PCB) designers and signal integrity (SI) engineers are provided with a variety of simulation tools nowadays to perform difficult design tasks. Cost and performance (speed and accuracy) are always the main criteria in choosing the desired tool set. However, it has been less discussed how to use an existing CAD tool set (from multiple EDA software suppliers) to achieve successful design goals and satisfy SI rules and EMI regulations.

In general, a good combination for design and SI / EMI analysis should include a layout tool, a thorough board level simulator, an accurate field solver, and a detailed simulation engine. This paper presents how multiple simulation tools to be properly used in providing solutions for Gigabit per second (Gbps) PCB designs in high speed communication systems that transfer data at 2.5Gbps to 12.5Gbps through cards and backplanes. The set of tools consists of Cadence Allegro, Cadence SpecctraQuest, Avant! Hspice, and Ansoft Spicelink and HFSS, with the reasons explained as follows. Allegro is a popular layout tool today. SpecctraQuest is used as the board level simulator because of its identical database with Allegro, which eliminates data translation problems. Hspice is the detailed analysis tool to perform more accurate simulations when necessary. Spicelink and HFSS provide 2D and 3D field solutions on various interconnect geometries (vias, connectors, etc.), especially when high frequency analysis is required. With these tools, this paper describes how SI and EMI engineers give design rules on board stack-up and loss prediction using SpecctraQuest, validate device models and perform power/ground analysis for de-coupling capacitor selection and placement using Hspice, and obtain accurate geometry parameters of special trace / component structures using Maxwell 2D and 3D field solver. The paper shows that in order to use an existing set of CAD tools effectively, each of the tools has to be employed at the right design stage and to solve the problems it is created for. The analysis results not only provide guidance to designers in meeting difficult technical requirements, but also in reducing testing cycles and unnecessary cost in parts selection. A standard procedure is also presented to integrate simulation in high speed board design process.

II. Using SpectraQuest to provide design rules

Allegro is a widely used layout tool in industry today. SpectraQuest, therefore, becomes a natural choice in board level simulation. The combination of these two has the advantages of sharing the identical library, employing same simulation engine, and using similar graphic user interface. As Allegro and SpectraQuest are integrated further, engineers will have more freedom to perform layout and simulation at the same time during design cycles.

Successfully transferring the signals of 2.5Gbps serial data, with 100ps-200ps edge rates, over cards and backplanes requires understanding the important SI issues at these frequencies and managing them effectively. Some of the major points to consider include skin effect, dielectric loss, crosstalk, and driver pre-emphasis. SpectraQuest can simulate and address these issues.

1. Using SignalExplorer for pre-layout analysis and for critical net extraction

As boards become more and more complicated, pre-layout analysis and design rule setup become more and more important. One advantage with SpectraQuest is its schematic extraction tool, SignalExplorer, which can perform pre-layout analysis considering circuit parameter variation and can extract critical nets into the circuit viewer for examination at the routing and post-layout stage. Like many other board level simulators, one of disadvantages with SpectraQuest is the lack of detailed modeling ability, in other words, IBIS model is the only type of device model that can be used. Therefore, reliable behavioral models have to be evaluated prior any analysis in SignalExplorer. We have been using SignalExplorer in the following problems: evaluate board stack-up including trace geometries; estimate losses due to skin effect and dielectric loss; and give design rules on allowable trace length for high speed data / clock, on spacing to control cross-talk, on termination selection in types and values, and on maximal length mis-match with all differential pairs. Our experience shows that the design rules obtained from above simulations provide engineers with valuable guidance to layout and routing, which can significantly reduce design cycle and risk of ill-performed boards.

2. Losses and compensation

Skin effect and dielectric loss are often mentioned as the major issues in Gigabit data transmission. Skin effect impacts the line widths used, whereas dielectric loss impacts the materials used to construct the PCB. To accurately model the two effects, board level simulator has to be able to handle lossy transmission lines with frequency dependent parameters. SpectraQuest satisfies this requirement. Simulation and measurement results show that dielectric loss at GHz ranges is dominant. In communication systems, high speed data are often transferred over long traces, which can be greatly degraded by dielectric loss. One commonly used method to overcome such loss is equalization / pre-emphasis. Although there are different equalization methodologies available, we will discuss the circuit with passive elements only. Since most of devices having equalization circuit built in, it is difficult for the IBIS type of models to address the compensation. The approach simulating equalization effect we used is to separate a passive equalization circuit from its device and put it on the board level. By analyzing the modified netlist with SpectraQuest, we obtained the general guidelines for equalization applications.

First of all, an equalizer should not be functioning when dielectric loss is not significant. It is only designed to compensate losses of high frequency components over long interconnects. Pre-emphasis may result in worse eye patterns for shorter interconnects. As interconnects become longer and longer, dielectric loss in FR4 is more and more significant. The higher frequency portion of the signal (corresponding to the sharp rise/fall edges) disappears, but the slower portion is reserved. To use pre-emphasis effectively, one must first estimate the length of interconnect that the signal will propagate through, then decide if compensation should be employed. Having pre-emphasis on for all interconnect lengths at the higher data rates may not be optimal.

Table 1 compares the eye openings and jitters with and without pre-emphasis for a 2.5Gbps signal propagating through different interconnect lengths.

Table 1 Eye openings and jitters with and without pre-emphasis

Configuration #	Description	Eye Opening (mV)	Jitter (ps)
1	Direct to scope, pre-emphasis off	584	22
2	Direct to scope, pre-emphasis on	220	35
3	10", pre-emphasis off	395	32
4	10", pre-emphasis on	224	38
5	20", pre-emphasis off	348	42
6	20", pre-emphasis on	224	30
7	30", pre-emphasis off	230	70
8	30", pre-emphasis on	214	36
9	60", pre-emphasis off	Closed	NA
10	60", pre-emphasis on	132	34

3. Crosstalk rules at GHz ranges

Crosstalk has been a major factor consuming noise margin in PCB designs with data rate lower than Gbps. Since crosstalk consists of more higher frequency components than the aggressive signal, it suffers even more severe loss than the original signal in the Gbps range, reducing its impact on the noise budget.

Most layout tools estimate crosstalk according to the coupling coefficients calculated from trace geometry and materials. This normally results in a linear estimation formula that limits parallelism, thereby reducing routing density. In reality, crosstalk gets saturated over long traces. Ignoring the saturation effect in estimation gives routing rules much tighter than necessary. Full simulation is therefore performed with SpectraQuest to determine crosstalk rules for our designs. For 2.5Gbps data, the rise time is typically about 150ps, and saturation length of about 300 mils. This means that coupled traces can actually be routed longer than 300mil without increasing crosstalk budget.

Table 2 shows the crosstalk saturation and loss for a 2.5Gbps signal with 500mv swing and 110ps rise time. It is clear, from the table, that the crosstalk gets saturated around 300-400mils, and its amplitude decreases over long traces because of the loss. Making use of what is revealed here allows designers to route traces more efficiently than many layout tools suggest.

Table 2 Crosstalk saturation and its loss

	0.2" coupled length	0.5" coupled length	1" coupled length	8" coupled length
8mil separation	8mv	13mv	13mv	11mv
10mil separation	5mv	9mv	10mv	9mv

III. Using Maxwell 2D/3D solver in complicated trace structures

1. Using Maxwell 3D solver in complicated trace structures

For transferring higher data rate at 10 to 12.5Gbps, FR4 introduces great loss. Other material with better loss quality is needed. A coplanar structure, as shown in Figure 2, is employed to transmit 10-12.5Gbps data on the top of the board in one of our designs, using RO4350 material. This material has much lower

loss-tangent in dielectric, but needs to be manufactured only on top/bottom layers to keep the overall cost down. This results in transferring 10GHz signals with microstrips. Coplanar provides better chance to ensure signal quality and to limit EMI level. A 3D field solver is necessary to calculate the trace width and separation to achieve 50Ω line impedance, matching the driver's output impedance. Maxwell 3D solver from Ansoft is employed here. Figure 1 is an illustration of the co-planar structure.

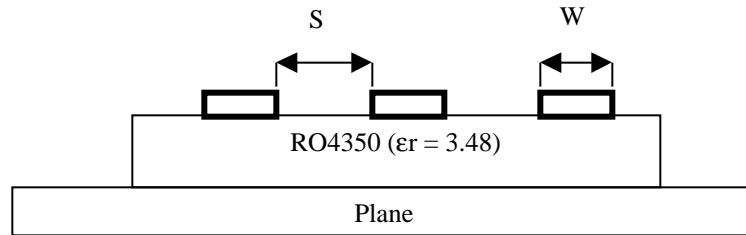


Figure 1 Coplanar structure

2. Modeling connectors

Vias, connectors, and associated stubs result in signal integrity problems at Gbps data rate. Accurately modeling and simulating connector and via effects become important in predicting signal quality. Maxwell 3D solver is used to extract connector models of VHDM and HSD. The connector models are then imbedded in SpectraQuest DML format as Hspice sub-circuit for board level simulation. While small Gbps cards are successfully designed, designing backplanes used to transfer data at 5-10Gbps remains challenging. Maxwell field solver helps create connector models for such data rates.

IV. Using Hspice in detailed analysis

1. Using Hspice in power plane analysis

Power delivery faces new challenges at frequencies over GHz range. It requires detailed modeling technique and analysis to obtain true plane responses. Hspice is a tool that can perform detailed frequency sweeping analysis and also has transistor based IC models when simultaneous switching noise (SSN) is interested. We will mainly discuss the issues in this section when dealing with planes that deliver power to high frequency differential parts.

To evaluate power/ground plane behavior at high frequency, a transmission line mesh model can be used [2]. In this example, a PCB with a pair of 2" x 2.5" power/ground planes is analyzed. The plane's separation is 4.5mil. With 70ps of edge rate, 5GHz bandwidth is required. Target impedance is pre-calculated as 272mΩ for a single plane pair, based on the parameter specification of one major differential part. The transmission line mesh is used to determine the plane's response in frequency domain. Analysis was done for the lossless and lossy cases to determine the impact of adding dielectric loss into the model, which is generally recommended for data rates over 1Gbps. Although loss tangent is frequency dependent, a constant value of 0.022 was used in the model for simplicity. The model was submitted to Hspice for simulation. The resulting resonance frequency is 1.2GHz (see Figure 2), which can be verified by analytical solution. Simulation results show that the resonant amplitude is reduced greatly by incorporated dielectric loss into the plane model, which helps the frequency response of the planes to meet the target impedance.

This pair of planes is specially designed for differential signals running at 2.5Gbps since most of the high speed serialized data is transmitted differentially. Ideally, differential parts will draw zero transient current because of the differential feature of the parts. In reality, this also means much more lenient (i.e. higher) target impedances can actually be allowed, and should be considered to minimize costly over-design by driving up PCB layer count unnecessarily.

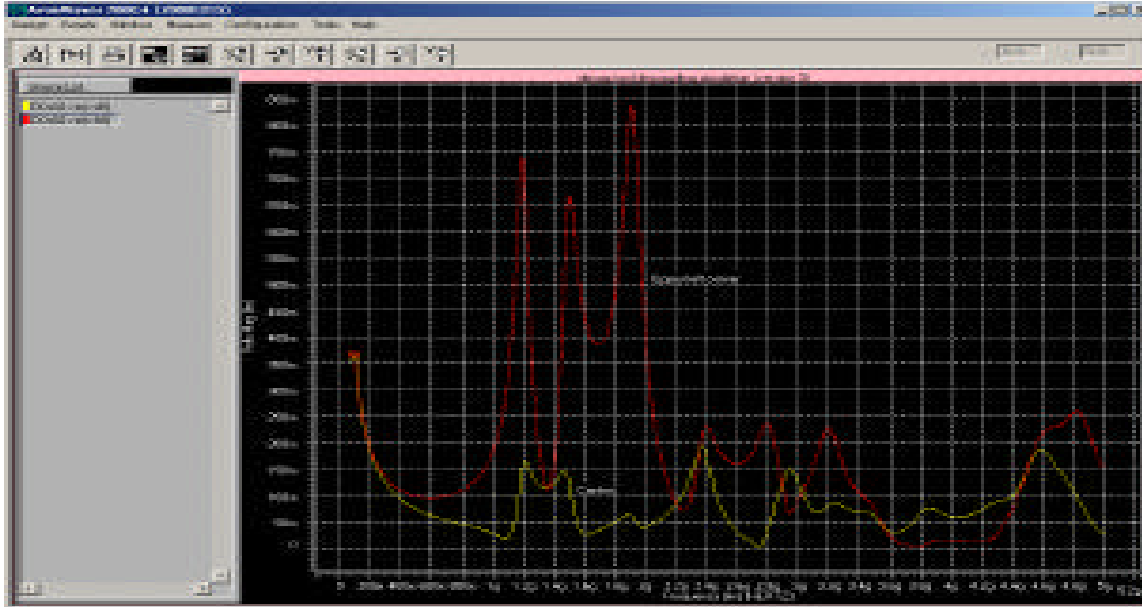


Figure 2 Plane responses

2. Using Hspice in component evaluation and higher frequency analysis

Although IBIS models are widely used on board level simulations, analysis with transistor based driver/receiver models is crucial in new component evaluation. As IC manufacturers provide transistor-based models more often in Hspice encrypted format, Hspice becomes the sole tool performing evaluation. Such simulation should include the cases with and without package effects, and with the device's driving transmission lines in different types and lengths. The manufacturer co-operation in providing correct models and making modifications in real parts are required as well. When the part is determined, IBIS models can be created and verified based on the results of the finalized Hspice model and function specification.

At even higher signal rates, such as 10-12.5Gbps, behavioral models may no longer be valid. There should be no attempt to make IBIS models for devices operating at these frequencies. Hspice is again used to simulate the special signal nets transferring such data.

V. Design and process with simulations

1. Successful designs

Using the above studies and SI guidelines, we have successfully designed boards transmitting and receiving 12.5Gbps data, and the boards transferring 2.5Gbps data to 40Gbps devices.

2. High speed PCB design process with simulation

We have discussed in details how CAD tools are used to solve different design problems. One aspect that normally gets ignored is when these tools should be applied during high speed designs. Reliable and efficient designs are only achieved when CAD tools are involved at the right design stages. Therefore, a standard procedure as follows is necessary to integrate simulations during design process.

- a. SI model development with Hspice and SpectraQuest;
- b. Stack-up and trace model development with Maxwell and SpectraQuest;
- c. Decoupling capacitance power plane analysis with Hspice;

- d. Floorplanning, layout specification, pre-routing analysis, and post-routing verification with SpecctraQuest.

To execute this procedure effectively, SI and EMI education is needed to hardware engineers and management.

VI. Conclusions

This paper addresses the problem, that many engineers face today, on CAD tool usage effectively in high speed PCB designs. There is no single tool performing all required simulations with acceptable accuracy. One should also avoid using a tool in an application that the tool is not designed for. This paper demonstrates how to take advantage of a set of available CAD tools and how to timely apply them to different parts of a design. The design rules for the data rate over Gbps, obtained with the simulation results provided by such tools, give crucial guidelines in high speed board designs to meet the system complexity and tight release schedules. A standard process that integrates high speed simulation into design cycles is also needed to guarantee successes.

References

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