

# The Impact of Split Power Planes on Package Performance

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## Abstract

The purpose of this study is to assess the impact of the split power planes on package performance. A non-custom package with 16 power plane splits is studied from the perspective of plane noise, trace impedance and trace crosstalk. 2D and 3D simulations are performed on the package using selected sections of the package. The plane noise is found not to be significant when there is either low or high driver transient current demand. In the low current demand case, current is primarily confined to the region of the plane beneath the trace and the transient plane voltage is small. In the high current demand case, guidelines are given to minimize the impact of the split planes. Among these guidelines, a minimum trace to plane split distance should be maintained such that the effective inductance is not increased. 2D simulations are performed to examine the impact of the split plane on the signal trace impedance. Signal trace impedance is found to vary depending on its proximity to the plane split. The impact of the plane splits on the signal trace crosstalk is investigated. Capacitive coupling between traces is reduced by distancing the signal trace from the plane split. 3D simulations using a subsection of the multiple split plane package are performed. Plots showing the near end and far end crosstalk for five traces distributed about a plane split are included. Crosstalk is found not to increase for traces bordering the plane split as long as a minimum trace to plane split distance is maintained.

## 1. Introduction

Non-custom, generic packages can have the advantage of lower cost and faster design cycles when compared with custom package designs. Often the advantages of non-custom packages must be weighed against the restrictions placed on the package by routing rules, the signal-to-ground ratio and power plane splits. In considering whether a non-custom package solution offers an acceptable level of performance for a given application, a number of package electrical parameters need to be scrutinized including I/O timings, signal trace impedance, and power delivery.

This paper resulted from a study which considered using a non-custom package to support a 0.18  $\mu\text{m}$  custom ASIC. The non-custom package is a 6-layer ball grid array (BGA) with 16 power plane splits. The purpose of the split planes is to provide configurable supply voltages for the die. This particular ASIC required only two supply voltages. A custom package solution with only two plane split would be ideal but at higher cost. The power structure consists of split planes on the third and sixth layer from the top. The package employs flip-chip technology to connect the die to the substrate. The ground plane is solid. The edge of the plane split is placed 60  $\mu\text{m}$  from the center of the nearest signal trace.

The splits are 100  $\mu\text{m}$  wide.

This paper specifically looks at the impact of the multiple power plane splits in a non-custom package on package performance. In particular, the impact on plane noise, trace impedance and crosstalk is examined.

## 2.1 Simultaneous Switching Noise

Transient current demands from switching drivers will generate power and ground noise that is proportional to the effective inductance. Effective inductance is defined as the inductance of the path through which the current passes. There are two primary paths which the current can take depending on the switching conditions. The first path results from a low-to-high transition, where the path consists of the power and signal leads (see Figure 1). The current path is shown for this case. The effective inductance for this case can be calculated using:

$$L_{lh} = L_p + L_s - 2M_{ps} \quad (1)$$

where  $L_p$  is the partial self inductance associated with the power lead,  $L_s$  is the partial self inductance associated with the signal lead and  $M_{ps}$  is the partial mutual inductance between the power and signal. The second path results from a high-to-low transition, where the path is formed by the signal and ground leads (see Figure 1). The effective inductance for this case can be calculated using:

$$L_{hl} = L_g + L_s - 2M_{gs} \quad (2)$$

where  $L_g$  is the partial self inductance associated with the ground lead and  $M_{gs}$  is the partial mutual inductance between the ground and signal. In both cases, the effective inductance is a loop inductance not a partial inductance. The power plane switching noise generated by either case is given by:

$$V_{noise} = L \frac{di}{dt} \quad (3)$$

where  $L$  is the effective inductance for either switching case. Of the two switching cases, only the low-to-high case involves the inductance of the power lead,  $L_p$ . Additional power plane splits will therefore primarily impact the low-to-high switching case.

There are two switching scenarios which bound transient current demand. The worst-case switching condition occurs when all drivers switch either low-to-high or high-to-low. This produces a high transient current demand ( $di/dt$ ). The best-case switching condition occurs when only a single

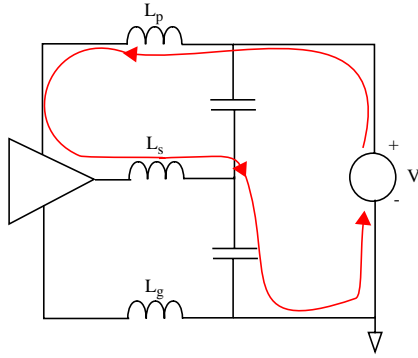


Figure 1. Switching current path for the low-to-high transition.

driver switches either low-to-high or high-to-low, producing a low transient current demand.

In the low transient current demand scenario (best case), only a single driver switches. There are two primary reasons why a multi-split plane will perform similarly to a solid power plane for best-case despite the differences in the number of power plane splits. First, since only a single driver is switching the overall transient current demand is low and therefore the resultant noise on the plane will be small. Second, the current redistribution that occurs as the frequency increases will cause the current to flow in a narrow strip of the power plane closest to the signal trace. Consequently, only the vias nearest to the signal trace will be utilized in the current return path. Figure 2 shows a plot of the AC surface currents at 100 MHz. Ansoft Maxwell Q3D was used for the simulation. The top level ground plane is hidden to show the surface currents on the power plane. The figure shows that the current density in the power structure is maximum underneath the signal trace and on the via closest to the signal ball. This current return path will minimize the loop inductance and impedance at high frequencies.

In the high transient current scenario, all drivers draw current simultaneously. As with the single driver switching case, the current for each driver will be confined to the current return path which minimizes the loop inductance. This will result in the current returning underneath the signal trace and on the via closest to the signal ball. For a multi-split power plane to behave equivalently to a solid power plane in the high transient current case, the packages need to have a high degree of similarity in terms of their construction and design rules. The packages should share the following in common: 1) The signal via and power via should be at the same distance. This insures that the loop area is constant. 2) The signal traces should not cross split planes. This prevents current from taking a circuitous return path which would increase the loop area. 3) The plane and via dimensions should be the same. 4) The ratio of IO's to power and ground balls and vias should be maintained. 5) The current sinks at the balls should be equivalent. That is, the current return path through all of the power and ground balls are the same. This means that the PCB and decoupling capacitors should have a high degree of symmetry from the package perspective. If this is not the case then there may be a preferred current return path.

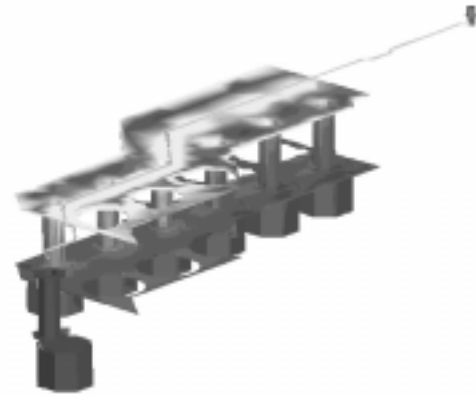


Figure 2. AC surface currents on power plane with a single signal trace. The ground plane is hidden.

In addition to these general construction and design rule considerations, attention should also be paid to the minimum signal trace to power plane split distance for the multi-split plane package. This distance is important because if the signal conductor is routed too close to the plane edge then the current distribution on the plane will be altered. Figure 3 shows the approximate distribution of high frequency current density in the power plane with 1 A of current. (The distribution is assumed to be symmetric about the y-axis.) The signal trace is located 35  $\mu\text{m}$  above the power plane. The x-axis specifies the distance from the center of the signal trace. At lower frequencies the current distribution can be much broader. The current density falls off in intensity with the square of increasing distance [1]. The graph shows that to minimize the impact on the current distribution the split should be located as far as possible from the signal trace. Routing rules need to specify the minimum distance the trace should be routed from the split. If the trace is routed conservatively far from the split then routing density is sacrificed. Therefore, careful estimates of the minimum tolerable signal to plane split distance are needed. Subsequent sections will analyze the impact of placing the split plane at various distances from the signal trace.

Next, the impact of the power plane split on the effective inductance is examined. A parametric simulation was performed using Ansoft Maxwell 2D. The accuracy of the simu-

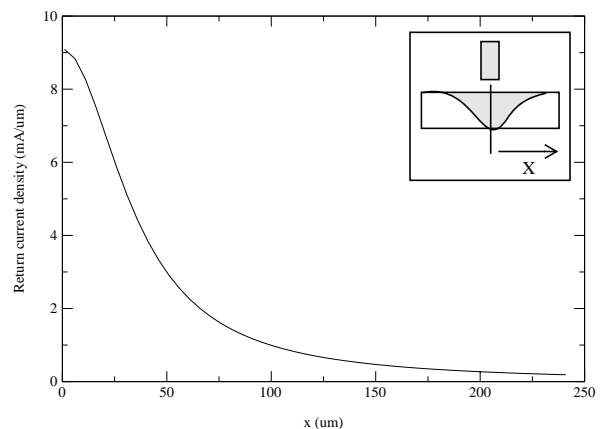


Figure 3. Approximate current density distribution on the power plane centered about a signal trace.

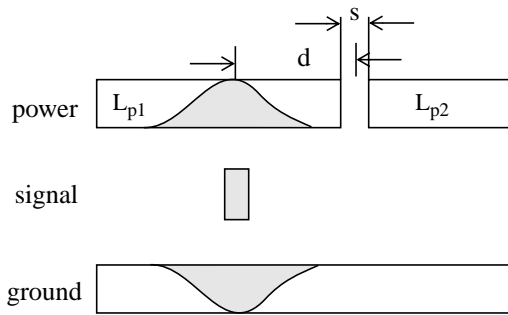


Figure 4. Test structure used for impedance and inductance simulations.

lation was set to 0.3%. The frequency of the extraction was set to 1 MHz. Frequency dependent effects were not considered. Unless otherwise stated, these simulation conditions were followed for all subsequent simulations. Figure 4 shows the test structure that was used for the simulation. All relative distances were fixed except the distance,  $d$ , which was swept from 0 to 300  $\mu\text{m}$ . The distance is specified from the center of the signal trace to the center of the plane split. The effective inductance, given by (1), was calculated from the partial inductance matrix as a function of the signal to plane split distance.

Figure 5 shows the results from the simulation. There are two current return paths shown (see Figure 4). With the split located directly above the signal trace ( $d = 0$ ), the current can choose to return through either path and the loop inductance will be nearly the same. As the split moves further away there are two distinct current return paths. The first current return path, through the  $L_{p2}$  conductor, is less favorable because of the high loop inductance. The effective inductance of the  $L_{p2}$  path continues to increase as the  $L_{p2}$  conductor moves further away from the signal conductor. The second current return path through the  $L_{p1}$  conductor is the preferred current return path at high frequencies. The effective inductance of this path drops off sharply with distance. With a distance of 100  $\mu\text{m}$ , the effective inductance is reduced by about 17% compared with the split located directly above the signal trace ( $d = 0$ ). The loop inductance using a stripline configuration is shown for reference and offers the lowest effective inductance. At distances greater than 100  $\mu\text{m}$ , the  $L_{p1}$  path inductance remains relatively constant, asymptotically approaching that of a stripline. The arrow on the x-axis indicates the location of the split plane on the non-custom package. This shows that at this distance the effective inductance will not significantly increase because of the presence of the plane split.

## 2.2 Signal Trace Impedance

The signal trace impedance can be modified by the splits in the power plane. Traces that are routed between the power and ground planes, in a dual-referenced stripline configuration, will have a different impedance than traces routed near the split plane where the impedance approaches that of a single-referenced (just ground) microstrip.

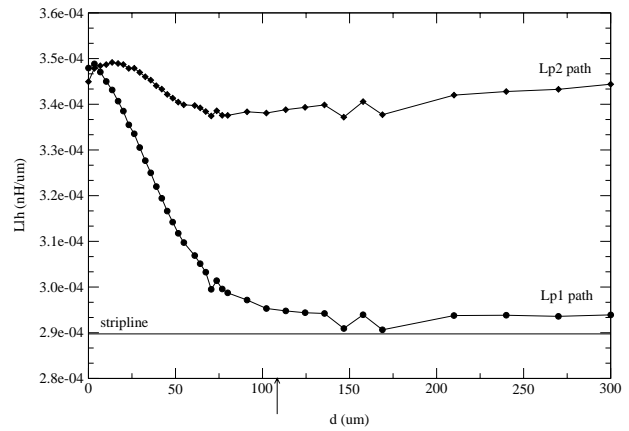


Figure 5. Effective inductance for low-to-high transition. Two current paths are shown.

The impact of the plane splits on the signal trace impedance was studied using the test structure shown in Figure 4. A parametric simulation was performed using Ansoft Maxwell 2D. All relative distances were fixed except the distance,  $d$ , which was swept from 0 to 300  $\mu\text{m}$ . As before, the distance is specified from the center of the signal trace to the center of the plane split. The impedance of the signal trace was measured as a function of the signal to plane split distance.

Figure 6 shows the results from simulation. Three plane split distances were simulated: 60  $\mu\text{m}$ , 100  $\mu\text{m}$  and 150  $\mu\text{m}$ . The non-custom package has a 100  $\mu\text{m}$  plane split distance. The family of curves shows that as the plane split moves far away from the signal trace the trace impedance approaches that of a stripline. With the plane split located immediately above the signal trace the trace impedance approaches that of a microstrip. Furthermore, the graph shows that larger plane splits exhibit greater impedance swings. Larger plane splits also require that the split be located farther from the signal trace for the split not to impact the trace impedance. For the non-custom package plane split distance of 100  $\mu\text{m}$ , the impedance starts at about 52  $\Omega$  with the split located directly above the signal trace ( $d = 0$ ). The impedance is reduced by about 10% at a distance of about 100  $\mu\text{m}$ . At greater distances the impedance is relatively constant. The arrow on the

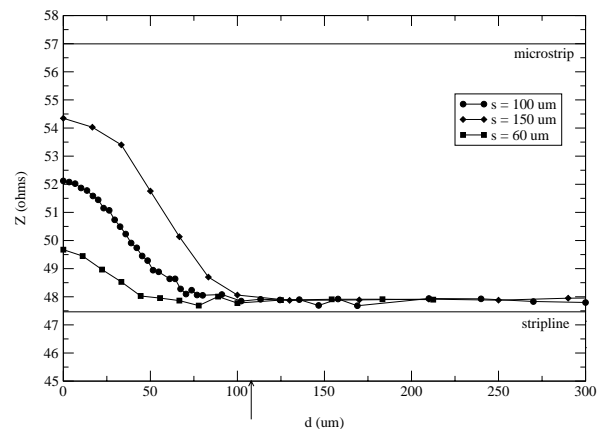


Figure 6. Trace impedance as a function of trace to split distance shown for three different plane splits.

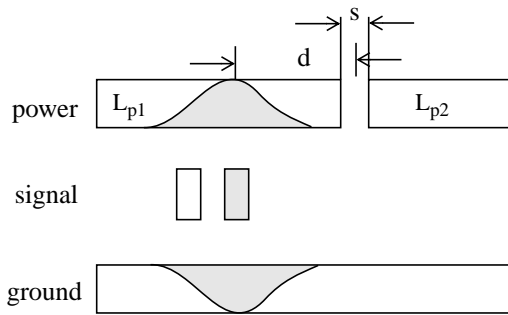


Figure 7. Test structure used for crosstalk analysis.

x-axis indicates the location of the split plane on the non-custom package. At this distance the trace impedance will not be significantly modified by the presence of the plane split.

### 2.3 Crosstalk

Crosstalk between signal traces can be affected by the split in the power plane. In general, although the total capacitance tends to be a fixed quantity, coupling capacitance is more sensitive to perturbations [2]. Consequently, traces neighboring the plane splits may exhibit more coupling capacitance and hence more crosstalk than traces that are routed over a solid power plane. The impact of the split plane on crosstalk was studied using the test structure shown in Figure 7. A parametric simulation was performed using Ansoft Maxwell 2D. All relative distances were fixed except the distance,  $d$ , which was swept from 0 to 200  $\mu\text{m}$ , using the same convention for distance. The second signal trace is placed 30  $\mu\text{m}$  from the primary trace. The coupling capacitance between the signal traces was measured as a function of the signal to plane split distance

Figure 8 shows the simulation results. The graph shows that the coupling capacitance,  $C_{\text{coup}}$ , between the signal traces is decreased as the distance increases.  $C_{\text{coup}}$  is reduced

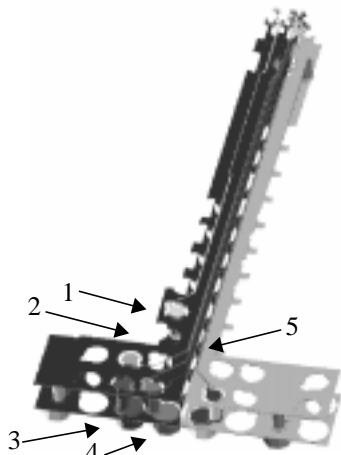


Figure 9. A subsection of the multiple plane split package used for crosstalk simulations.

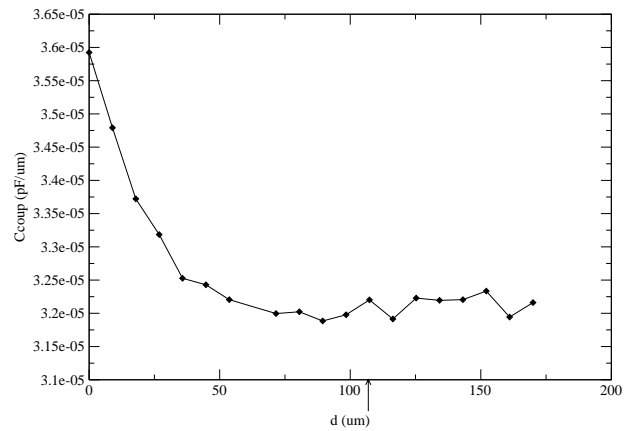


Figure 8. Coupling capacitance between neighboring signal traces.

by about 10% by placing the plane split at a distance of 75  $\mu\text{m}$ . The arrow on the x-axis indicates the location of the split plane on the non-custom package. At this distance, the coupling capacitance has significantly decreased. This shows that the capacitive crosstalk will not be enhanced by the presence of the plane split.

Finally, a subsection of multi-split plane package was extracted using Ansoft Maxwell Q3D (see Figure 9). The ground plane is hidden to show the trace routing and power plane split. The subsection includes five traces gathered around the power plane split. Traces 1-4 are located above a single power plane and trace 5 is located above a separate power plane. A SPICE model was generated from the simulation data and the circuit was simulated using HSPICE. The package circuit model was connected as it would be in an ASIC environment including a mock IO driver, trace termination and connections to the PCB. Simulations were performed with trace 4 switching, the neighboring nets quiet, and the crosstalk was observed on the neighboring traces on the near and far end.

Figure 10 and Figure 11 show the far and near end waveforms, respectively. The results show that the magnitude of the total crosstalk (inductive and capacitive) at the bump and ball of the package circuit model scale with the aggressor-victim distance. For example, traces 2 and 3 exhibit the largest crosstalk and they are the two closest

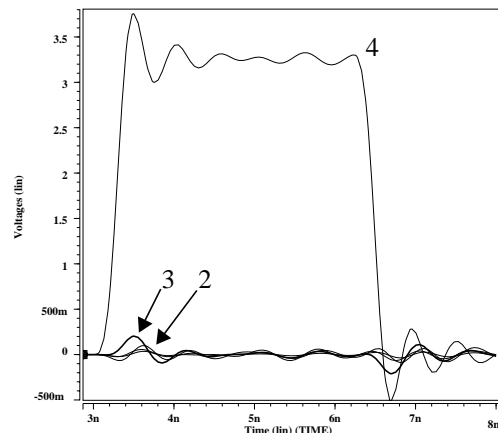


Figure 10. Far end crosstalk for five coupled traces distributed about a plane split.

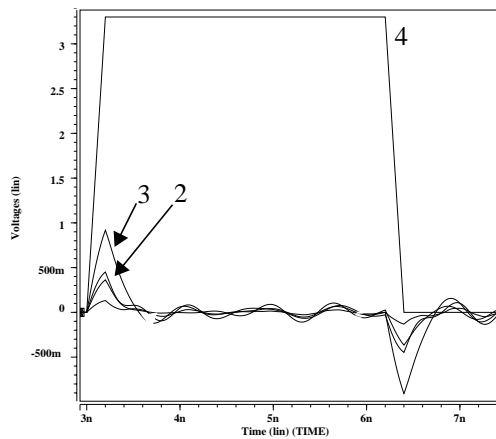


Figure 11. Near end crosstalk for five coupled traces distributed about a plane split.

traces to the aggressor. This indicates that the presence of the split plane did not alter the tendency of crosstalk to increase with decreasing aggressor-victim distance.

### Conclusions

This paper examined the impact of power plane splits on several performance criteria including plane noise, trace impedance variation and crosstalk. It was shown that a minimum trace to plane split distance should be maintained to not alter the current distribution on the power plane. The ASIC supplier's standard, multi-split plane package considered here provided a sufficient signal to plane split distance. These results show that properly implemented, multi-split plane package designs do not necessarily sacrifice performance.

### Acknowledgments

The author would like to thank Keith Newman, Istvan Novak, and Bidyut Sen for kindly reviewing this work and offering many excellent suggestions. The assistance of Ed Fulcher in obtaining packaging specifications and databases is appreciated.

### References

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