New planar field solver for very large and very small structures

New algorithm offers designers the ability to simulate large planar electromagnetic problems on their PC.

By Lawrence Williams, Ph.D., Brian Gray, Tony Donisi, and Richard Hall, Ph.D.

Have you heard this before? "Electromagnetic field solvers are only useful for simulating simple discontinuities or isolated components like filters or single element antennas." Most circuit and antenna designers have lived with that reality ever since the first planar field solvers were commercialized some ten years ago. Circuit designers who include electromagnetic (EM) simulation in their design process have had to contend with partitioning their layouts into regions that will be simulated using circuit simulator distributed models and regions that will be simulated using an EM field solver. Of course that partitioning is based on the designer's experience and circuit assumptions. Antenna designers would analyze just a few patch elements of a large phased array antenna hoping that mutual coupling was insignificant. The reason is simple: the EM solvers were either too slow when simulating large structures, or were simply unable to solve them because they ran out of core memory. The only viable option is to specify overly-cautious design rules.

Ansoft recently announced Ensemble Version 7.0 with a new solver technology breakthrough called SVD FastSolveä. The new algorithm, based on singular value decomposition (SVD), is a patented technology that allows engineers to simulate truly gigantic planar EM problems on a PC or workstation. It is now possible, for example, to simulate an entire MMIC layout in a single EM field simulation project, or a complete planar phased array antenna. Designers no longer have the partitioning dilemma; if multiple components are closely-spaced, simply place all of them into Ensemble and hit solve.

Another issue has been the frequency range over which a full-wave field solver is valid. New loop-tree methods make EM field solvers inherently stable at low frequencies (or equivalently, for electrically small geometries). This is particularly important for broadband communication applications where structures on-chip or on PCB boards are expected to perform at Gigabit per second data rates.

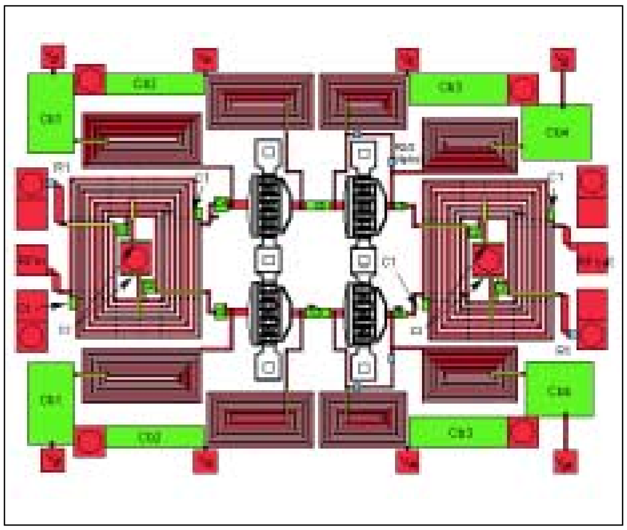

Figure 1. MMIC layout for 2.4 GHz balanced low noise amplifier

This article surveys the use of Ensemble for electrically large and electrically small structures. It begins with a summary of commercial EM field solvers and a brief discussion of the new SVD FastSolve technology and the loop-tree methods. The technology is applied to a low noise amplifier (LNA) design to capture the electromagnetic behavior of the full layout. Solver performance is discussed and high-frequency electric currents are illustrated. The technology is also applied to a large, 16 x 16 element planar phased array antenna. Also, a broadband receiver image reject filter on a multi-chip module (MCM) silicon substrate is simulated to illustrate the stability of the new loop-tree methods for electrically small structures. Comparison with measured results is given.

SVD FastSolve Technology

There are several commercial planar EM field solvers, including Ansoft Ensemble, that are based on the method-of-moments (MoM) technique. They can run out of gas when analyzing large problems for two reasons. First, memory requirements go up with the square of the problem size (double the problem means four times as much memory). Second, the time required to solve the MoM matrix equation goes up with the cube of the problem size.

The practical result is that these tools cannot easily go beyond a certain problem size that results in about 5000 unknowns. Ansoft's SVD FastSolve incorporates Lucent–Bell Labs patented fast solver technology for high-speed and wireless component design. This technology employs a matrix compression algorithm based on singular value decomposition (SVD) that extends by 10X or more the size and complexity of structures that can be analyzed. Ansoft added a matrix pre-conditioner, advanced loop-tree methods, 3D planar full-wave Green's functions, and efficient matrix fill algorithms to round out the SVD FastSolve technology. For large problems, Ensemble's memory and processing requirements have linear growth (n log(n)) rather than quadratic or cubic. This all adds up to an Ensemble solver that can simulate designs that are simply too large for traditional methods. Indeed, it is now possible to solve over 30,000 unknowns accurately and efficiently.

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2.4 GHz MMIC LNA full-layout EM simulation

Figure 1 depicts a MMIC LNA circuit layout that was created in Ansoft's Serenade Design Environment using the UMS 600um (8x75um) PHEMT. The balanced design provides exceptional match and power handling across a significant bandwidth. The input match of a typical LNA is poor due to the necessity of providing a noise match to the amplifier, which does not lend itself to exceptional input matching. Balancing the amplifier cures this problem, with the penalty of added noise figure due to the loss inherent in the hybrid circuitry. An additional benefit is a 3 dB increase in power handling and third-order intercept (TOI) performance. Power combining is achieved using a pair of spiral couplers with integrated thin film capacitors.

The transistor was defined by small signal s-parameter device data. The parameterized layout cell is assigned to the s-parameter black-box element in the schematic. Although the FET layout was not solved using Ensemble, including its footprint in the layout will ensure proper spacing. Initial design parameters were calculated and simulated with the design targeting an operating frequency of 2.4 GHz. In that region, the desired performance included a noise figure of less than 3.0 dB, greater than 16 dB gain, and a return loss below 15 dB. Since it is a balanced design, the parameters will be relatively independent of the source or load impedance, which is a very desirable characteristic.

The spiral couplers were originally modeled in Serenade with sections of Harmonica's multi-coupled line element (MCPL) based on the proprietary full-wave spectral domain algorithm. This advanced model helps ensure that critical line coupling due to adjacent and non-adjacent lines is accounted for in the circuit model. The corners were constructed in Serenade, but simulated separately in Ensemble for greater accuracy. To minimize die space, thin film capacitors were placed inside the spiral couplers. The overall chip size is approximately 2mm X 1.5mm (80 mils X 60mils).

A unique feature of Ensemble is the ability to insert s-parameter black box elements into the electromagnetic simulation. This feature was exploited to simulate the Phemt devices and the thin film capacitors, including those used in the spiral couplers. The Ensemble model has 26 black boxes for the thin film capacitors and six thin film resistor elements. Further complexity of the electromagnetic model includes 10 spiral inductors, 10 vias to ground, and 18 airbridges.

Electromagnetic simulation was performed from 2 to 4 GHz. The model had 3,436 triangular elements with 4,029 unknowns in the MoM matrix equation. Simulation time was 50 minutes per frequency on a 750 MHz, Pentium III computer with 512 Mbytes RAM. Simulations result in an S-parameter block which may be imported back into Harmonica for circuit simulation and comparison with the distributed models. Figure 2 is a plot of current on the circuit traces.

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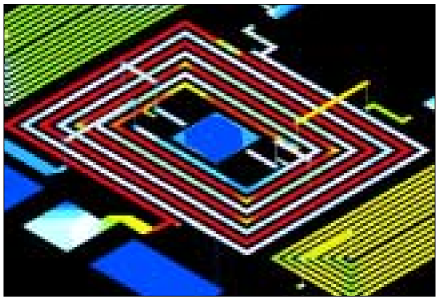

Figure 2. Full-wave electric currents in the MMIC layout.

16 x 16 element planar phased array antenna

Figure 3 is a snapshot of a 16 x 16 element planar patch array antenna as viewed in Ensemble [1]. The structure has a corporate feed to excite each of

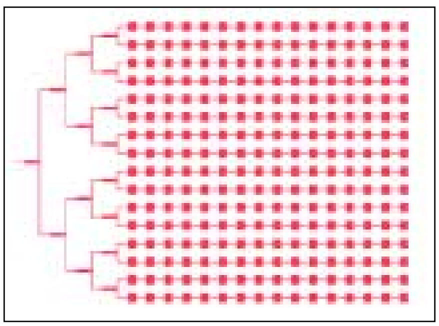

Figure 3. 16 x 16 element planar phased array in ensemble EM simulator.

the 16 rows of the antenna; each row is resonantly fed. Simulations were performed at 9.42 GHz. The Ensemble model had 34,420 triangles and 47,770 unknowns in the MoM matrix equation. Simulation time was eight hours, 40 minutes per frequency on a 400 MHz PC. Peak RAM required was 781 Mbytes. The SVD FastSolve algorithm compressed this problem to reduce

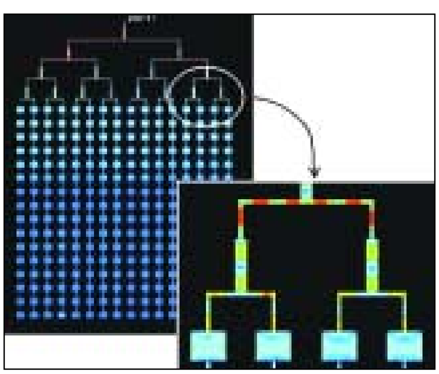

Figure 4. Full-wave electric currents in the 16 x 16 element planar array.

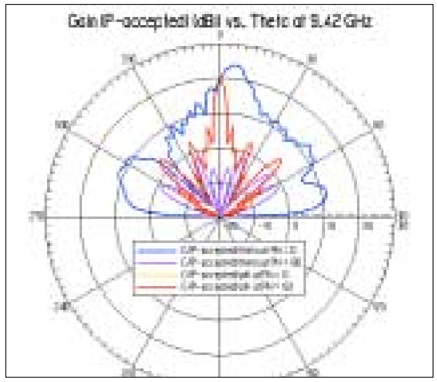

Figure 5. Far-field pattern at 9.42 GHz for 16 x 16 element planar array.

memory by 40X and increase speed by 8X. A traditional MoM solver would have required over 30 Gbytes to solve this geometry.

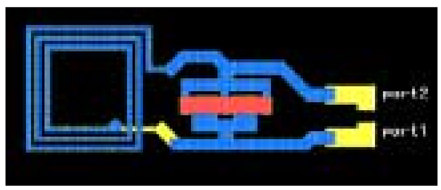

Figure 6. Image reject filter on MCM silicon substrate.

Image Reject Filter on MCM Silicon Substrate

Figure 6 depicts an image reject filter on a MCM silicon substrate[2]. It consists of an inductor, a parallel plate capacitor, and various interconnect. The two-port structure was simulated over an extremely wide 1 MHz to 8 GHz frequency band with a single mesh. The filter is approximately 1.5 mm in length. This corresponds to 5.e-6

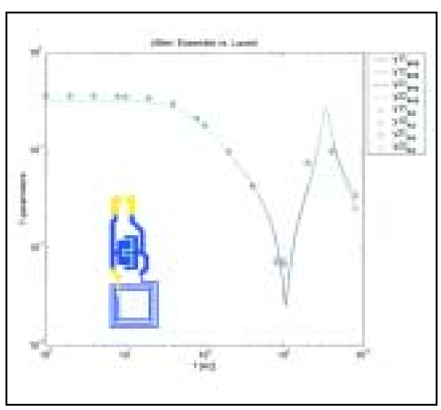

Figure 7. Plot of wideband y-parameters produced by Ensemble (solid curve) versus the Lucent solver results.

wavelengths at 1 MHz. This is indeed a very small structure. Simulation required a MoM matrix with 5577 unknowns and the wideband sweep took 10 hours 33 minutes on a 750 MHz PC. Peak memory usage was 152 Mbytes. Figure 7 is a plot of the wideband y-parameters produced by Ensemble (solid curve) versus the Lucent solver results from reference [2]. Good agreement was achieved. Such wideband results may now be used for transient simulation for sharp rise-time, Gigabit per second broadband communications signals.

Conclusion

A 2.4 GHz MMIC low noise amplifier, full layout EM simulation was illustrated using the Ensemble planar EM simulator. A large 16 x 16 element planar phased array antenna was simulated and simulation results were illustrated. An image reject filter on MCM silicon substrate was simulated to illustrate the stability offered by loop-tree methods for extremely wide frequency ranges. By simulating the passive structures in MMIC circuits and antennas, engineers may greatly reduce design iterations by discovering excessive coupling prior to fabrication. Furthermore, using the new technology, circuits may be designed that are packed extremely densely in order to save die space and reduce cost. RF

References

[1] C.-F. Wang, F. Ling, and J.-M. Jin, "A fast full-wave analysis of scattering and radiation from large finite arrays of microstrip antennas," IEEE Transactions on Antennas and Propagation, Volume 46, Number 10, October 1998.

[2] S. Kapur and D.E. Long, "Efficient full-wave simulation in layered media," Digest of the Custom Integrated Circuits Conference, Denver, 1998.

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