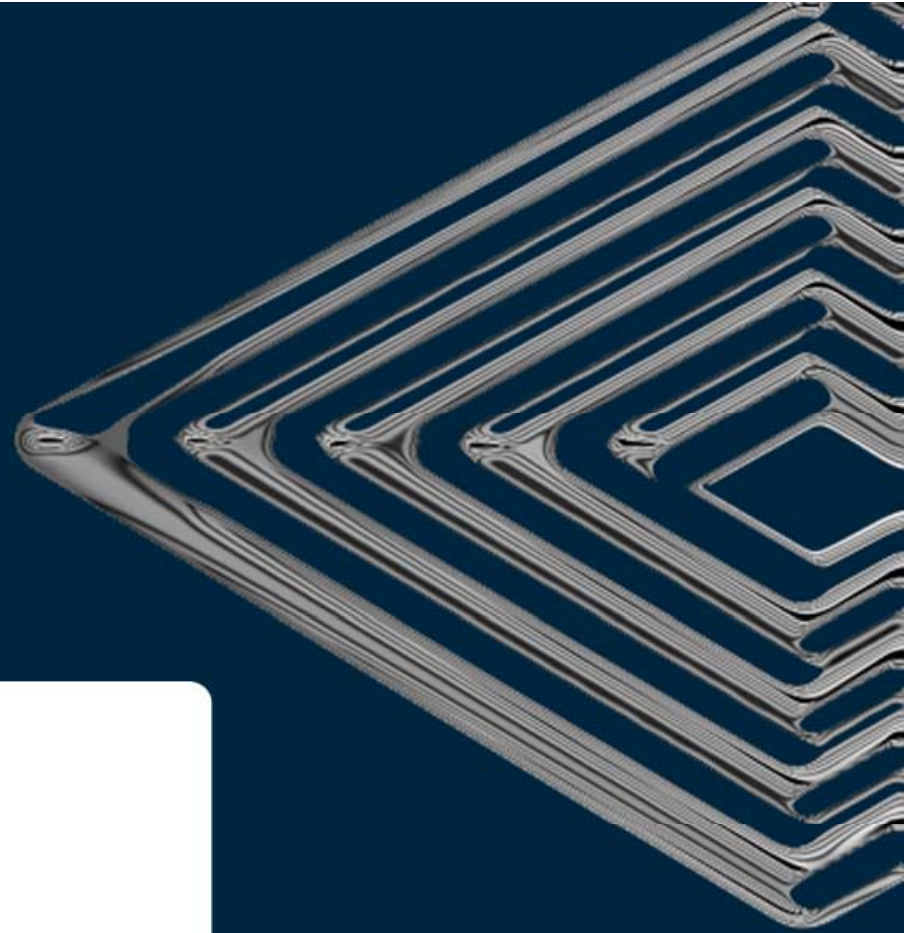


Accurate and Efficient SSN Modeling

Chris Herrick

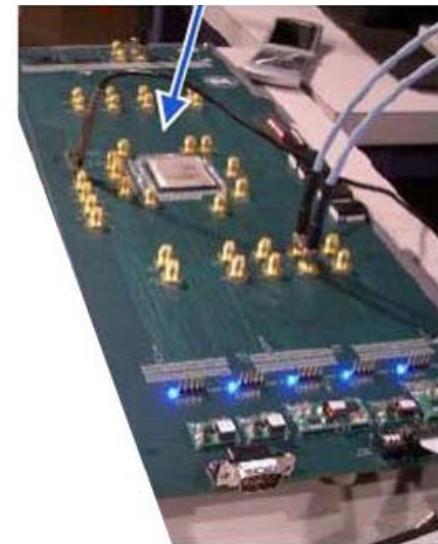
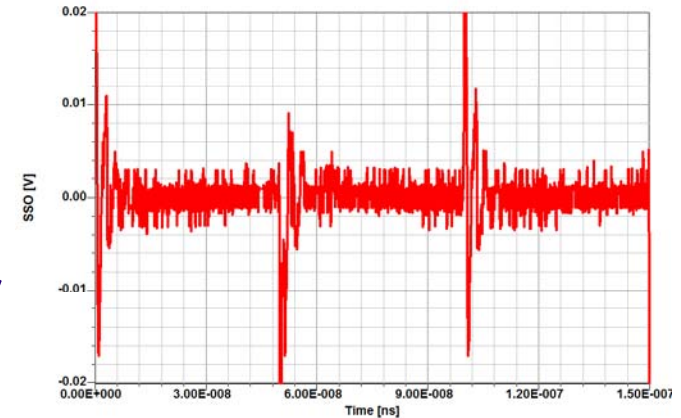


Agenda

- What is SSN?
- Model Types
- Modeling techniques
- Simulation Tips and Tricks
- Incorporating the latest Ansoft features
- Conclusions

What is SSN?

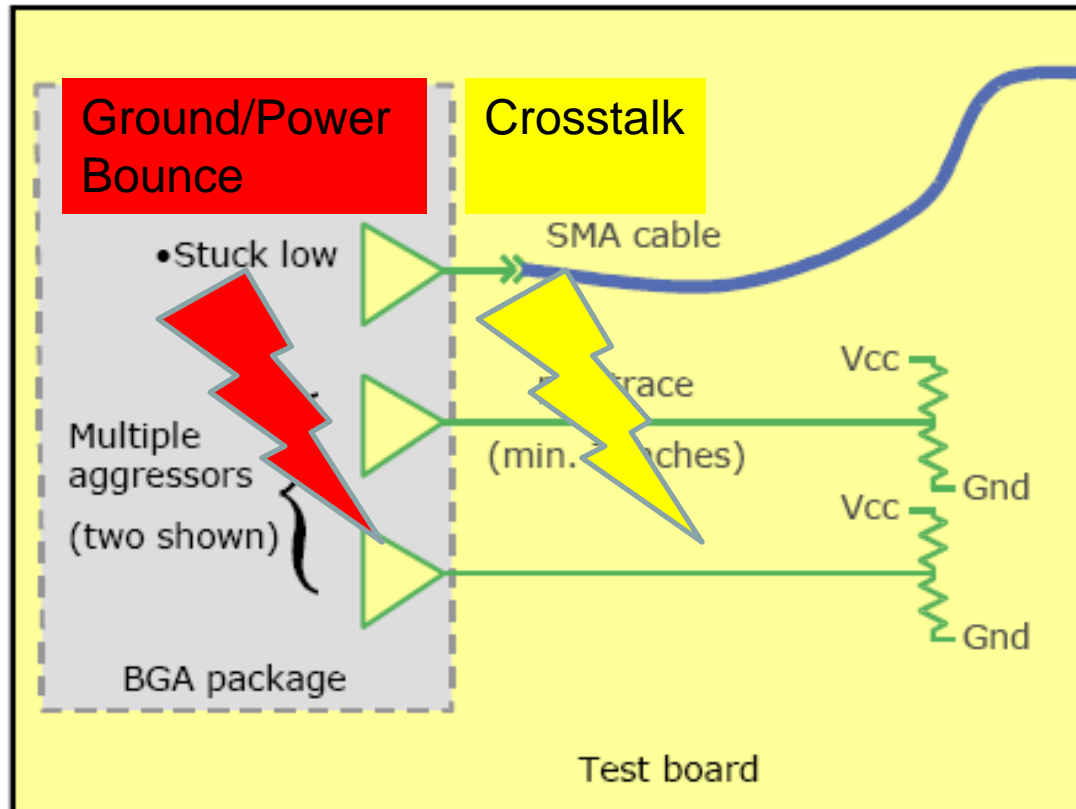
- Simultaneous Switching Noise is the deleterious effect of simultaneous switching outputs (SSO).
- Also referred to as Ground Bounce or Power Bounce
- Exacerbated by poor return path and high loop inductance
- Measured by fixing victim High or Low and monitoring output



Why is SSN important?

- SSN Analysis gives more complete picture of both Signal Integrity and Power Integrity
- Ignoring the effects of SSO can result in a failed system design
- Increased challenges as speeds increase, voltages decrease and current increases
- Helps uncover problematic crosstalk
- Helps evaluate true PDN performance

Typical Setup



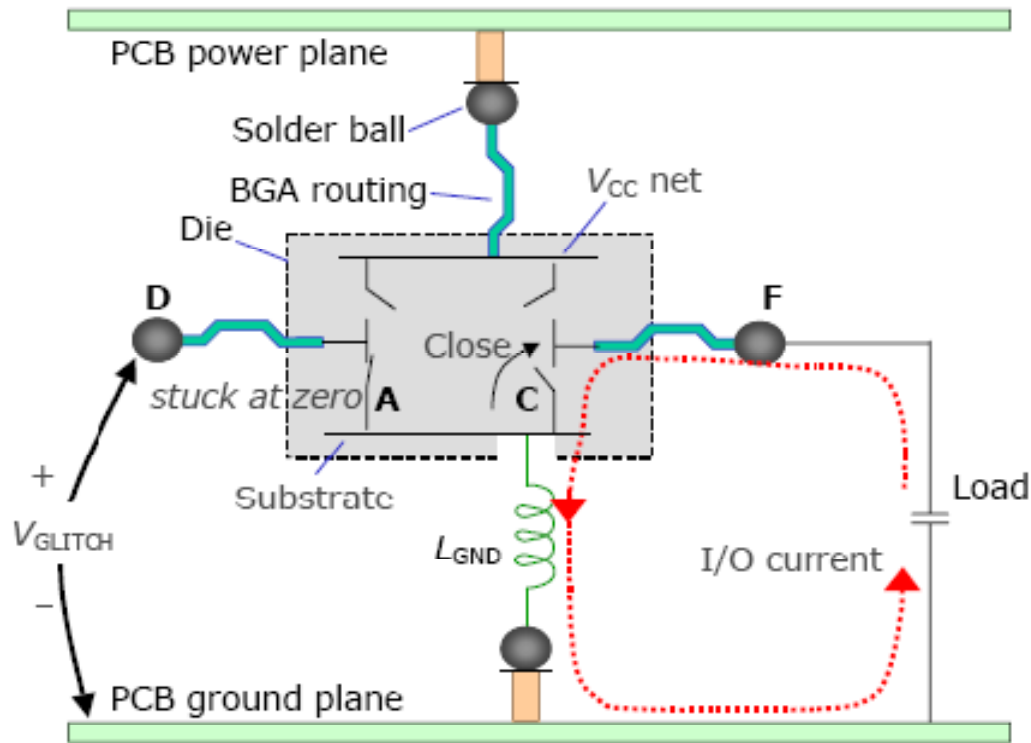
Probe location

Setup

- Victim is held "high" or "low"
- Many I/O's driven at the same time
- Worst case Data Patterns transmitted
- Noise monitored on victim from PCB location

Ref: BGA Crosstalk by Howard Johnson, March 1, 2005

SSN From Ground Bounce



- ◆ BGA between PCB power and ground planes

- ◆ At time zero switches C closed and F transitions Low -> huge I/O current transient

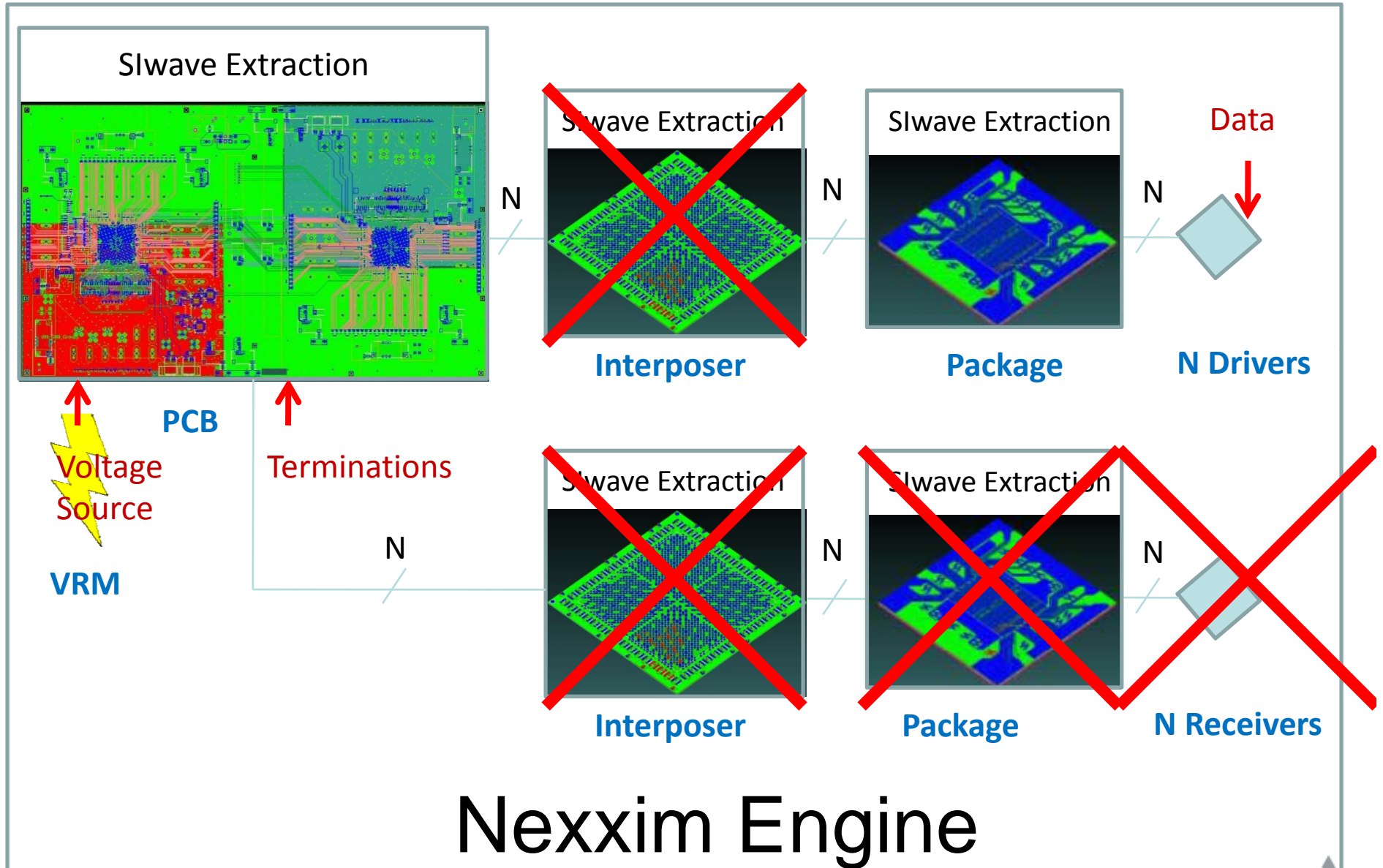
- ◆ $V_{\text{glitch}} = L_{\text{gnd}} di/dt$

- ◆ Victim D is held low will transmit voltage V_{glitch}

Model Types

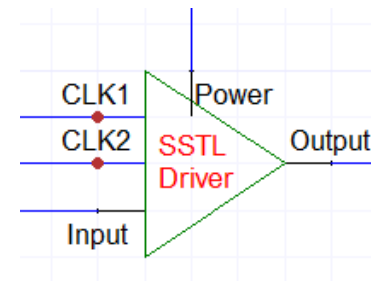
- Need to include all relevant effects of system; Both SI and PI
- Need models for: ICs, Packages, PCBs and VRMs
- Models may be extracted or gathered from vendors
- Each model should be independently verified for accuracy

Designer Environment

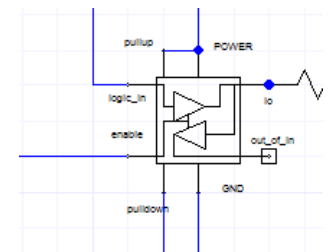


Driver Models

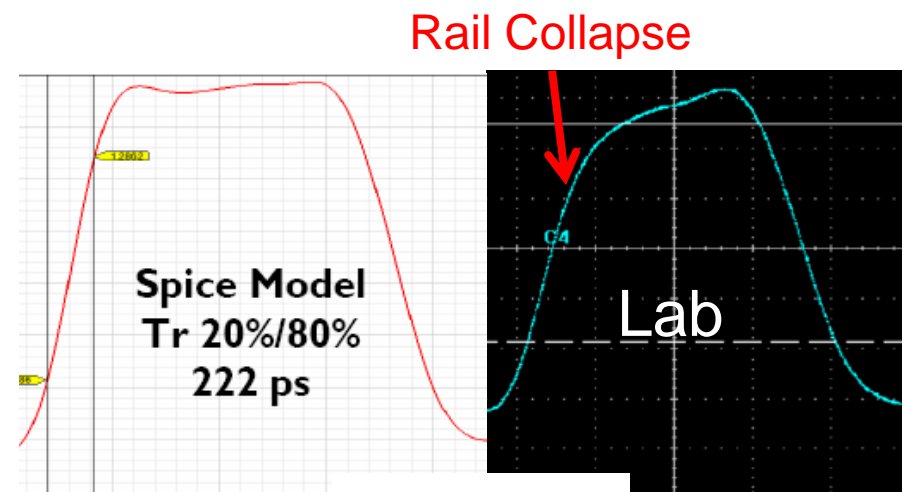
- Need to accurately model Signals and Power
- Obtain transistor level models if at all possible
- IBIS tends to be pessimistic because current scales linearly with increased drivers
- Verify waveforms for single driver AND during SSO



Spice



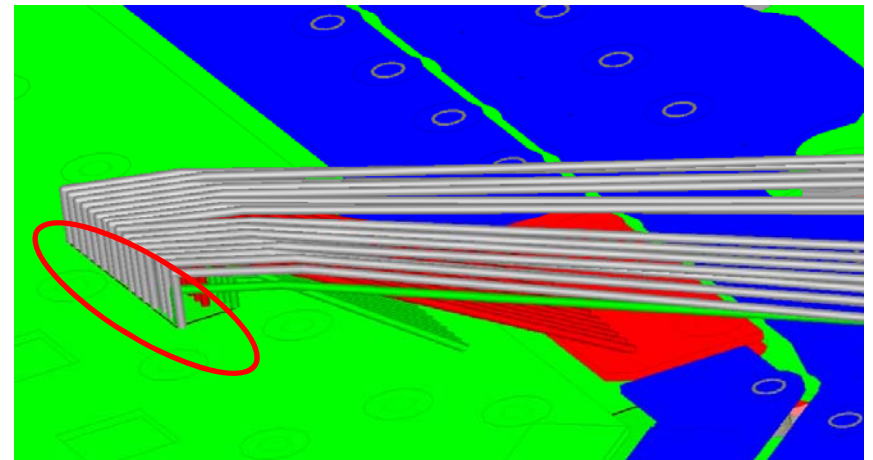
IBIS



During SSO

Package Model

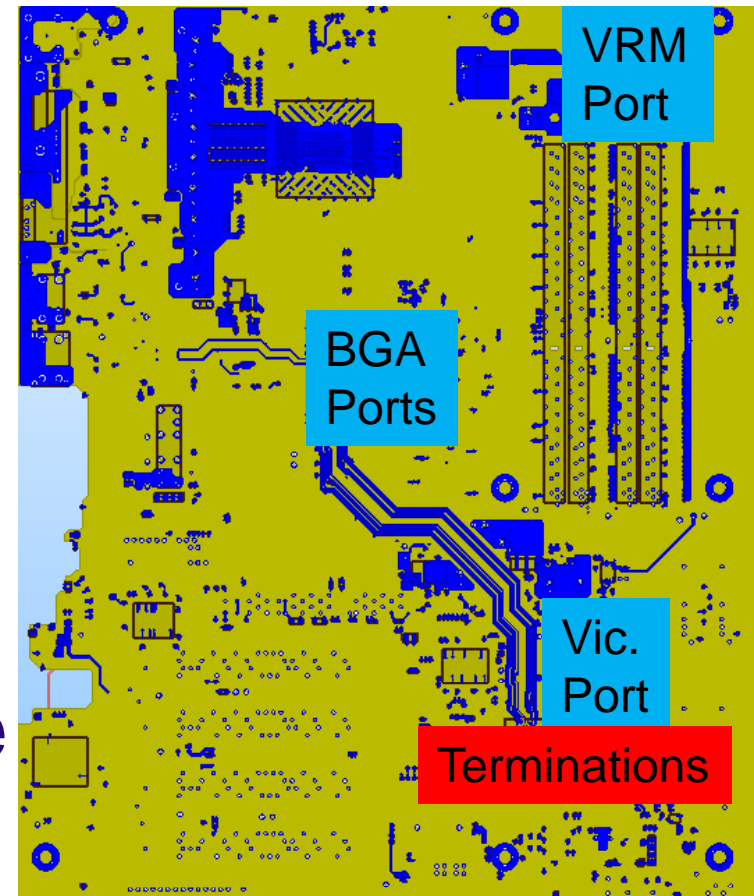
- Obtain layout and extract if possible
- Add Solderballs, Solderbumps, Bondwires to model



- Group Power/Ground pins on die side
- Extract Bank of signals

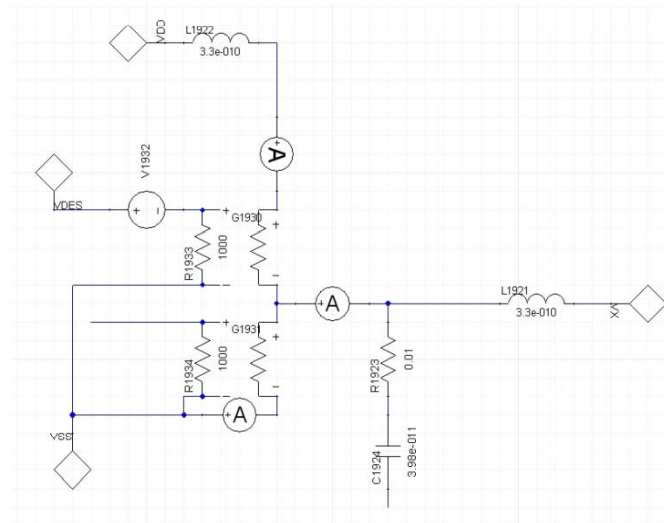
PCB Model

- Extract individual Signal Power/Ground Pins at Package if feasible
- Place port at VRM
- Place port on victim far end
- Terminate far end of line with resistors



VRM Model

- Almost always modeled as an ideal voltage source
- Could also use non-ideal circuit model
- Important for DC-DC switching power supplies

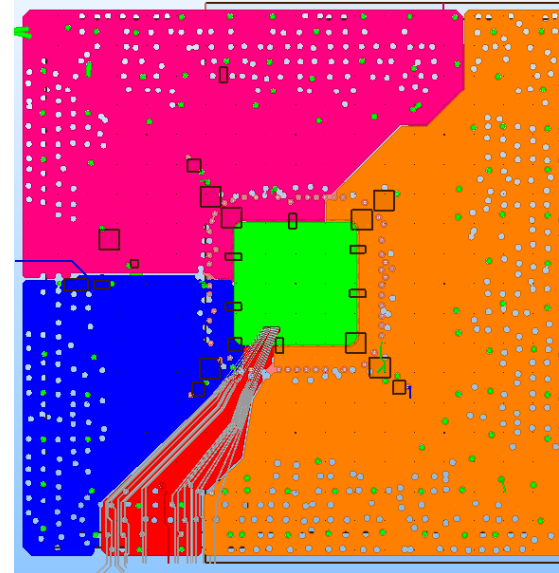


Modeling Techniques

- Kitchen Sink - Simulate Everything!
 - Generally not practical
- Nearest Neighbors
 - Only simulate what's relevant
- Signal grouping
 - Combine many pins into one and scale driver
- Current Mirror
 - Mirror a single driver multiple times

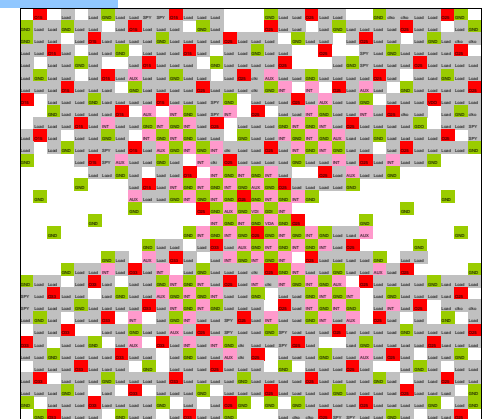
Nearest Neighbors

1. Identify Victim and nearest neighbors based on proximity
2. Extract largest segment you can afford with available hardware
3. Attached Driver models to each signal pin



High Speed Packages generally have banks-easy to segment

Well placed PWR/GND balls limit return path loop area

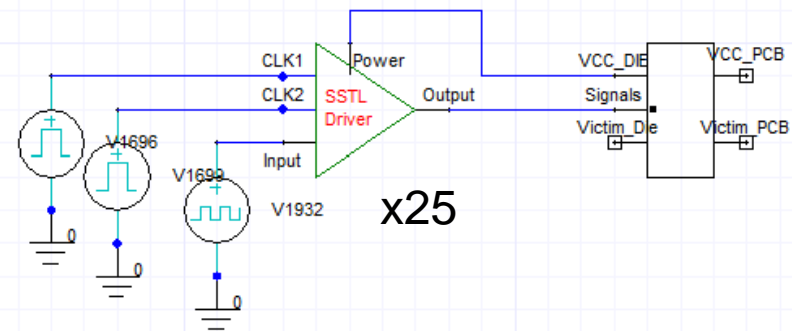
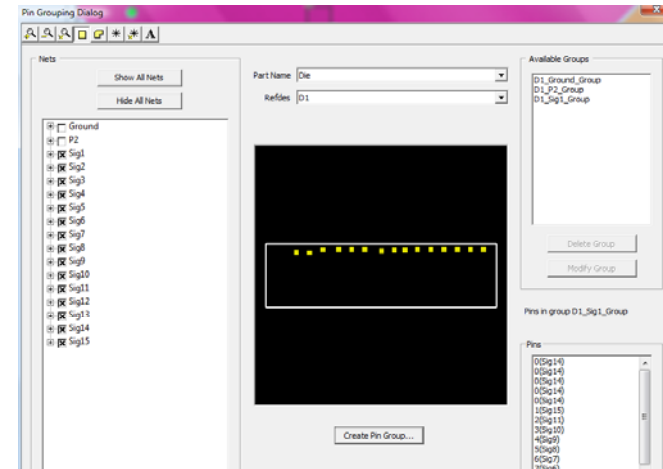


Nearest Neighbor Tradeoffs

- Most accurate and flexible method
- Simulates Skew/Delay between lines
- Allows different data patterns
- Long transient simulation
- Potential for convergence trouble

Signal Grouping

1. Apply pin grouping to signals at Die side
2. Attach single port for Aggressor group
3. Extract PCB ports as before
4. Create subcircuit for driver model
5. Multiply subcircuit M times and connect to aggressor port



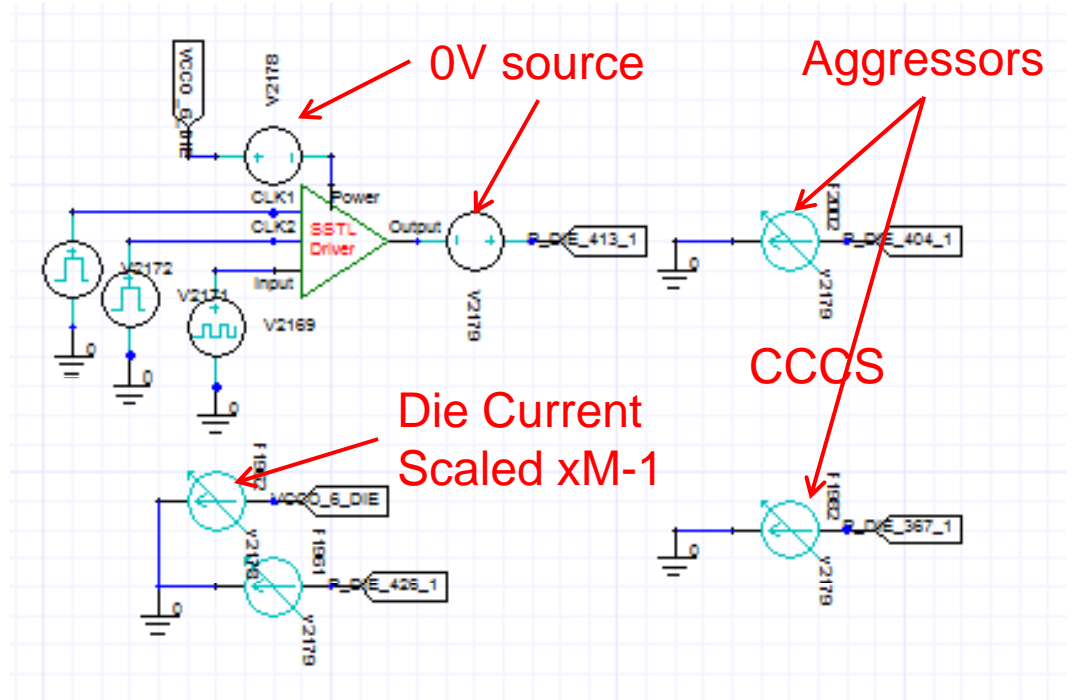
X1 CK1 CK2 Input Output Power driver M=25

Signal Grouping Tradeoffs

- Much quicker analysis
- Greatly reduces port count
- Eliminates convergence issues with multiple drivers
- Not simulating XTLK induced skew
- Same data pattern used on all aggressors
- Assumes all lines are similar in impedance and delay
- Lose information on individual lines
- One bad signal line will affect net results

Current Mirroring

1. Use same extracted model as “Nearest Neighbors”
2. Place driver on one aggressor
3. Monitor current at signal and die connections using series 0v Voltage sources
4. Attach CCOS to all other signal lines mirroring same current as driver
5. Attach CCOS to die scaling current x M-1 drivers



Current Mirroring Tradeoffs

- Much quicker analysis
- Eliminates convergence issues with multiple drivers
- Still can inspect individual s-parameters
- Not simulating XTLK induced skew
- Same data pattern used on all aggressors
- Assumes all lines are similar in impedance and delay

Simulation Tips and Tricks

- Convolution versus state-space
- Frequency sweep setup
- Mixed port impedances
- Achieving Convergence

S-parameter Handling

State-Space (Default)

- Much faster for long transients
- Passivity enforcement
- Causality enforcement
- Up front cost building model
- Does not extrapolate
- May not achieve fit on noisy data
- Cannot model long delays, $\sim 22\lambda$

Convolution

- More options for convergence
- Can handle long delays
- Data filtering options
- Extrapolates well
- Sim time increases quadratically with tran time
- Requires linearly spaced data

Sweep Setup

DC point required

Coarser sweep used at Higher frequencies

Discrete Sweep ensures causality and passivity enforcement

| | Start Freq / Hz | Stop Freq / Hz | Num. Points | Distribution |
|---|-----------------|----------------|-------------|--------------|
| 1 | 0 | 0 | 1 | Linear |
| 2 | 1 | 50e6 | 25 | By Decade |
| 3 | 50e6 | 15e9 | 601 | Linear |

Min Rise/Fall Time / s: 3.33333E-011

Set FWS generation parameters

Sweep Selection:
 Discrete Sweep
 Interpolating Sweep

Error Tolerance: 0.005
Number of Interpolation Points: 200

Parameter Plot Options:
 Plot S-parameters
 Plot Y-parameters
 Plot Z-parameters
 Plot magnitude response at all ports
 Plot phase response at all ports

Buttons: Save Settings, OK, Cancel

Log sweep helps capture low frequencies important to PDN

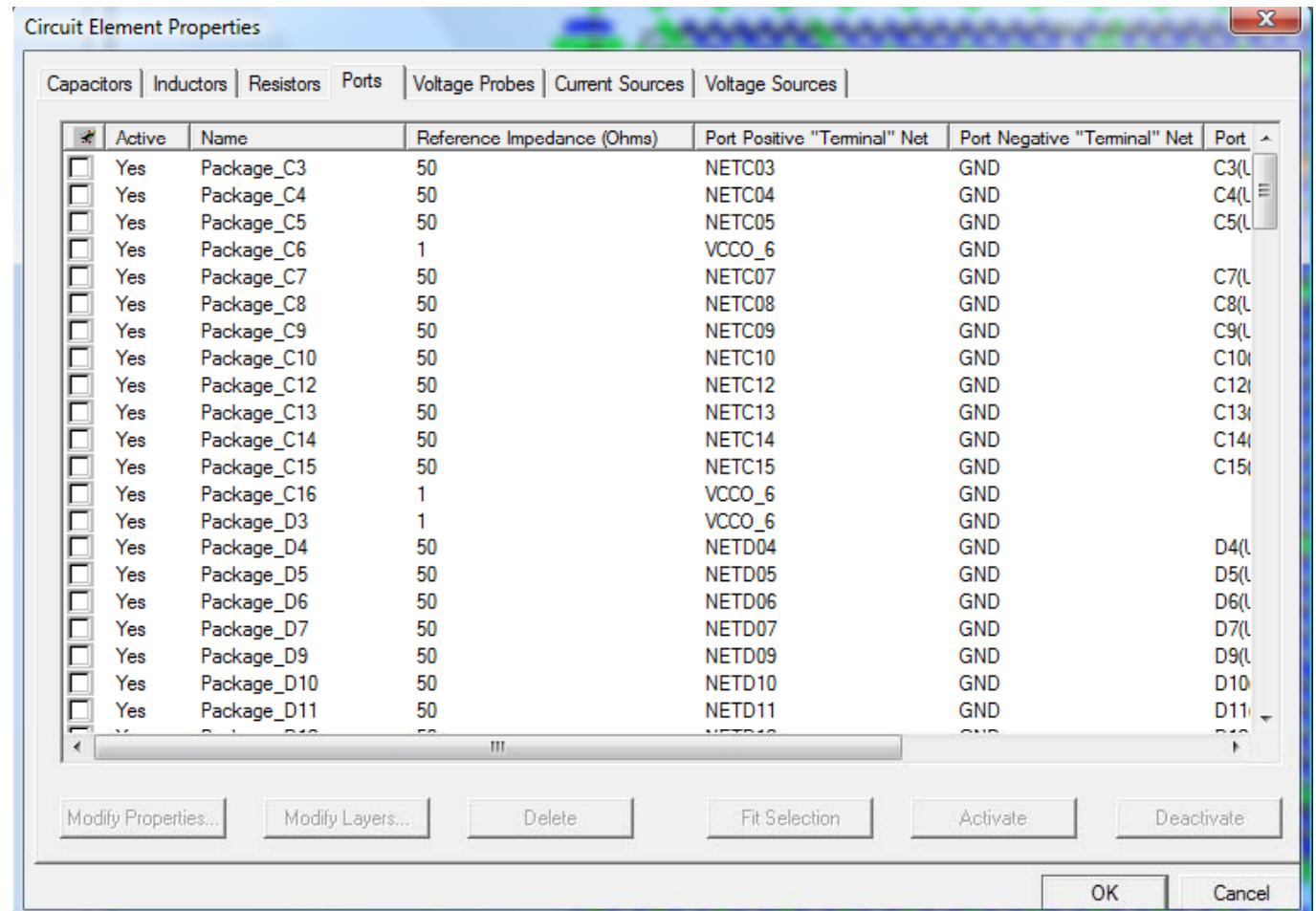
Set max even higher than knee frequency: State space doesn't extrapolate!

Port Impedances

Choose port impedances that are relatively close to structure impedance

Use 1 or .1 ohms for power, 50 ohms for signal lines

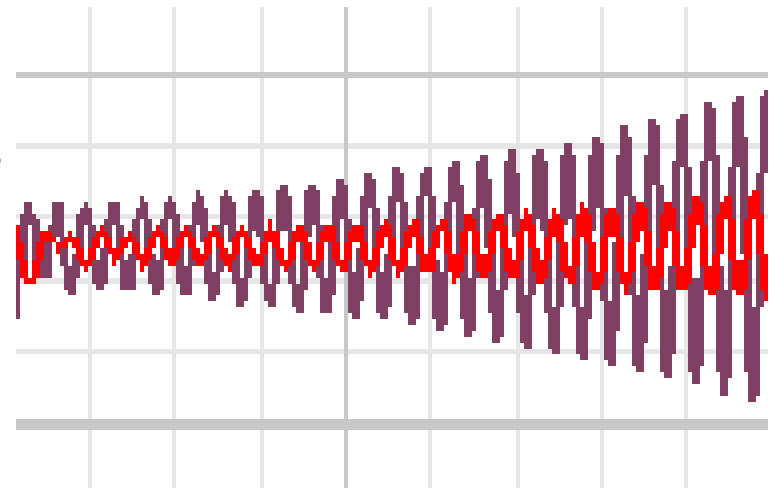
This helps model accuracy and avoids 0dB values in touchstone file



Designer dynamic link to Slwave will preserve port impedances

Achieving Convergence

- Inspect individual models (Divide and Conquer)
 - Realistic data, passive, causal
 - Sufficient bandwidth, resolution
 - Frequency dependent materials
- Bypass/Deactivate components to find root cause
- Check state-space fit; tighten `s_element.reltol`
- Increase `s_element.max_states`
- Slow risetimes/Soften Edges
- Try generic sources, i.e. Gaussian PRBS
- Reduce `.tran` step
- Decrease `reltol` and `abstol`
- Try convolutions 1-3
- Reduce s-parameter port count



Schematic Setup

- Schematic setup can be tedious and error prone when working with large number of components
- Modular/hierarchical blocks can aid with design management and debugging
- Four methods for automatic setup:
 - Dynamic Linking
 - APDS
 - Designer I/O Wizard
 - Slwave Slwizard

Dynamic Links

Project Manager

- Dummy_channel*
 - IBIS_Drivers_High
 - IBIS_Drivers_Low
 - No_aggressors
 - Power_Supply
 - Probe
 - Top_Level
 - Definitions
 - Components
 - Symbols
 - Footprints
 - Padstacks
 - Models
 - Package
 - PCB
 - PCB_080321
 - PCB_080401
 - PCB_080402
 - PCB_080410
 - PKG_080321
 - PKG_080401
 - Materials
 - Scripts

Power Supply

Victim Spyhole

PCB

Package

Drivers

1 2 New Page

Add symbols for each block in the channel

| Name | Value | Unit | Evaluated Value |
|-----------------|-------------|------|-----------------|
| ModelName | FieldSolver | | |
| CosimDefinition | Edit | | |
| CoSimulator | PCB_080410 | | |
| Status | SIwave | | |

- PCB_080321
- PCB_080401
- PCB_080402
- PCB_080410
- PCB_080410

Add additional model choices by dragging models onto symbol

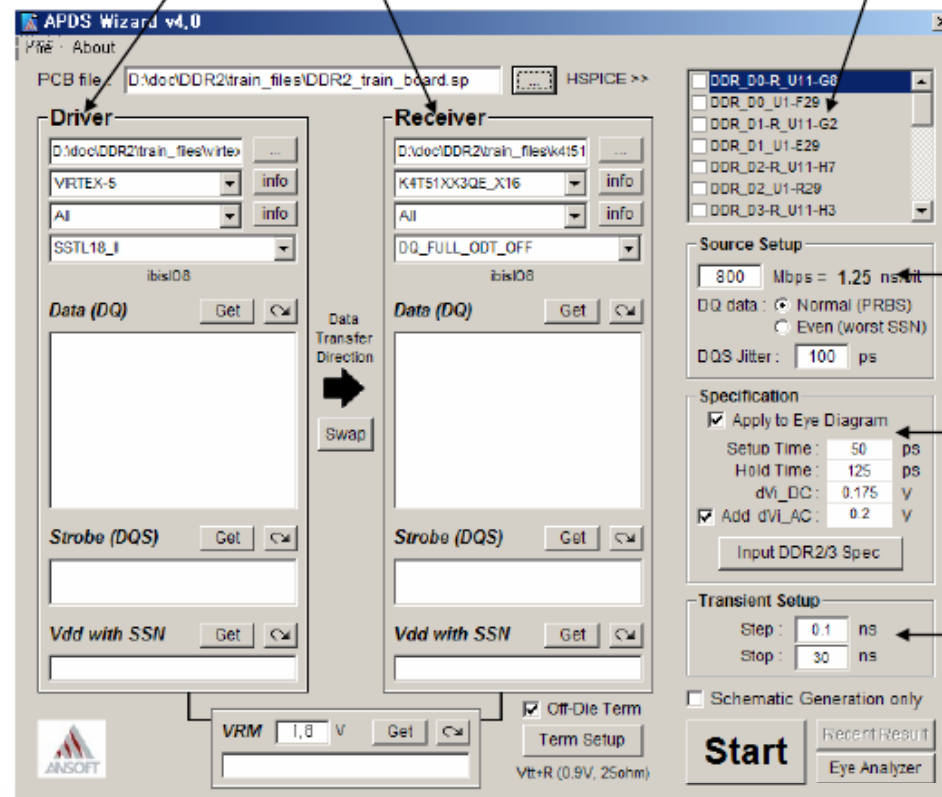
APDS

Separated IBIS & ports
for Driver & Receiver

Open ports list
to be applied to appropriate port

Stand-alone GUI to
setup transient analysis

Specifically tailored to
SSN of DDR interfaces



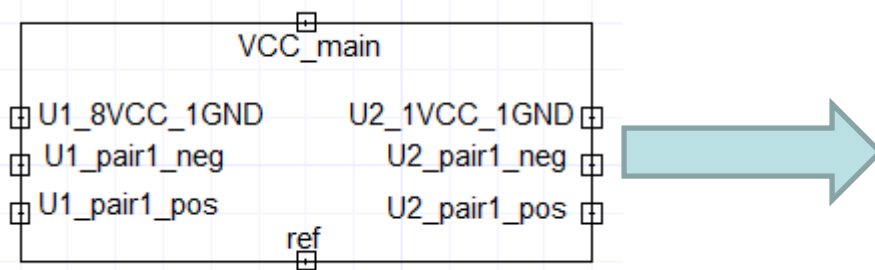
Source Setup

Spec Setup

Transient Setup

Designer I/O Wizard

- Launch GUI from Designer 4.1
- Rapid setup of drivers for high pin counts
- Easily link generic model types for all blocks in the channel



m1 - Schematic

Channel - Via transitions and Connector

StateSpace Options

U4 Transmission lines

HfssVia

U16 Transmission lines

HfssVia

HfssVia

I/O Wizard

Summary

| Pins | Action | Options |
|---------------------------------------|------------|---------------|
| SIwave35_Component;989 : U1_8VCC_1GND | Power/GND | Not Connected |
| SIwave35_Component;989 : U1_pair1_neg | Unassigned | |
| SIwave35_Component;989 : U1_pair1_pos | Unassigned | |
| SIwave35_Component;989 : U2_1VCC_1GND | Power/GND | Not Connected |
| SIwave35_Component;989 : U2_pair1_neg | Unassigned | |
| SIwave35_Component;989 : U2_pair1_pos | Unassigned | |
| SIwave35_Component;989 : VCC_main | Power/GND | Not Connected |
| SIwave35_Component;989 : ref | Unassigned | |

Actions

Set as power/ground pins...

Set as signal pins...

Setup Sources/Analysis...

Subcircuit Grouping

Enable Subcircuit Grouping

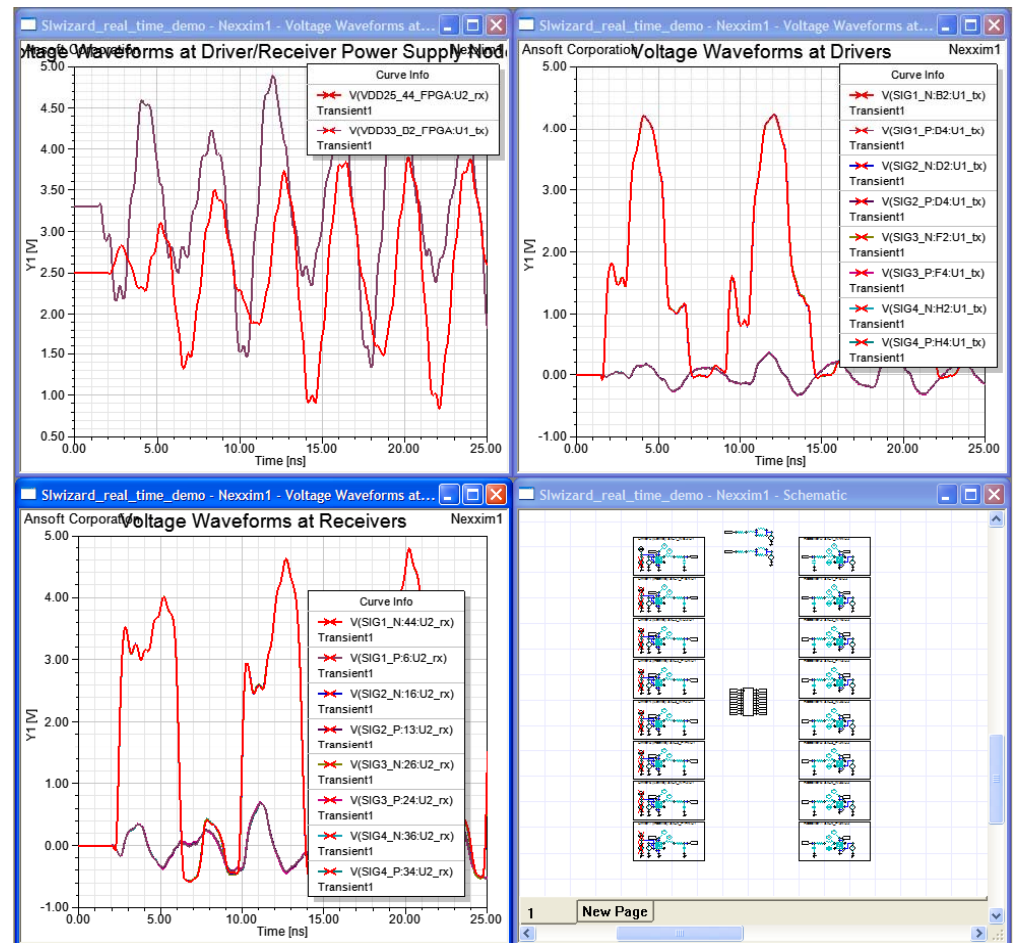
Set group: []

Auto assign all groups

OK Cancel

Slwizard in v4.0 Slwave

1. Select signal nets to simulate
2. Assign IBIS TX/RX models to pins on nets
3. Identify component power/ground nets
4. (Optional) Set VRM parameters
5. Set Transient Simulation parameters



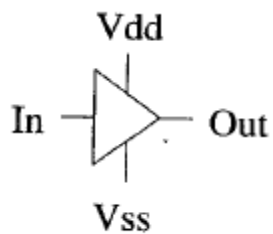
Pin info preserved from layout

Conclusions

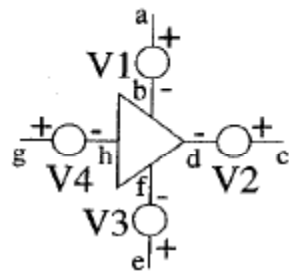
- SSN is a powerful simulation offering insight to both Signal and Power behavior
- Accurate device models are critical
- Set realistic goals and choose the best method to obtain them
- Ansoft has the capabilities and the automation to perform accurate and efficient SSN simulations

Current Mirroring

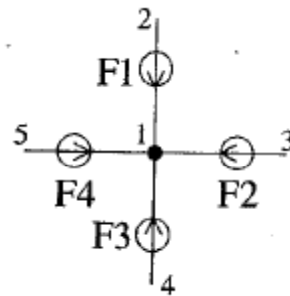
- Place drivers for a single aggressor and the victim. Mirror the current to all other aggressors using CCCS.



Original



Original
w/ Detectors



Mirrored

* The current detectors

V1 a b 0

V2 c d 0

V3 e f 0

V4 g h 0

* The current mirror

F1 2 1 V1 1

F2 3 1 V2 1

F3 4 1 V3 1

F4 5 1 V4 1

Ref: Digital Signal Integrity, Young