

# High Speed PCB Design

## *Ride the Wave Workshop*



# **Post Route Analysis of a High Speed PCB Design**

## **Design/Analysis for Power Delivery System (PDS)**

# Post Route Analysis of a High Speed PCB Design



# Designing for the Future

- In today's world, the demand for ultra-high-speed PCB design is on the rise
- Engineers are assigned the task of design mixed analog and fast rise-time digital boards, and have all signals arrive at their destination cleanly
- With the advance of highly specialized design and layout software, the design of these boards has become increasingly 'easy' (automated)
- These physical design and layout tools can be provided with design constraints and auto-routed easily, resulting in increased productivity of the layout engineer *and* contributions to signal integrity problems

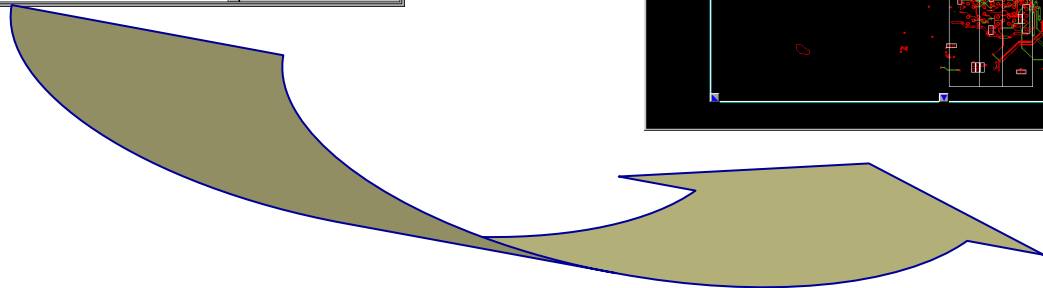
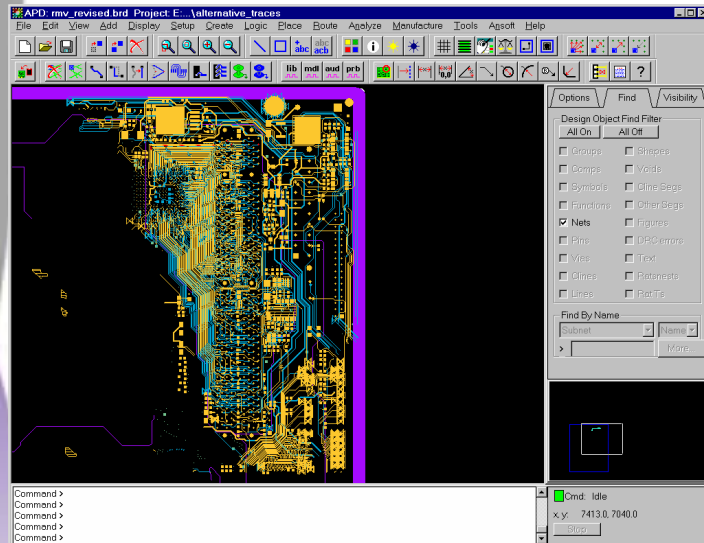
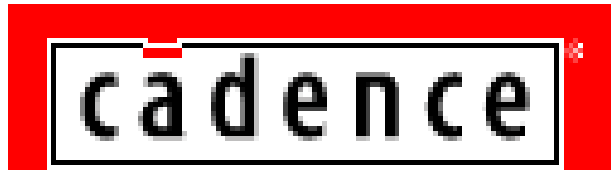
# Designing for the Future

- The advancement of design and layout software needs to be matched by the accompanying advancement in powerful ANALYSIS tools used to solve timing delays, mismatched line impedances, crosstalk, and dielectric loss on high speed lines
- Just as an auto-layout program cannot layout 100 percent of the nets on a complex, high-speed board, an analysis tool cannot default to 2-dimensional field solvers and behavioral models on 100 percent of the nets on a PCB.
- Many nets on a board may be analyzed accurately using 2-d solvers. However, critical signals will require a full 3-d solver that does not default to an 'ideal' case for the current return path. The full 3-d solver will take into account ground planes with holes, cutouts or that are split. Changes in reference planes, cutouts, and coupling to power/ground planes are other situations that require a full 3-d solver

# Goals for this Presentation

- Show the integration between Allegro and PCB/MCM
- Show mixed 2D and 3D extractions
- Show single net and multiple net simulations
- Show how to investigate signal integrity issues caused by meandering traces used for timing delays
- Show Crosstalk simulations on a victim net in the design
- Show how to setup up differential pair simulations
- Show comparison between full 3D PEEC solutions and mixed 2D/3D subcircuits

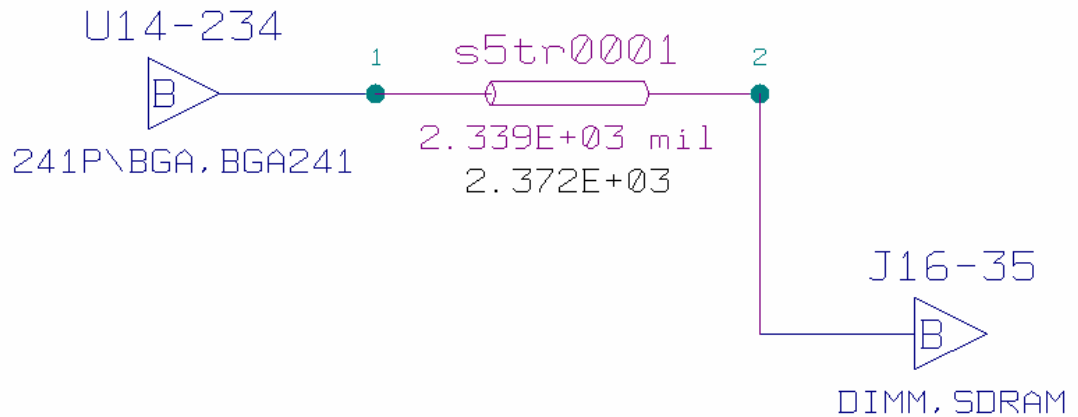
# INTEGRATION



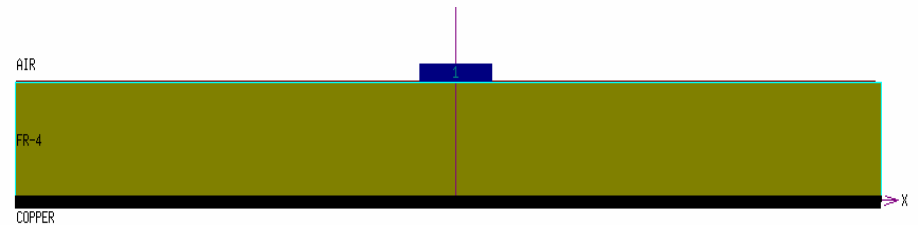
high performance EDA

# Automatic Translation

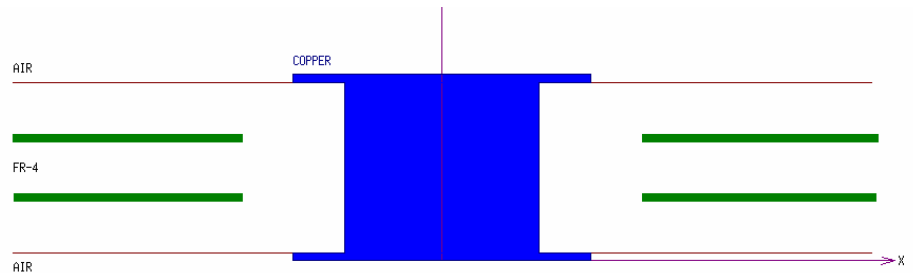
Net Name  
**MAA4**



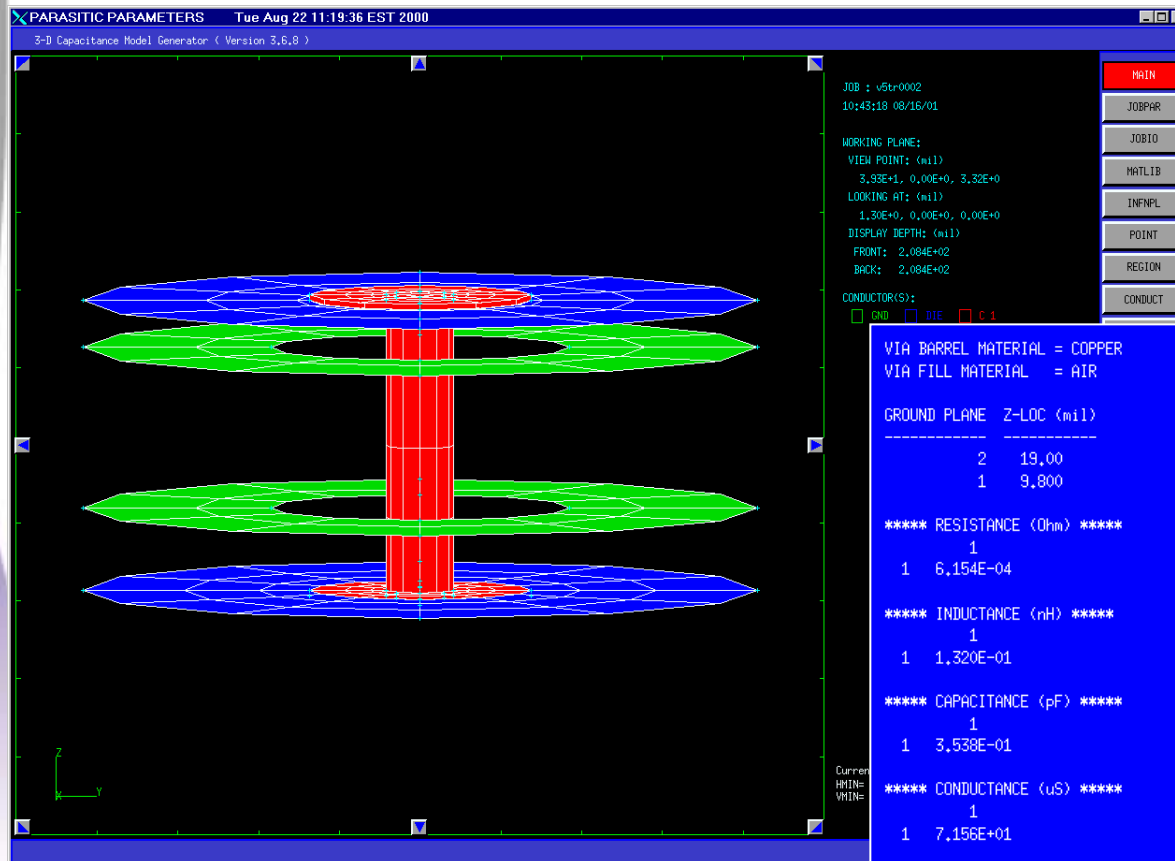
2D Cross-section of  
every net in board



3D Via parasitics  
calculated for every  
via in board

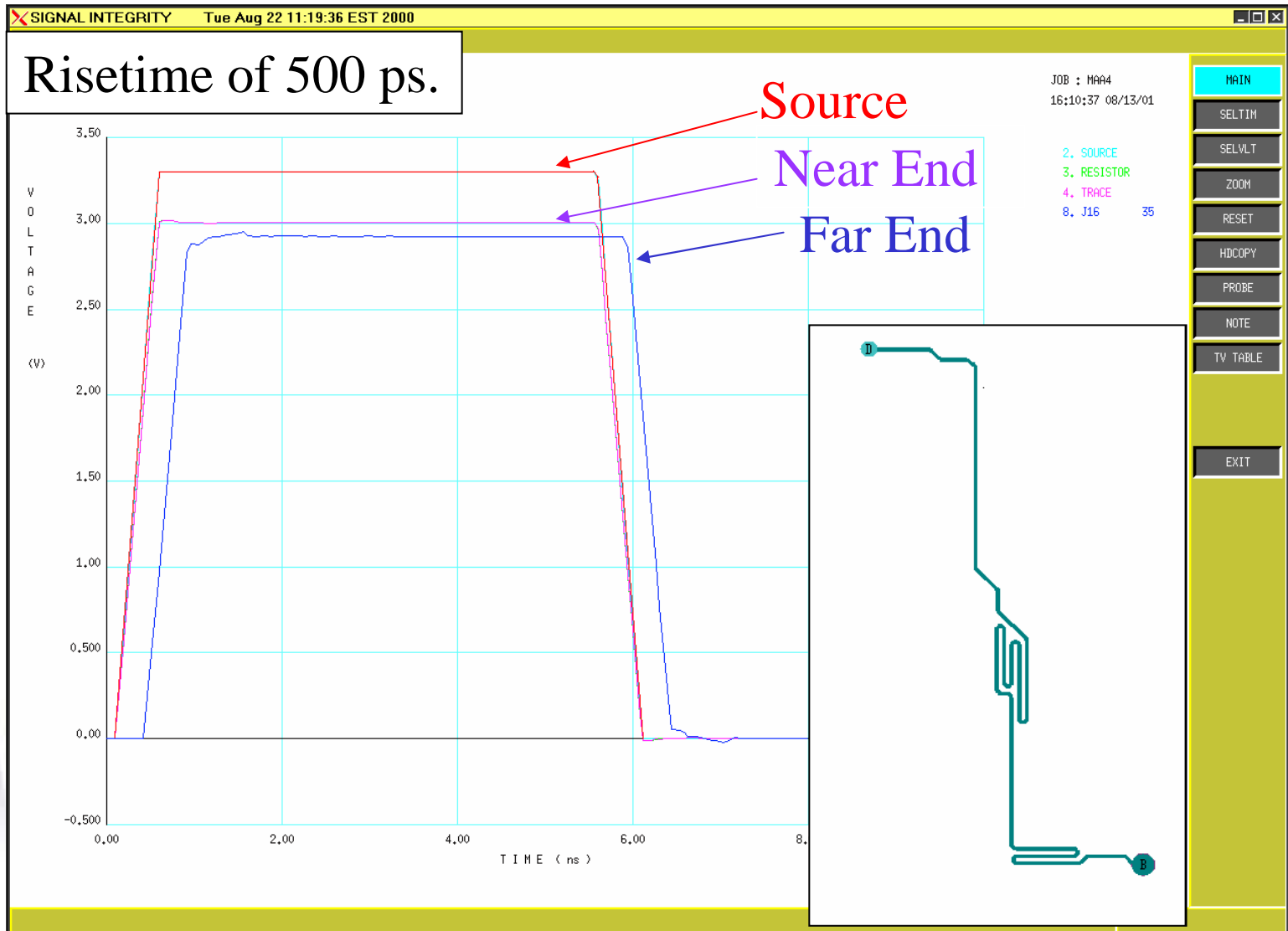


# 3D Via Parasitics



A 3D model is used to calculate all via parasitics.

# Single Net-by-Net Simulations



# Single Net-by-Net Signal Integrity Violations

\*\*\*\*\* DRIVER-RECEIVER PAIR INFORMATION \*\*\*\*\*

NOTE: NUMBERS IN ( ) ARE VIOLATIONS.

ns FOR TIMES

V FOR VOLTAGES

[MAA4]

<U14-234 J16-35>

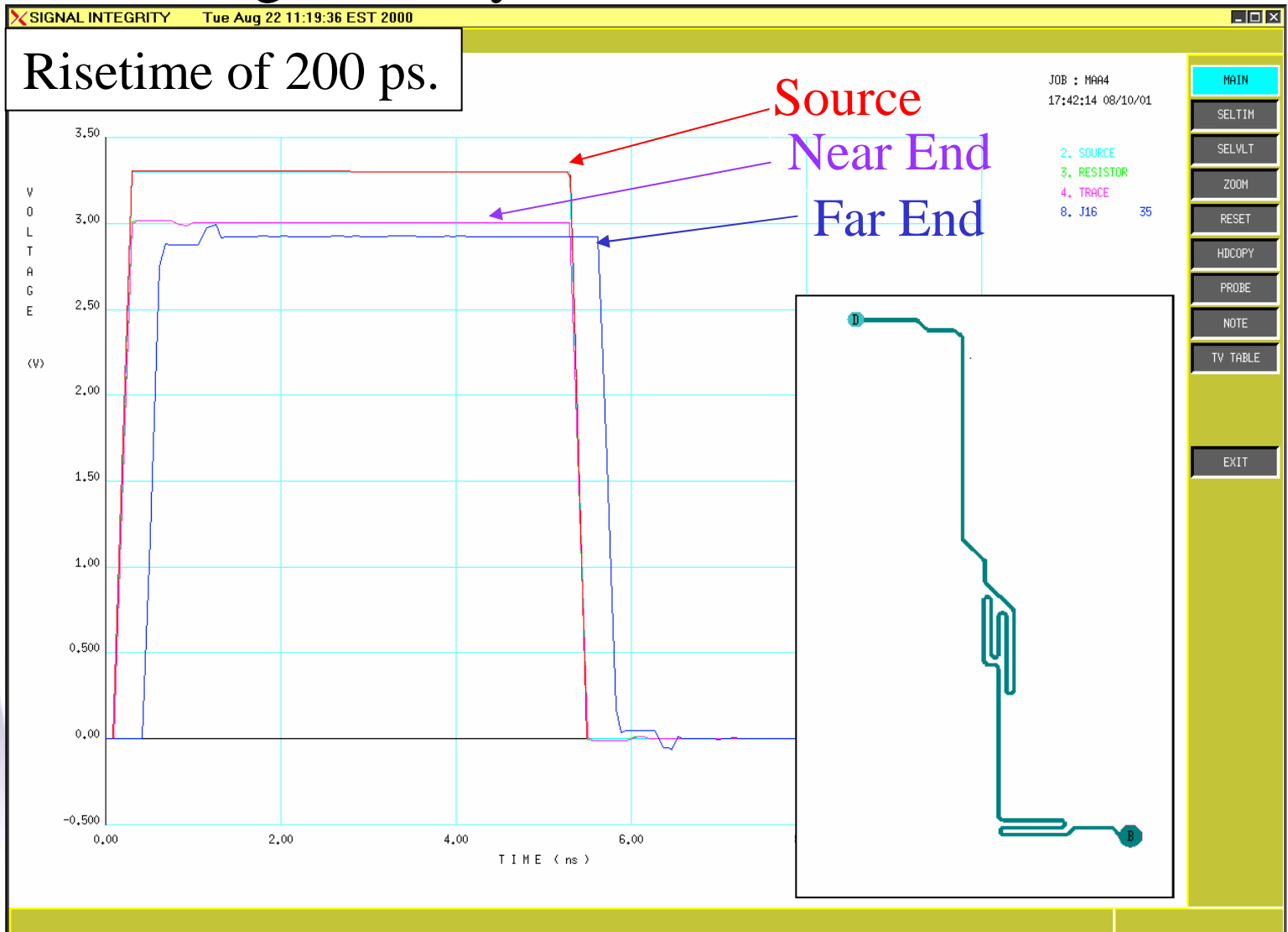
WAVE PROPAGATION DELAYS AT RISE & FALL = (	0,5979)	(	0,5227)
SETTLING TIMES AT HIGH & LOW LEVELS =	1,2389		1,1838
SETTLED VOLTAGES AT HIGH & LOW LEVELS =	2,9184		0,0000
SETTLED PERIODS AT HIGH & LOW LEVELS =	81,2 %		80,8 %
POSITIVE & NEGATIVE OVERSHOOT VOLTAGES =	0,0000		0,0613
POSITIVE & NEGATIVE UNDERSHOOT VOLTAGES=	0,0000		0,0066
META STATE VOLTAGES AT RISE & FALL =	2,8681		0,0499

<J16-35 U14-234>

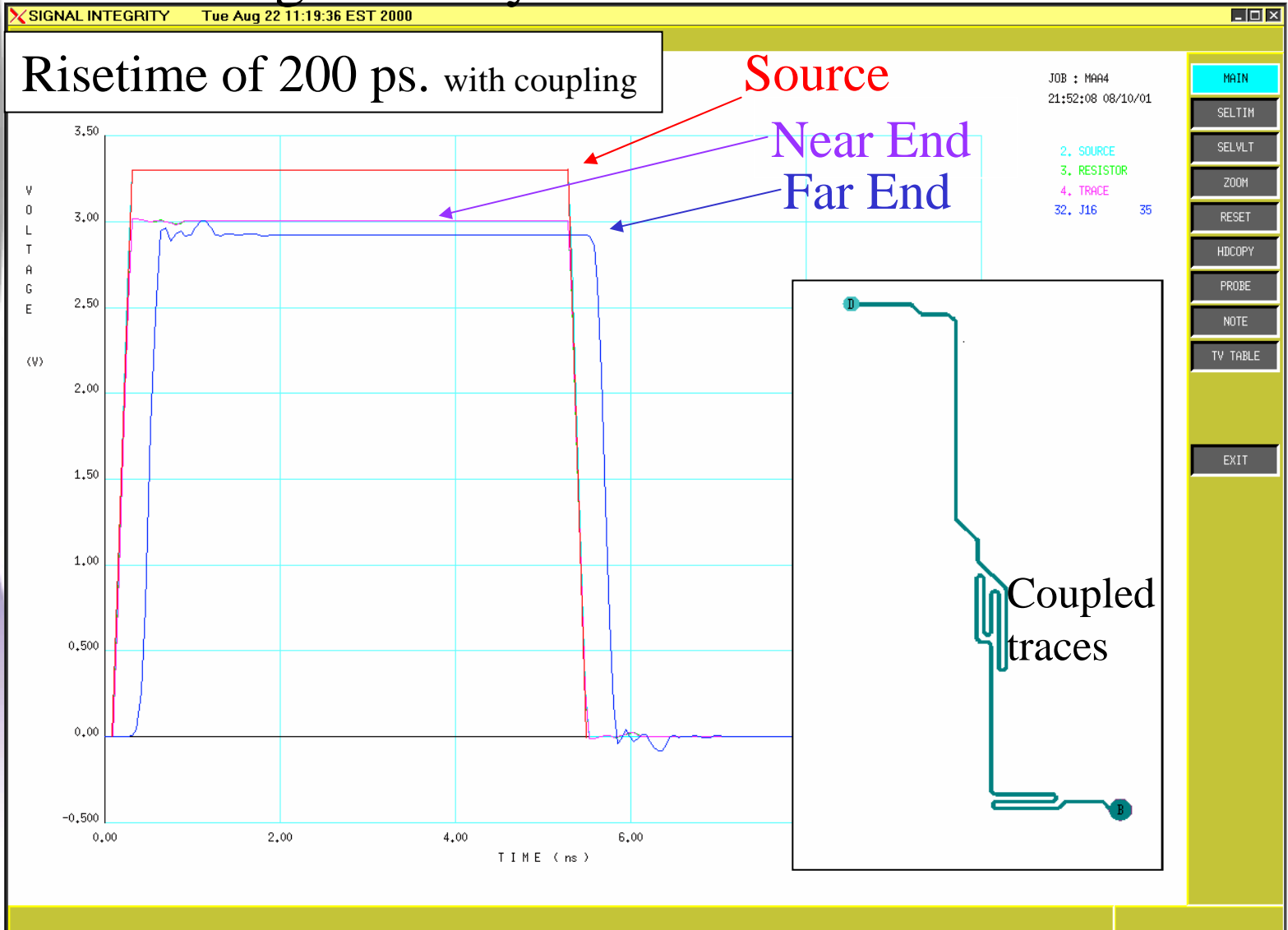
WAVE PROPAGATION DELAYS AT RISE & FALL = (	0,5940)	(	0,5191)
SETTLING TIMES AT HIGH & LOW LEVELS =	0,6493		0,6493
SETTLED VOLTAGES AT HIGH & LOW LEVELS =	2,9185		0,0000
SETTLED PERIODS AT HIGH & LOW LEVELS =	93,0 %		92,4 %
POSITIVE & NEGATIVE OVERSHOOT VOLTAGES =	0,0000		0,0180
POSITIVE & NEGATIVE UNDERSHOOT VOLTAGES=	0,0000		0,0026
META STATE VOLTAGES AT RISE & FALL =	2,8714		0,0470

- Quickly screen information for every net on the board for violations such as Propagation Delay and Settling times

# Single Net-by-Net Simulations



# Single Net-by-Net Simulations

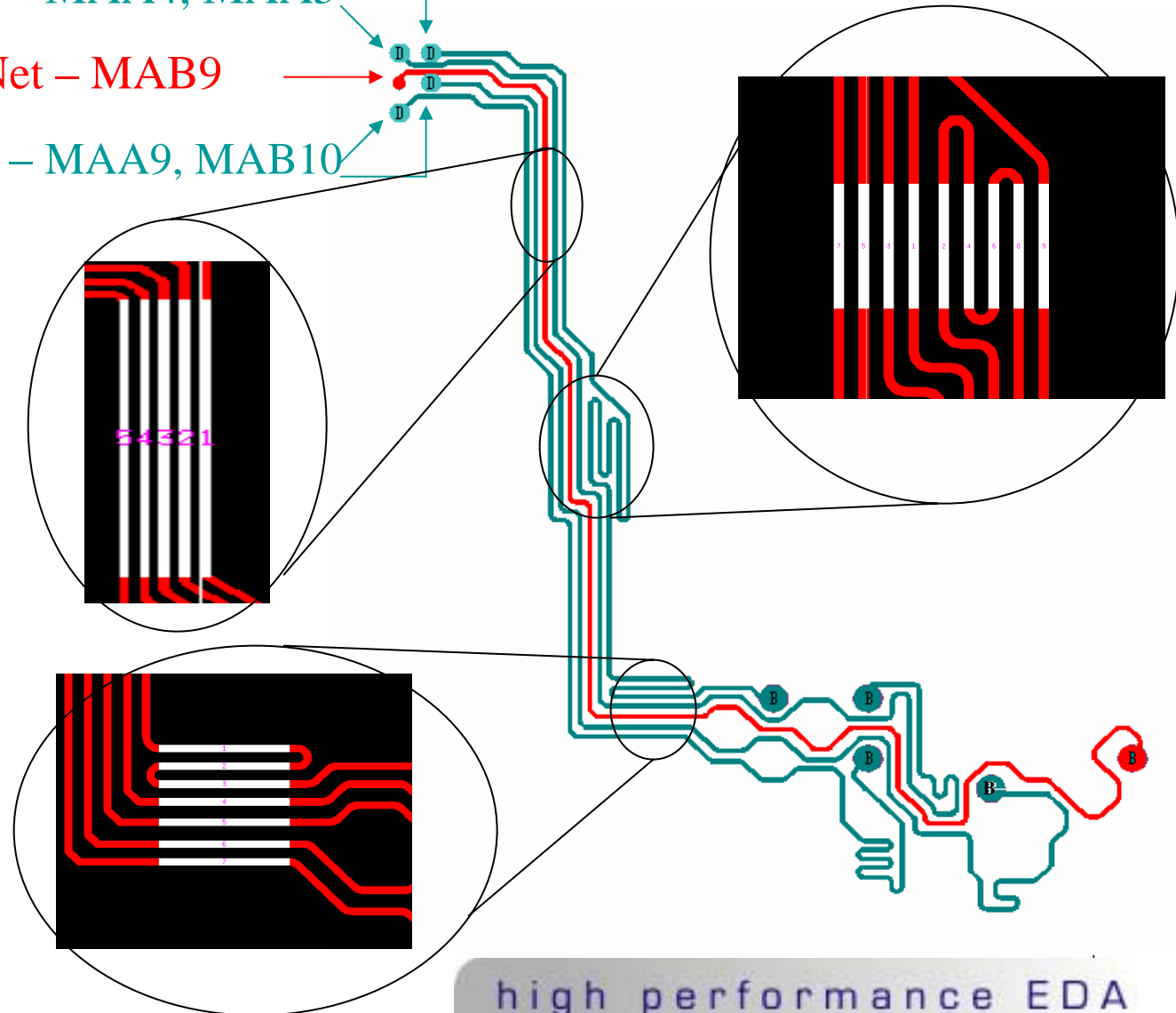


# Crosstalk Simulation – The Setup

Aggressor Nets – MAA4, MAA5

Victim Net – MAB9

Aggressor Nets – MAA9, MAB10



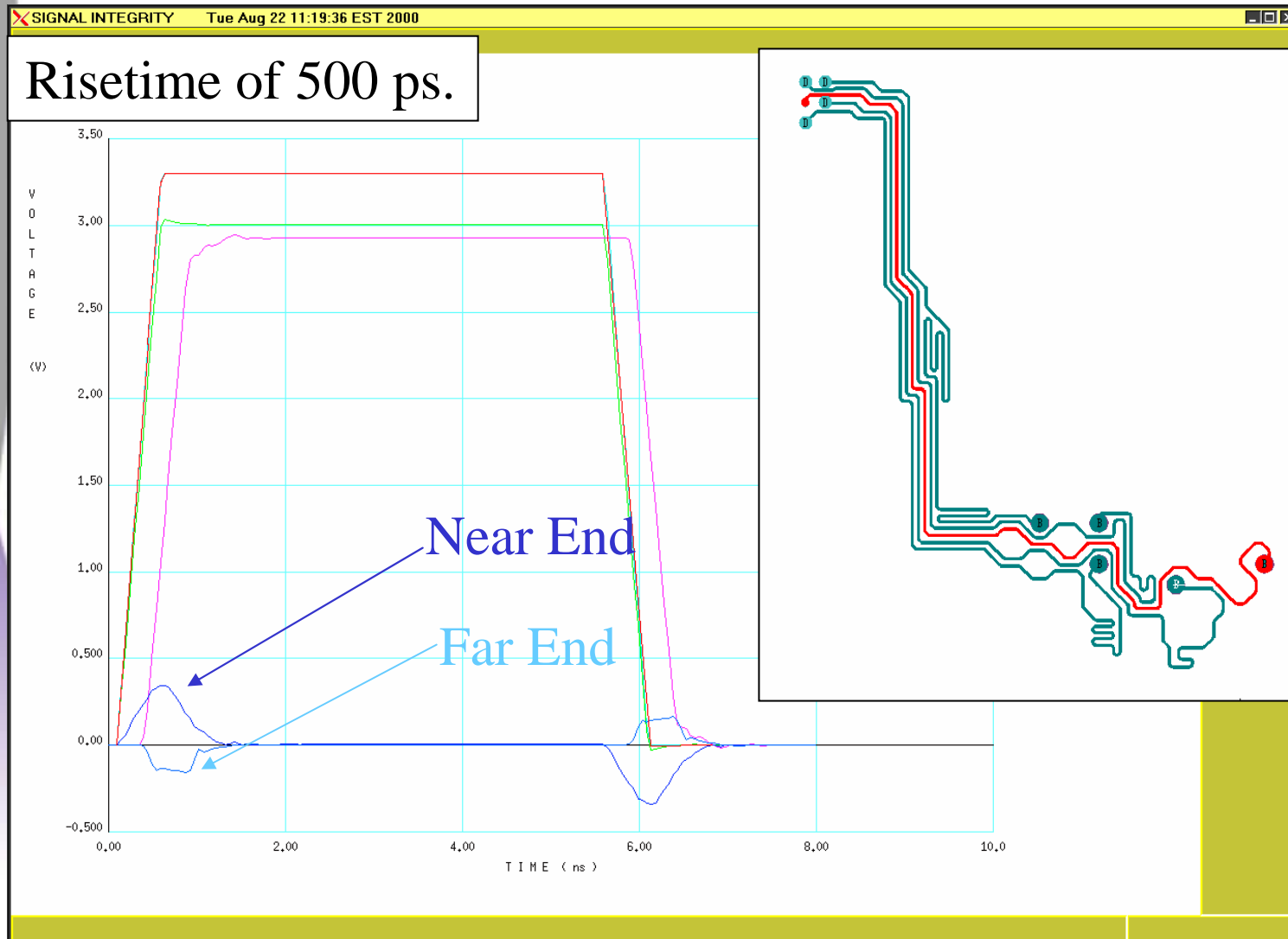
## Crosstalk Simulation – The Setup

- ◆ Create 2D cross-sections of single line and mutual parasitics for all 5 nets
- ◆ Apply 3.3V pulse to one terminal of MAA4, MAA5, MAA9 and MAB10, and put 75 ohm terminators on the other terminals
- ◆ Terminate net MAB9 with 75 ohm terminators at each end

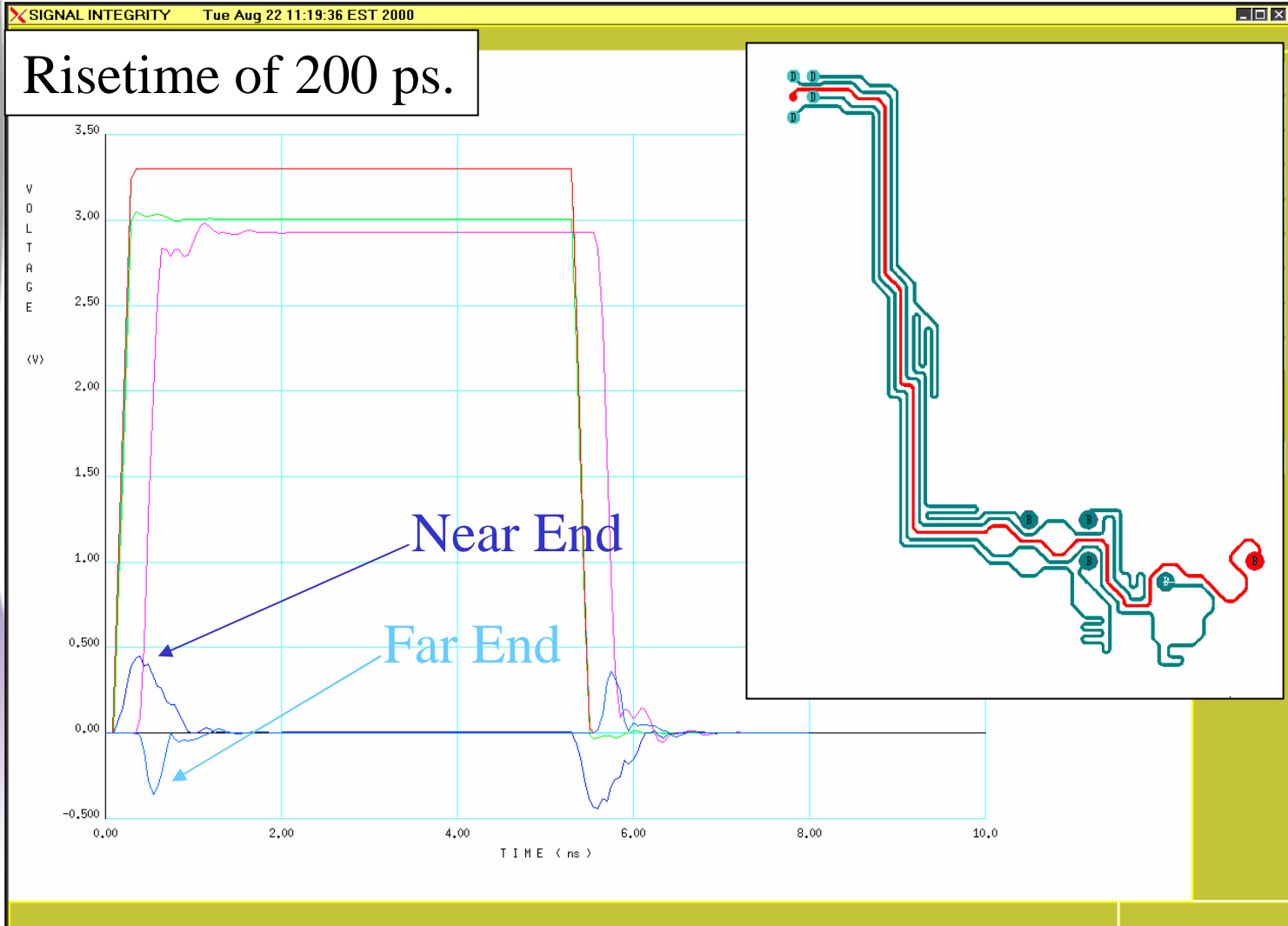
The above 3 steps are done by the program automatically.

- ◆ First run simulation with 0.5 ns rise/fall time, then run again with 0.2 ns rise/fall time

# Crosstalk Simulations

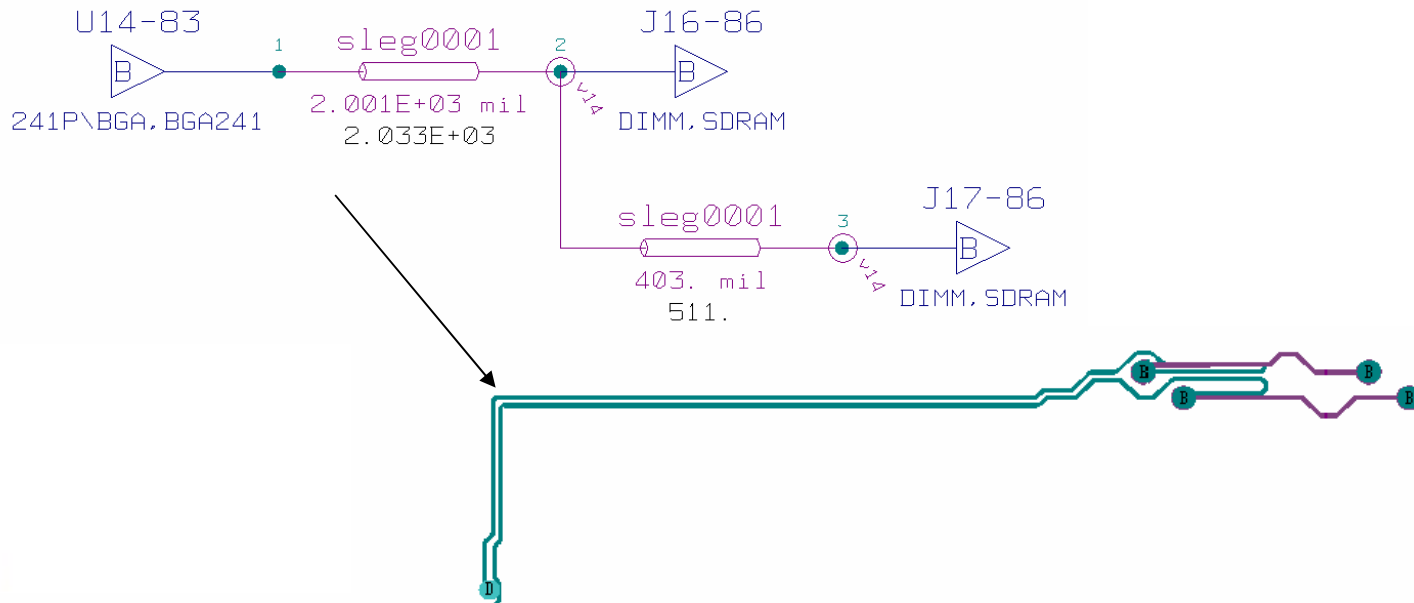


# Crosstalk Simulations

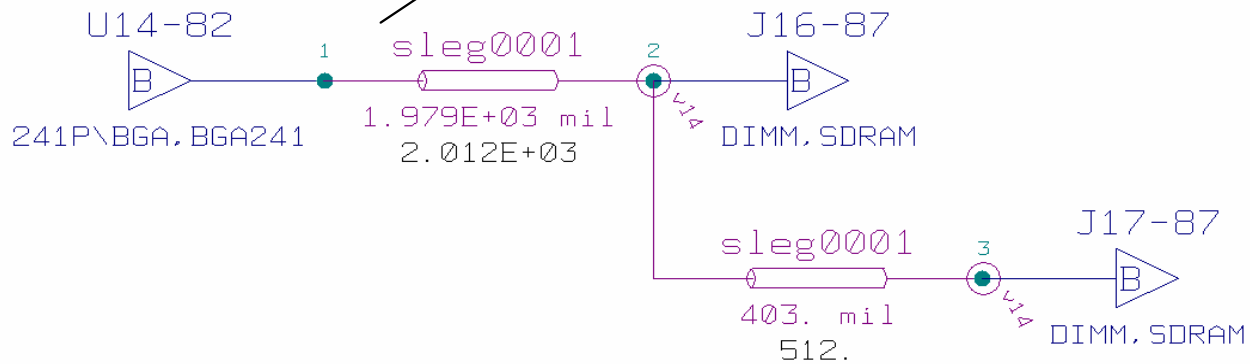


# Differential Pair

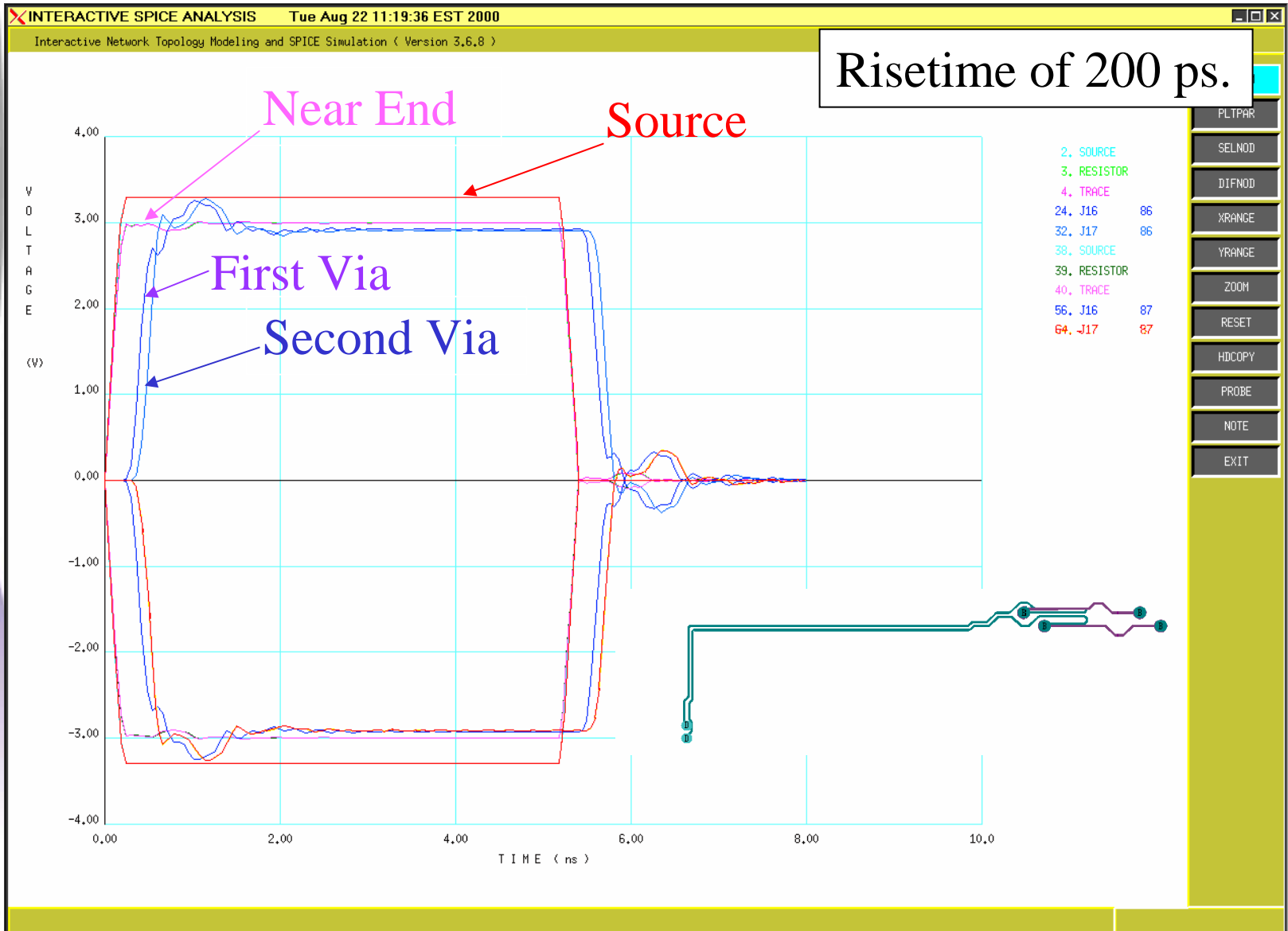
## MD32



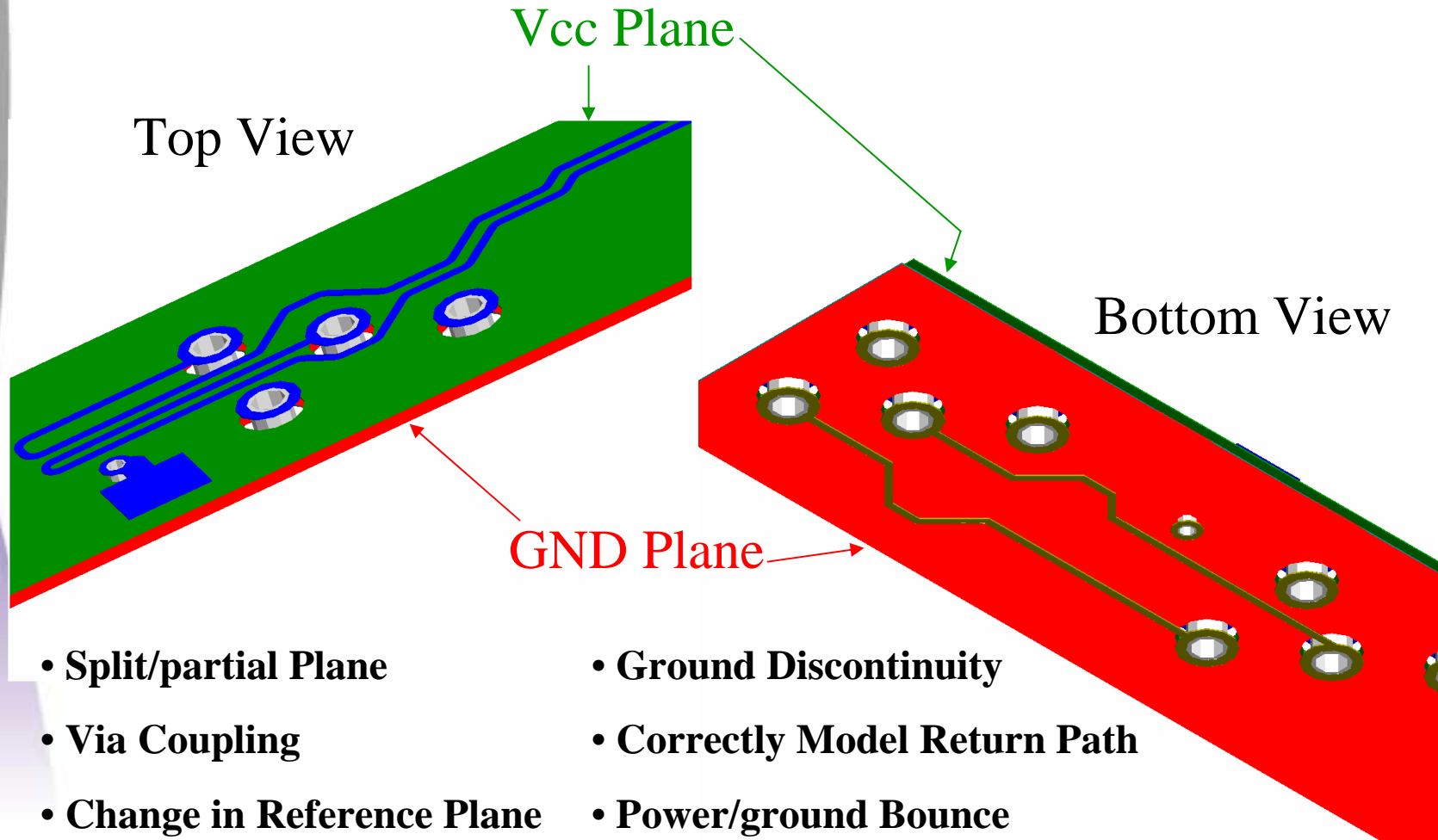
## MD33



# Differential Signaling with Linear Source

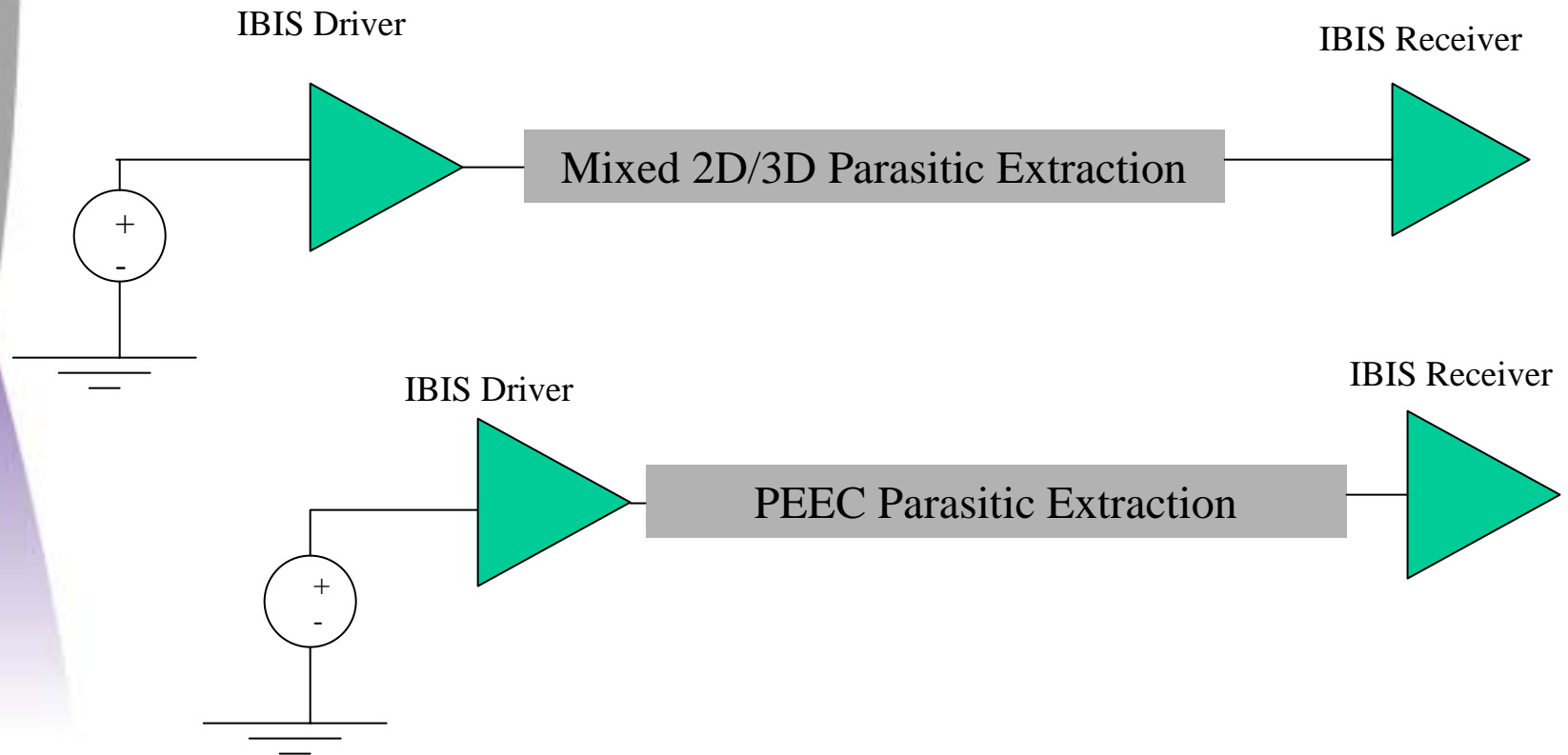


# When to Analyze in 3D?

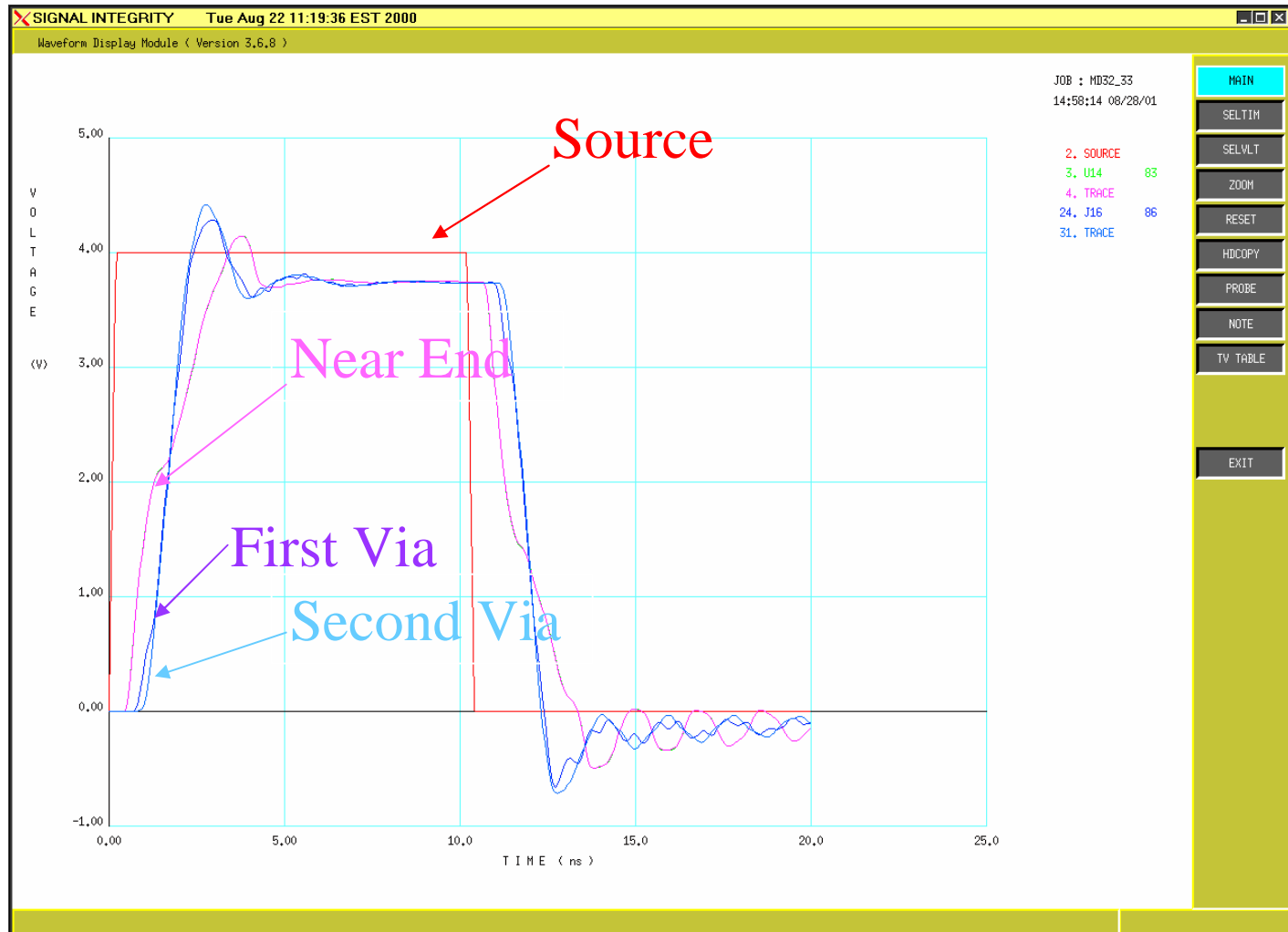


- Split/partial Plane
- Via Coupling
- Change in Reference Plane
- Ground Discontinuity
- Correctly Model Return Path
- Power/ground Bounce

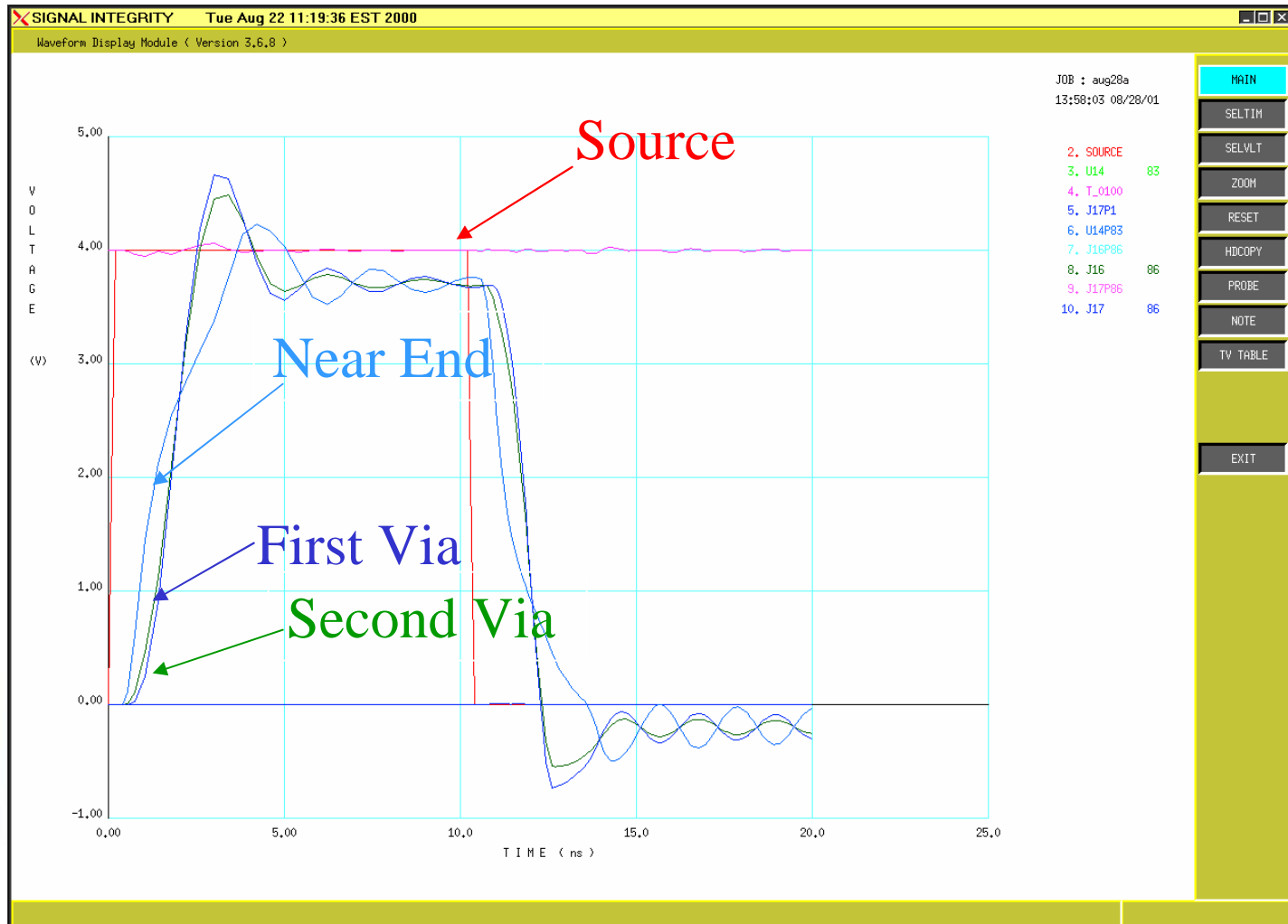
# Comparison of Mixed 2D/3D with IBIS Driver/Receiver



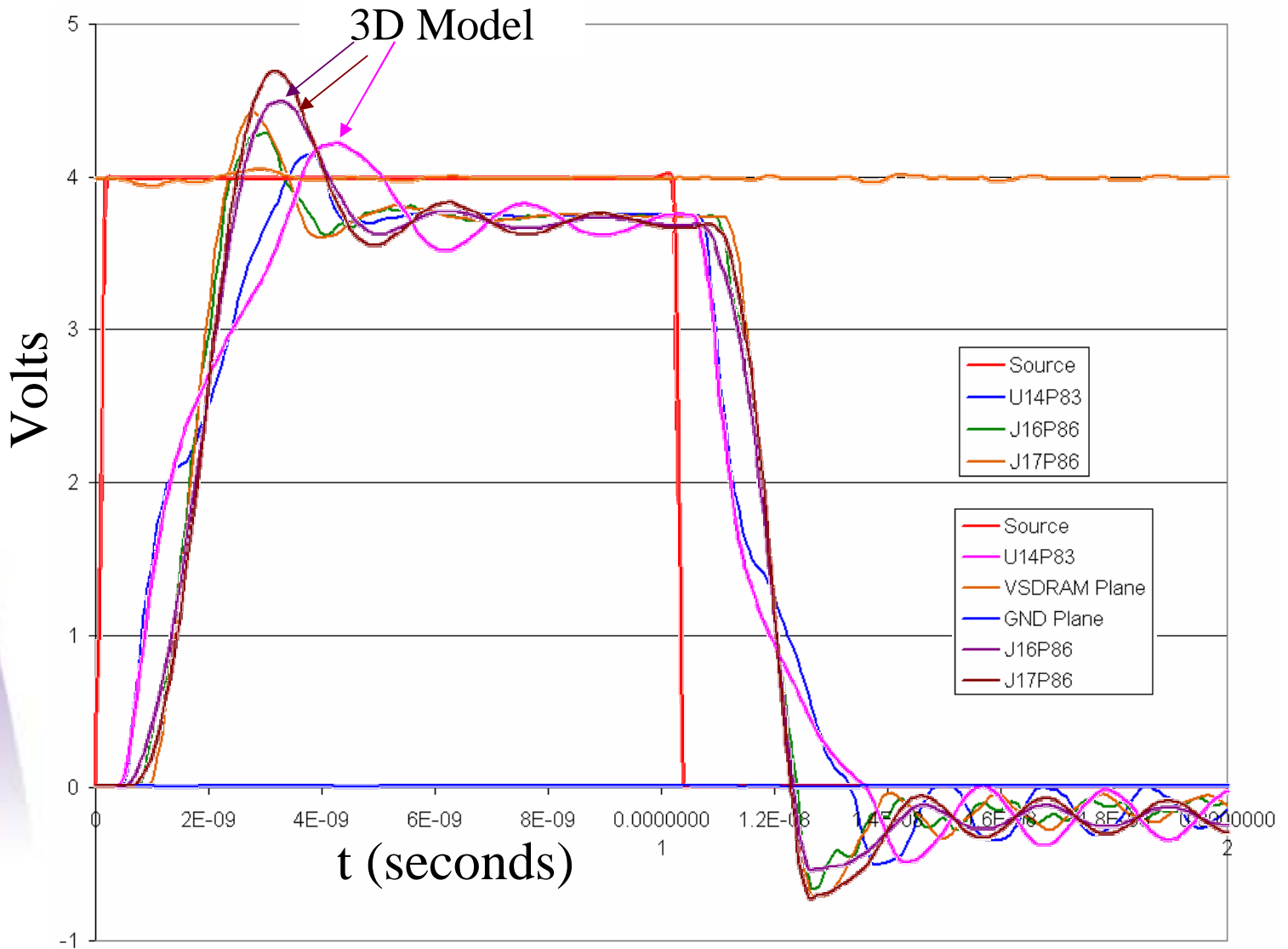
# IBIS Driver/Receiver with Mixed 2D/3D model



# IBIS Driver/Receiver with 3D model



# IBIS Waveforms



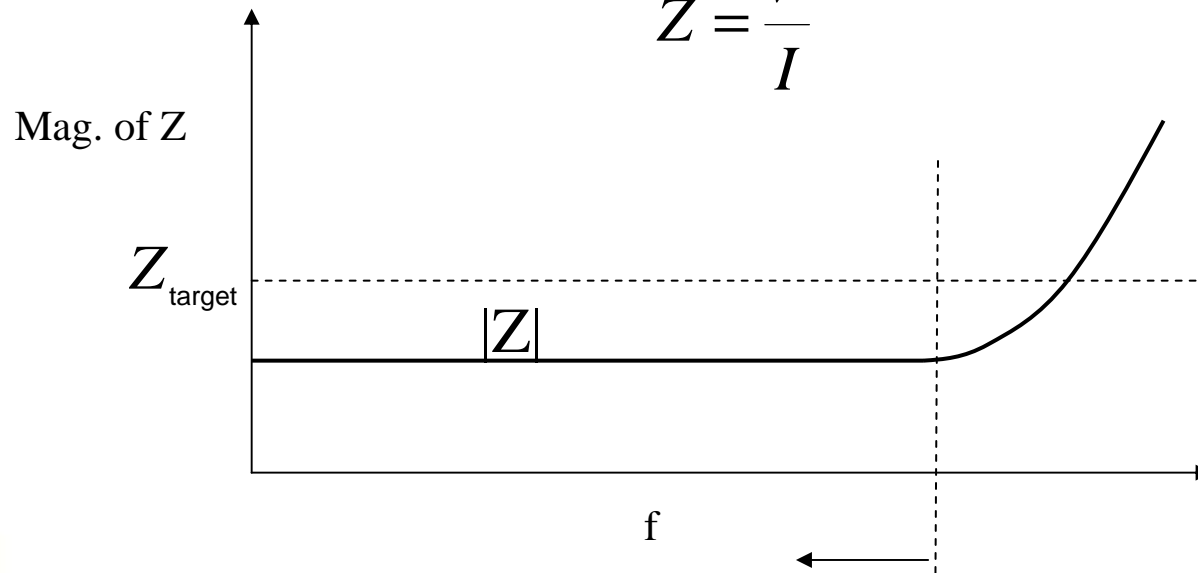
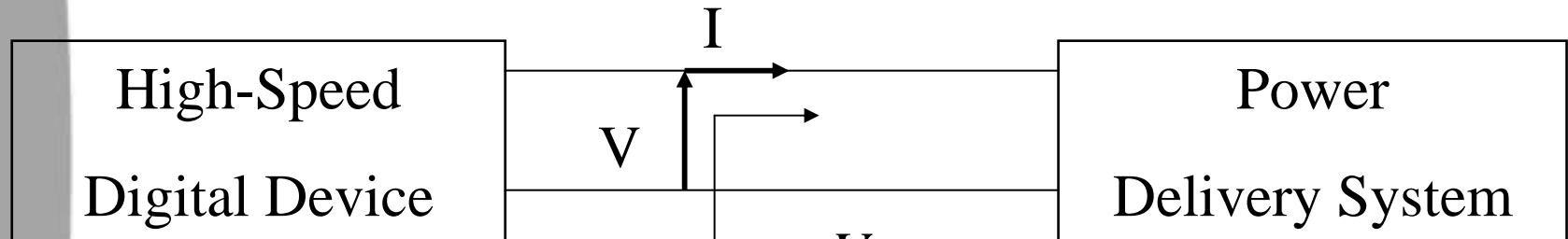
# What did we learn?

- How PCB/MCM is tightly integrated with Allegro
- How automatically mixed 2D and 3D extractions are performed
- How single net and multiple net simulations are performed
- How Crosstalk simulations on a victim net can be seen
- How differential signaling can be performed
- How the 3D PEEC model compared with the mixed 2D/3D simulations using an IBIS model

# **Design/Analysis for Power Delivery System (PDS)**



# The Impedance of PDS

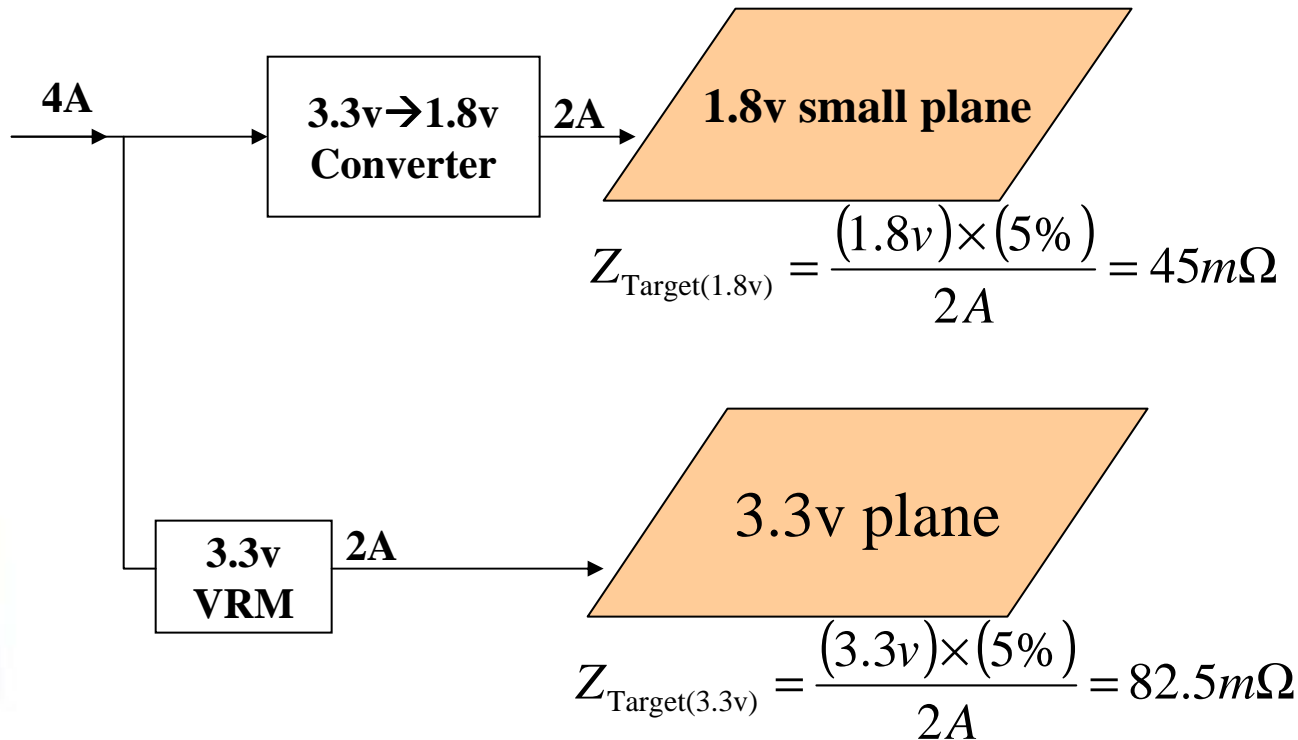


The Impedance see into PDS at the device should keep low from DC to several harmonics of clock frequency!

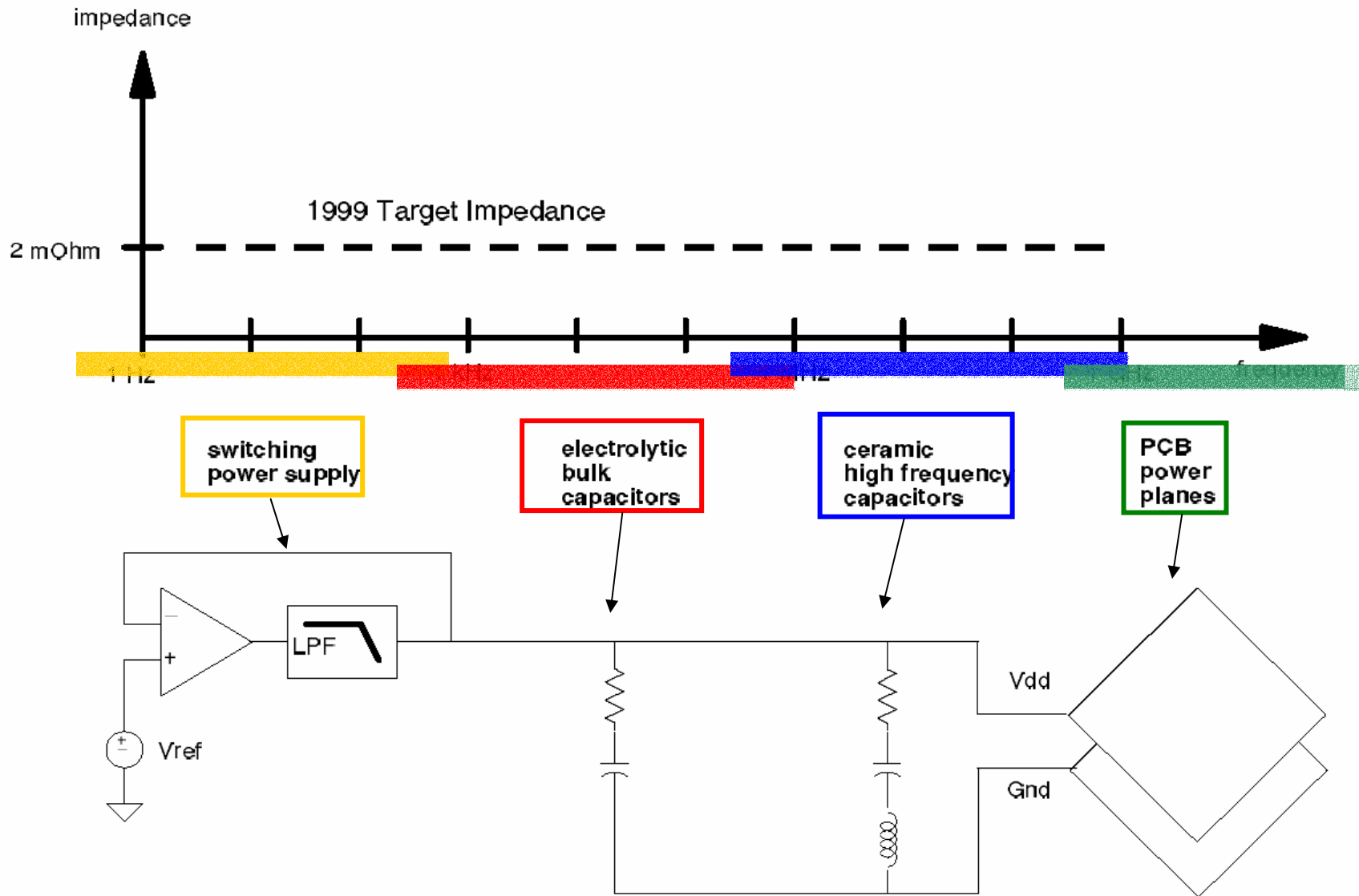
# Target Impedance Calculation

$$Z_{\text{Target}} = \frac{(\text{Power Supply Voltage}) \times (\text{Allowed Ripple})}{\text{Current}}$$

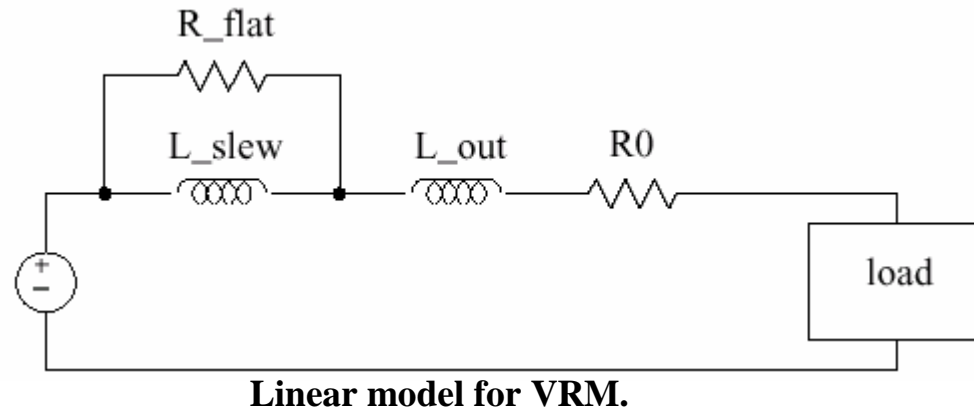
## Hardware Example



# PDS Components



# Voltage Regulator Module (VRM)



**$R0$ :** the value of the resistor between the VRM sense point and the actual load and is usually only a few mOhms

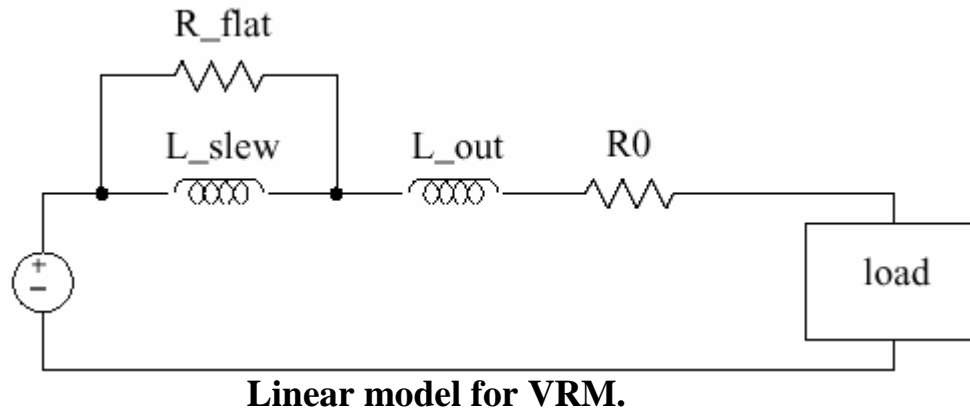
**$L_{out}$ :** the output inductance of the VRM

**$R_{flat}$ :** the ESR of the capacitor associated with the VRM

**Ideal voltage source** has the value of the power supply voltage

**$L_{slew}$**  is chosen so that current will be ramped up in the linear model in about the same time that it is ramped up in a real VRM.

# Voltage Regulator Module (VRM)

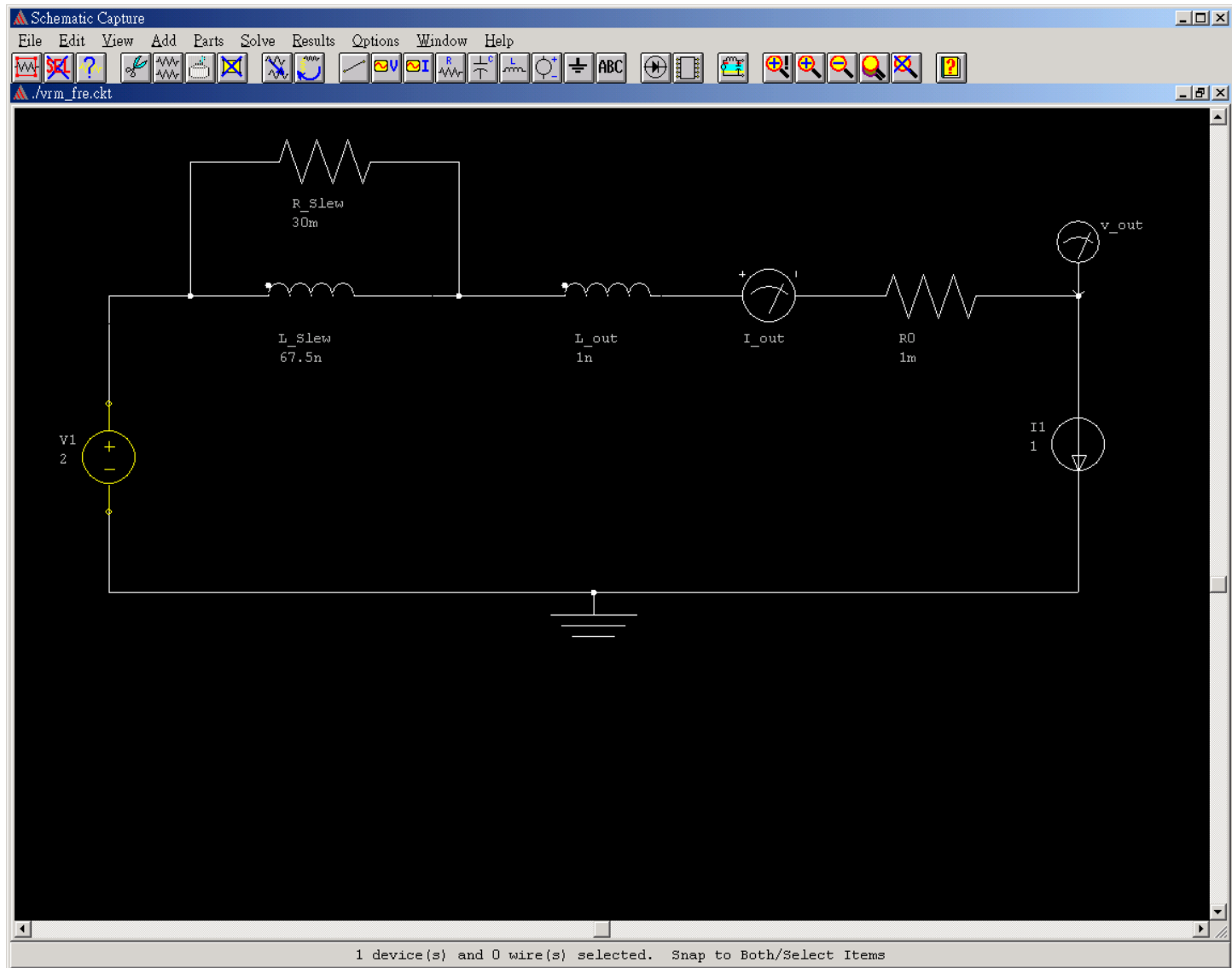


$$\begin{aligned}R_0 &= 1\text{mohm} \\L_{\text{out}} &= 4\text{nH} \\R_{\text{flat}} &= 30\text{mohm} \\L_{\text{slew}} &= 67.5\text{nH}\end{aligned}$$

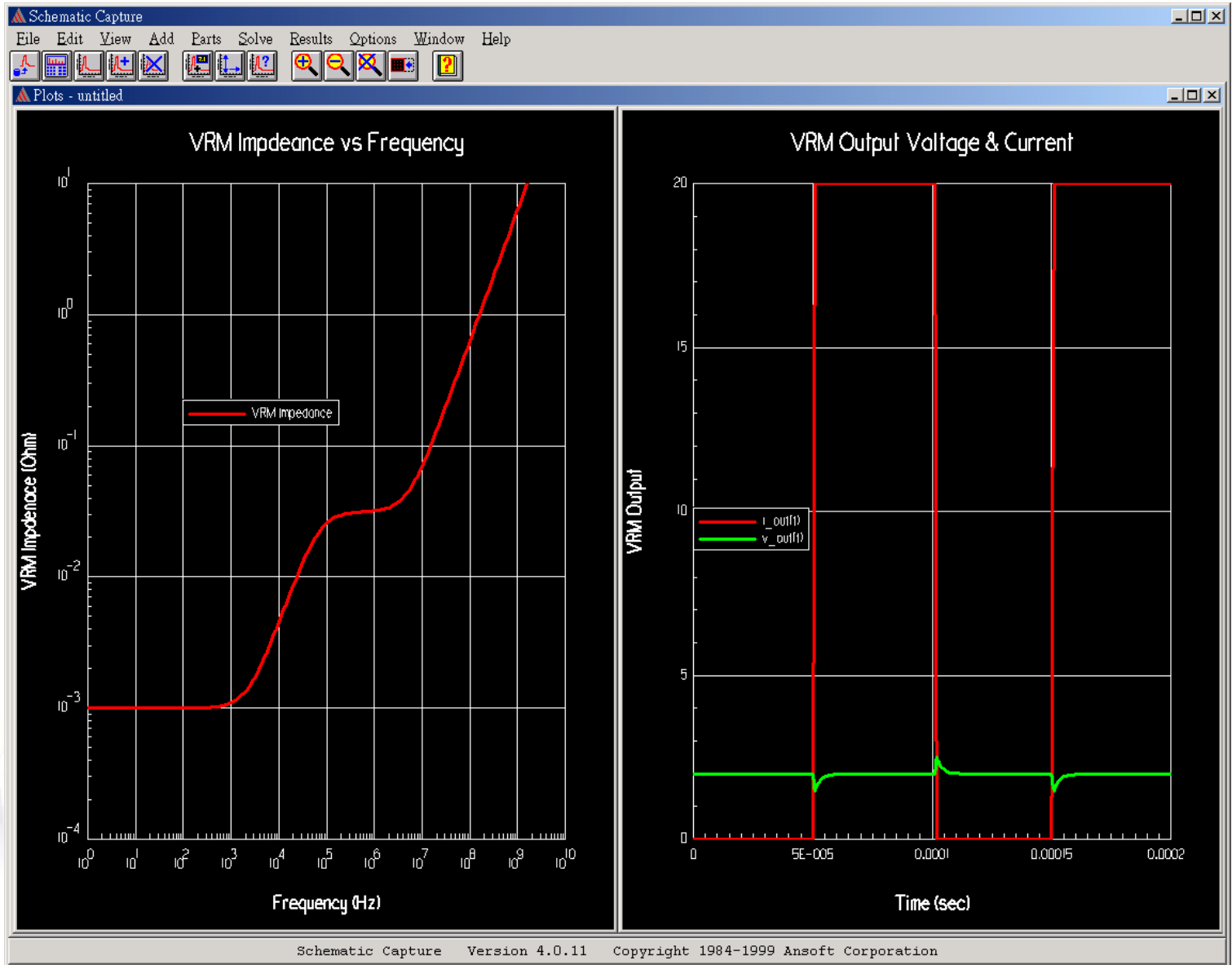
- ◆  $V = L \cdot di/dt$
- ◆ For a VRM to ramp this 20 A transient current either up or down in 15 us

$$L_{\text{slew}} = \frac{V}{\frac{di}{dt}} = 0.05 \cdot 1.8 \text{ V} \cdot \frac{15 \mu\text{sec}}{20 \text{ A}} = 67.5 \text{ nH}$$

# Simulation for VRM



# Simulation for VRM (cont'd)

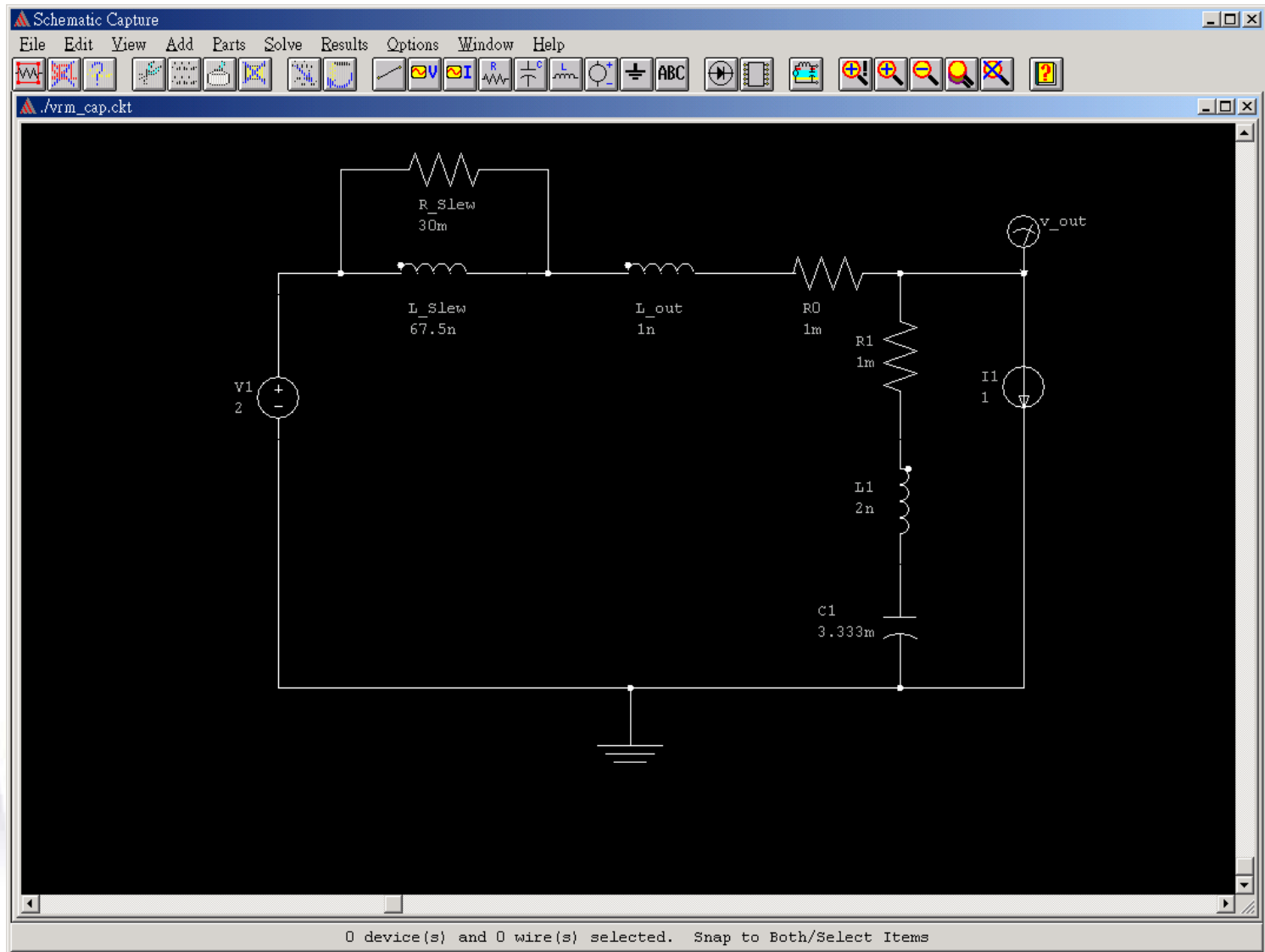


# Bulk Capacitor

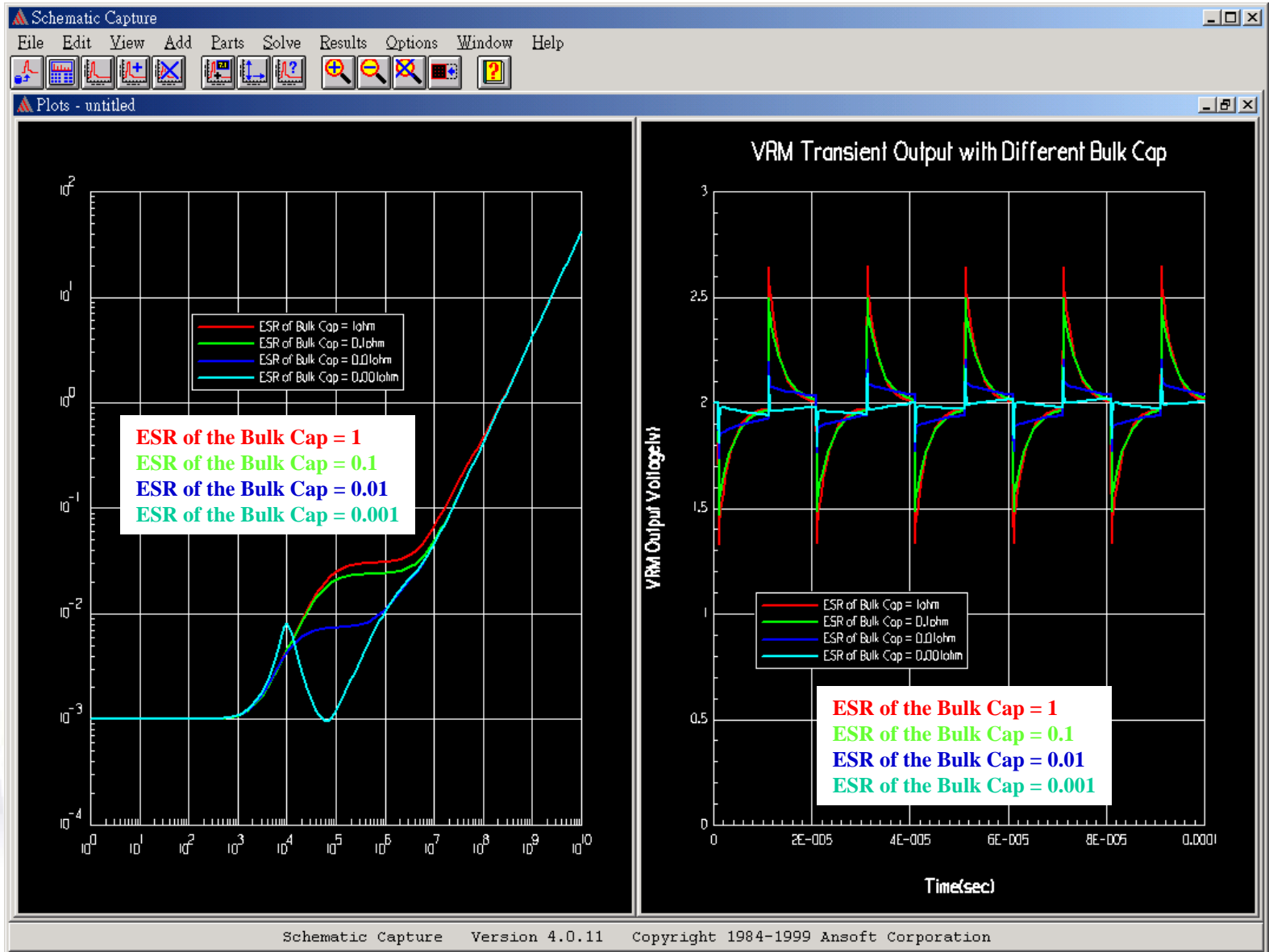
- $I = C \cdot dv/dt$
- **Suppose there is a 20 A current transient, the VRM responds in 15us, and the PDS must remain within 5% of a 1.8V power supply**

$$C = \frac{I}{\frac{dV}{dt}} = 20 \text{ A} \cdot \frac{15 \mu\text{sec}}{1.8 \text{ V} \cdot 0.05} = 3333 \mu\text{F}$$

# Simulation for VRM + Bulk Cap



# Simulation for VRM + Bulk Cap (cont'd)



# Simulation Impedance using Serenade Tune Mode

Serenade Desktop - vrm1 - d:\bull\_pjt\vrml\vrml.sch

File Project Edit Parts Draw View Settings Analysis Reports Tools Window Help

Wire Symbols

Mag(Z11(ckt=vrm1))

Ansoft Corporation - Harmonica ?v8.71

d:\bull\_pjt\vrml\vrml1.ckt

Mag(Z11(ckt=vrm1)) [Ohm]

FREQ [Hz]

X1= 5.28EC  
Y1= 1.03E-

vrm1Y  
Mag(Z11)  
r = 0.010

vrm1Y  
Mag(Z11)  
r = 0.001

vrm1Y  
Mag(Z11)  
r = 0.10h

Tune

\\Ckt\SymbolParam Orig Val ==> Applied Val

\\vrm1\mhres#6jr	1e-0930h
------------------	----------

Add Add All Remove Clear

Type

Step

Single Point/List

Sweep

Start: 1E-01 Oh

End: Oh

Step: 10 % Oh

Apply Manual Scaling To Graphs

Tune Analysis for 0.10h is Complete.

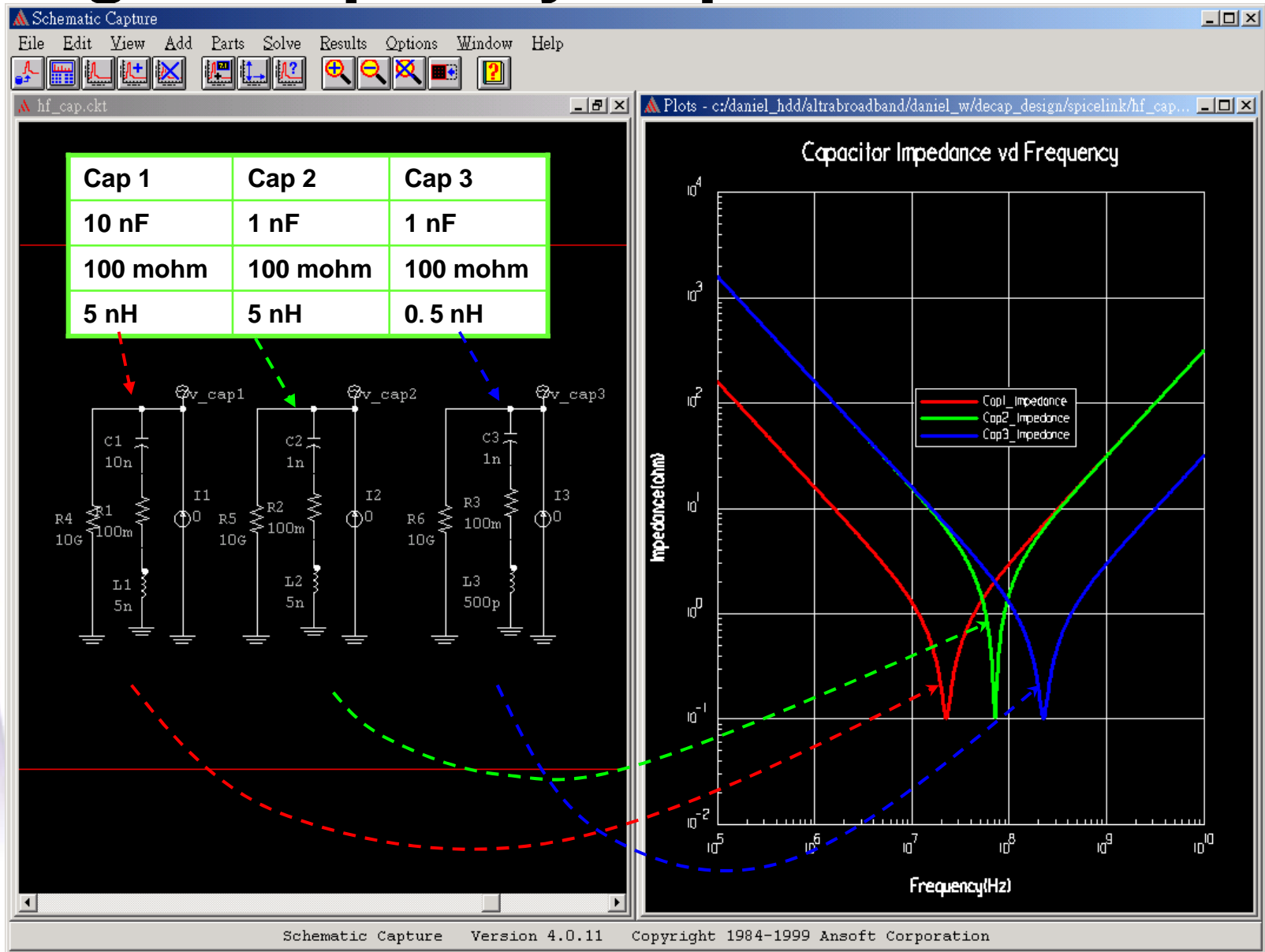
Tune Incr Decr Apply Revert Abort Done

Wire Symbols (46, 65) SELECT | REPEAT | MENU (-482, 78) | SGrid:16 NONE | VGrid:16

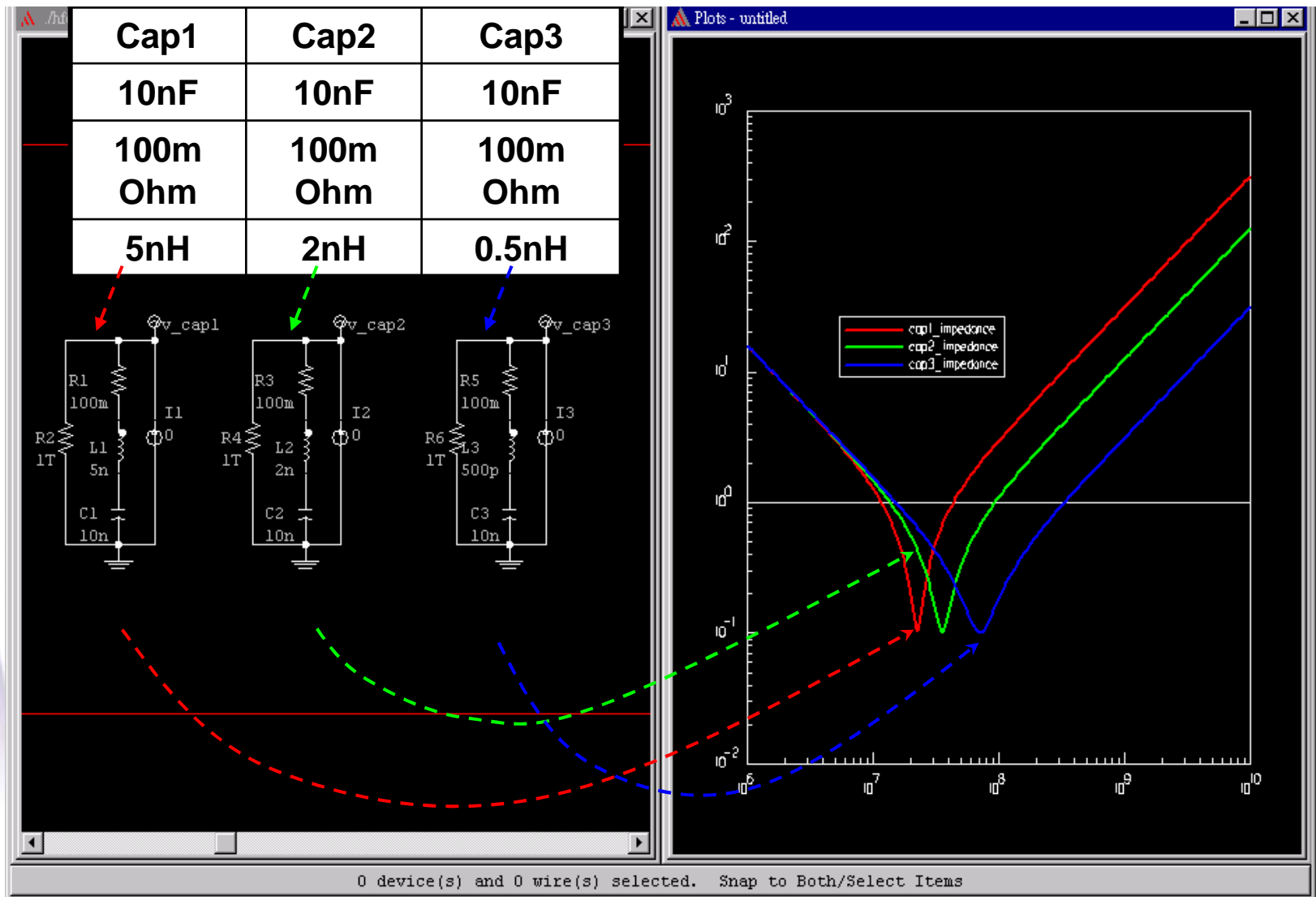
# High Frequency Ceramic Capacitor

- **NPO** capacitors have the **lowest ESR** and **best temperature and voltage properties**, but are **only available up to a few nF**.
- **X7R** capacitors have reasonable voltage and temperature coefficients and are **available from several nF to several uF**.
- **X5R** is **similar to X7R**, but with **reduced reliability** and are being **extended to 100uF**.
- **Y5V** dielectric is used to achieve high capacitance values, but has **very poor voltage and temperature characteristics**.

# High Frequency Capacitor

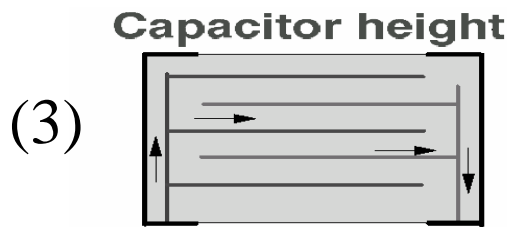
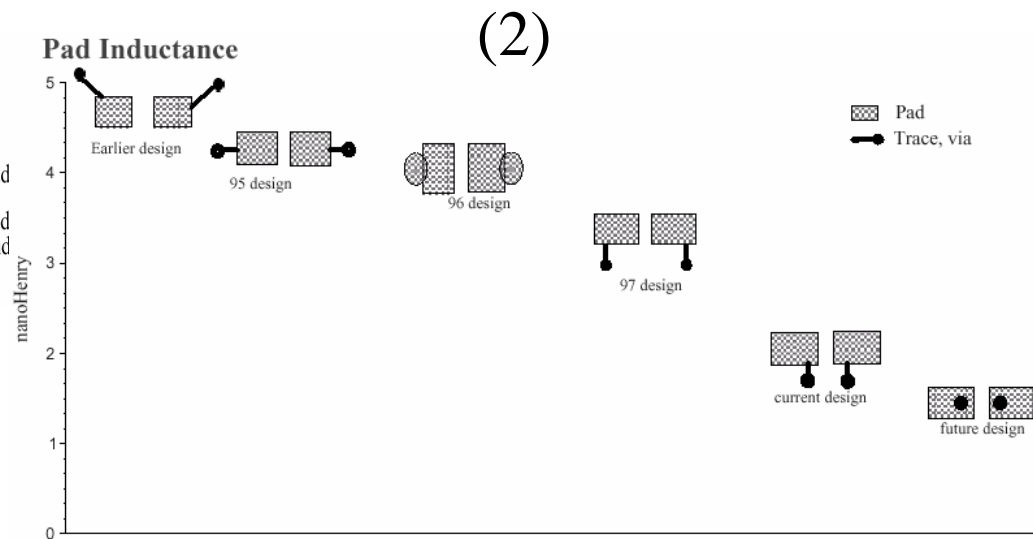
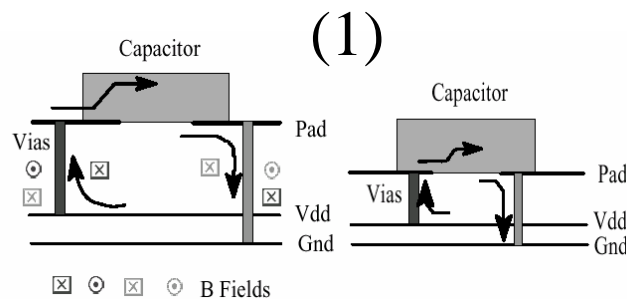


# High Frequency Capacitor



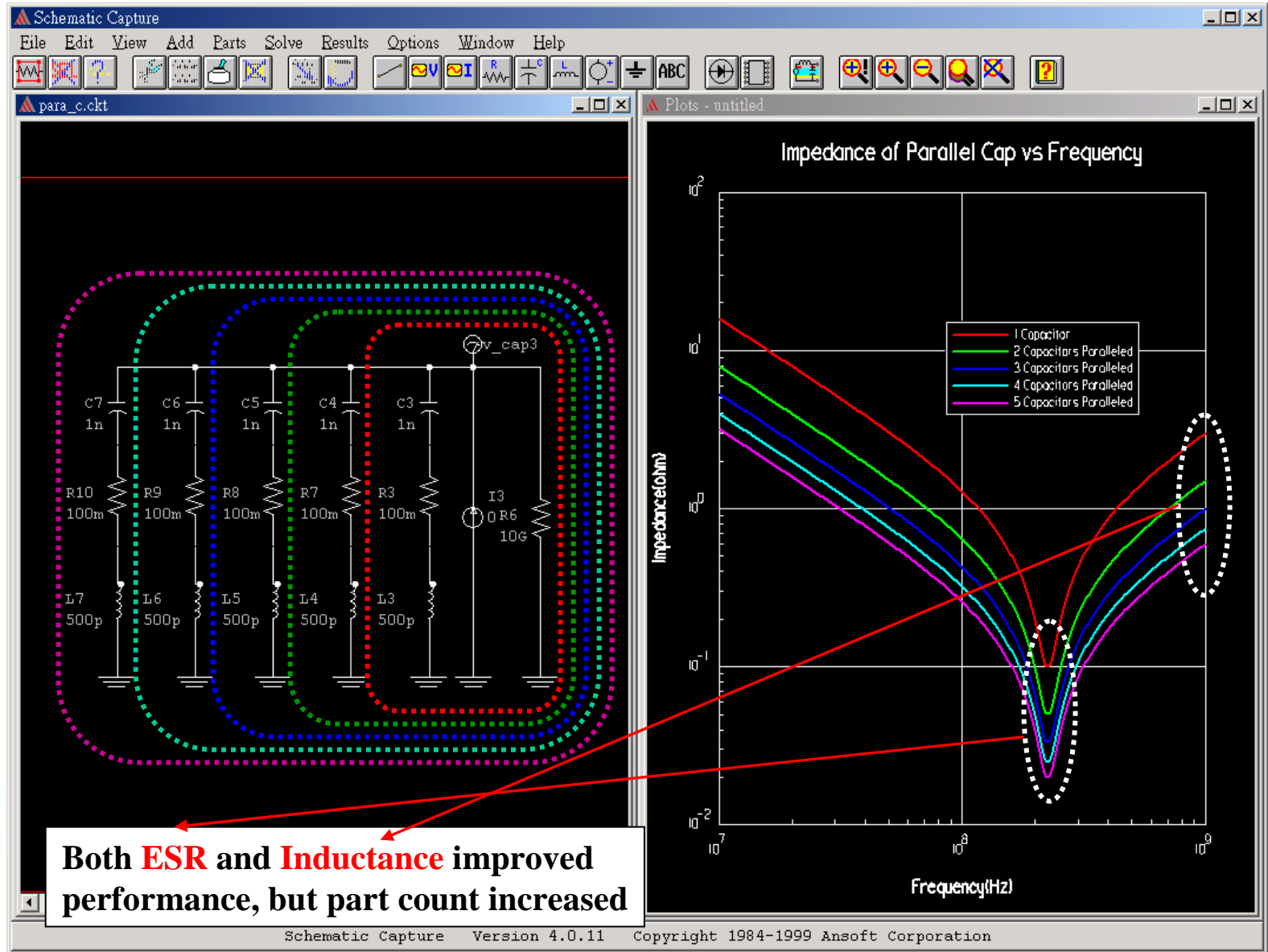
# Reducing the Parasitic Inductance for HF Cap

1. Reduce the length of via for decoupling capacitors (i.e.reduce the loop inductance)
2. Change the layout of decoupling capacitors
3. The thickness of high frequency capacitors
4. Parallel the decoupling capacitors with same value or multiple skew values

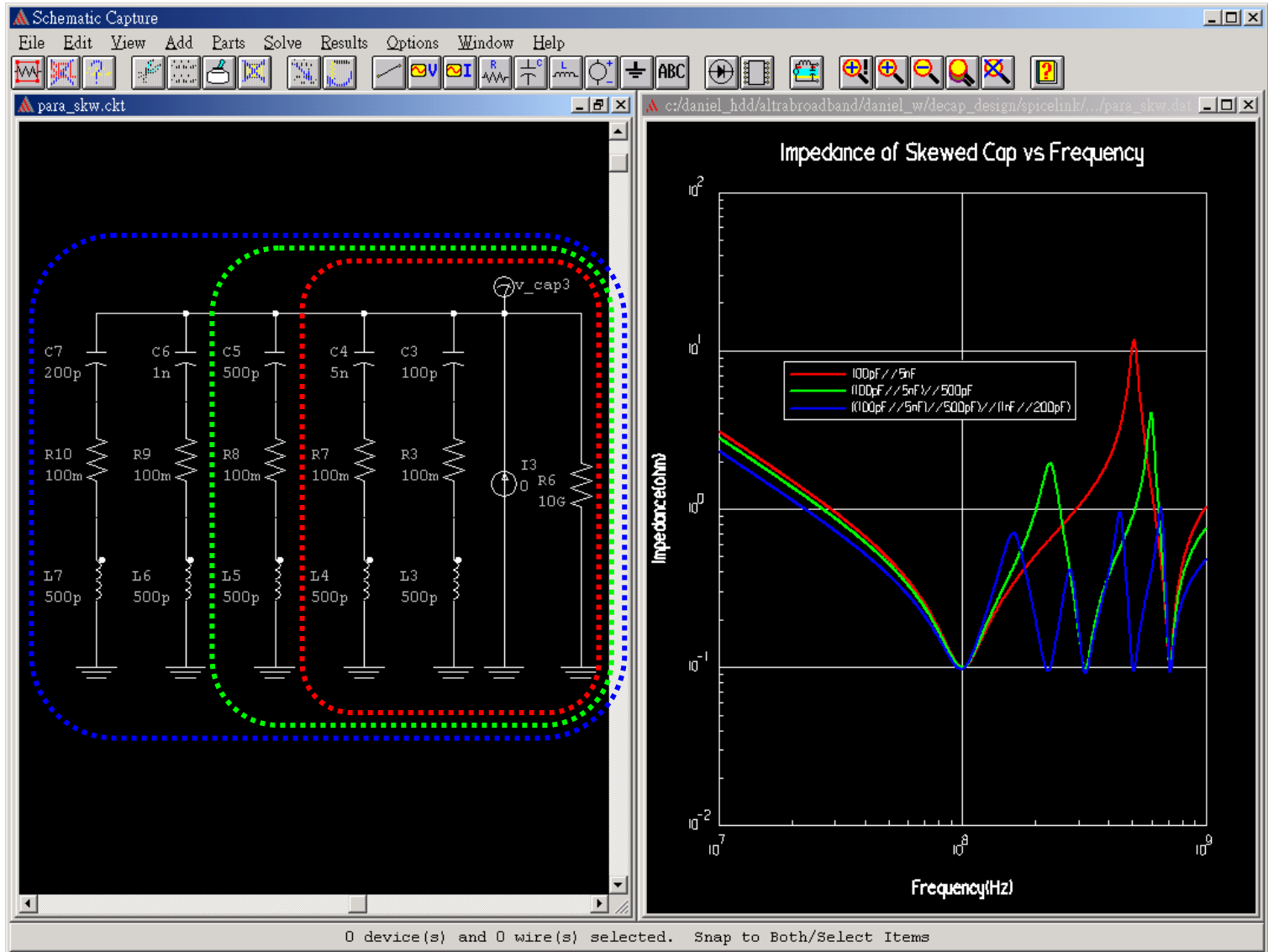


Thickness(mils)	Inductance(pH)
20	300
30	450
40	600
50	700

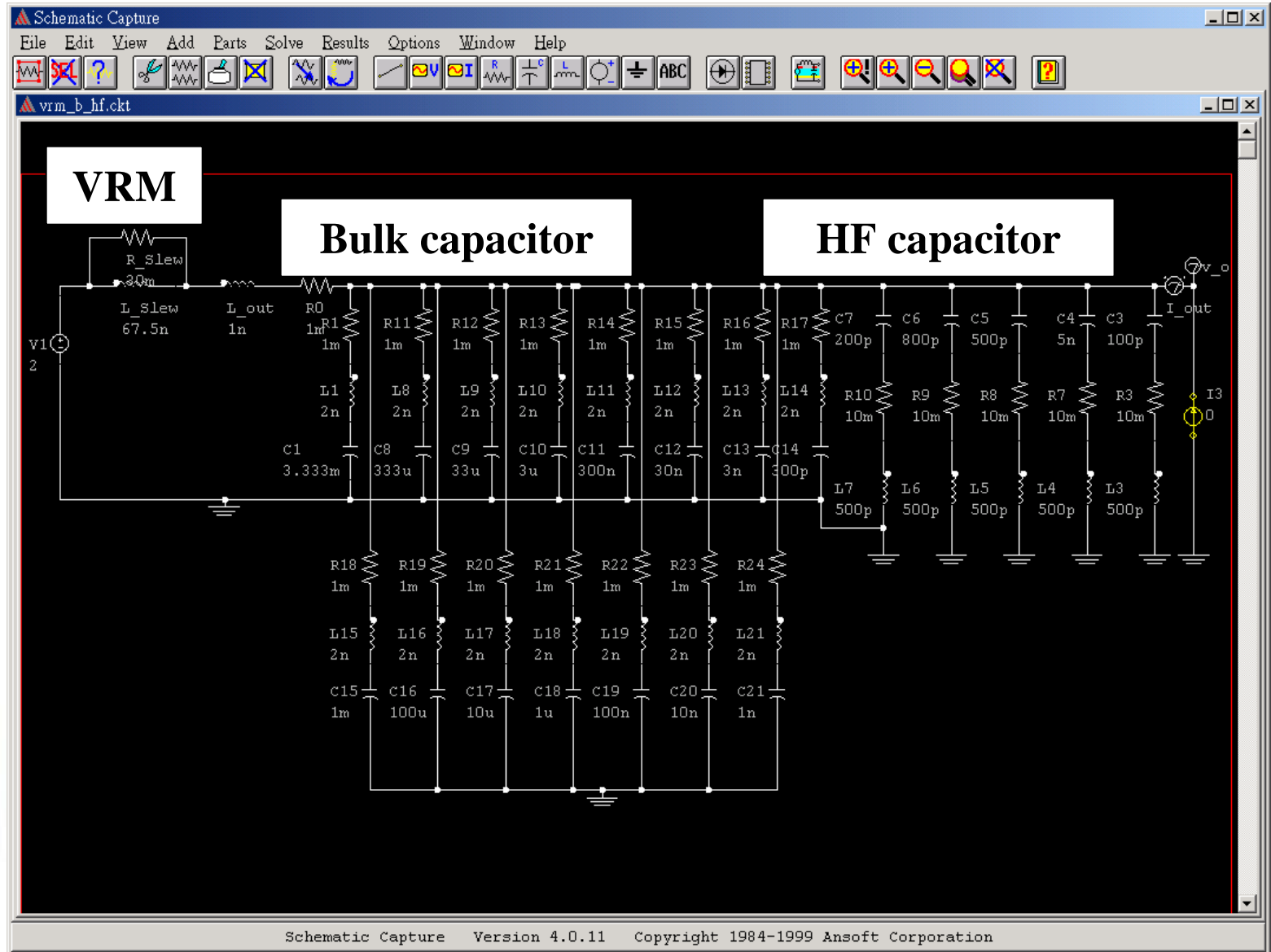
# Simulation for Impedance of Parallel Capacitors



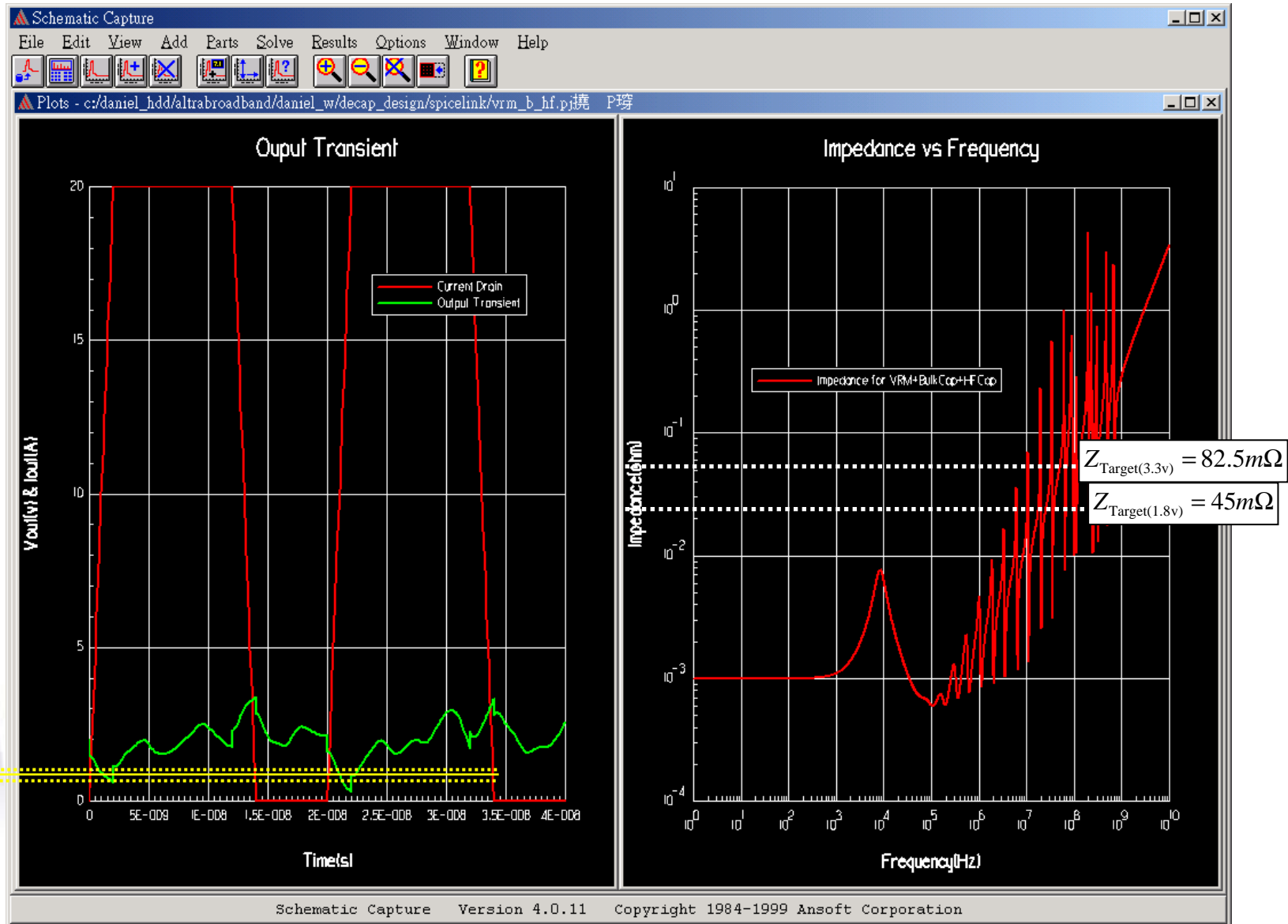
# Simulation for Impedance of Parallel Capacitors with Skewed Capacitance



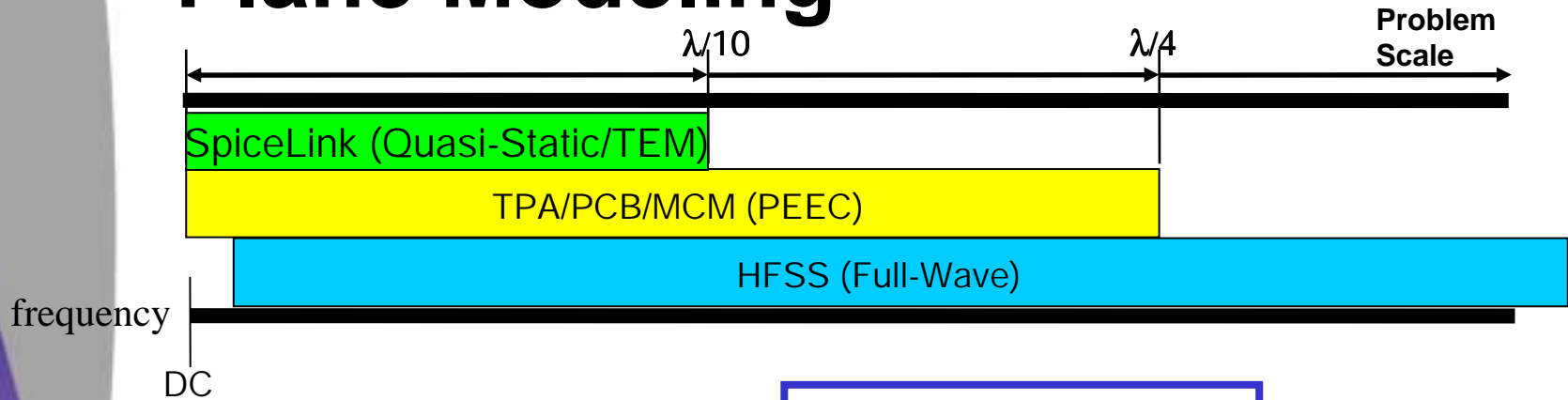
# Simulation for VRM+Bulk\_cap+HF\_cap



# Simulation for VRM+Bulk\_cap+HF\_cap (cont'd)

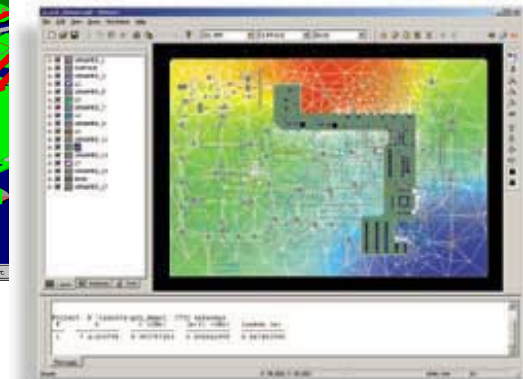
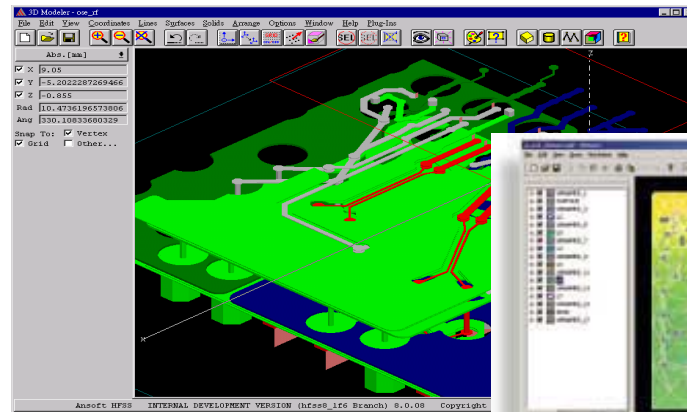
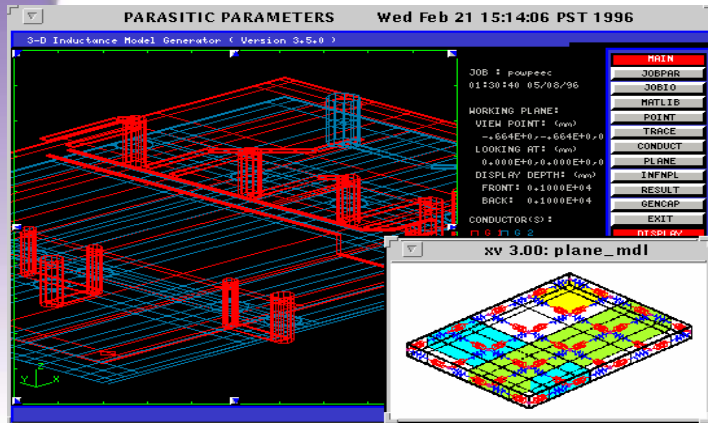


# Plane Modeling



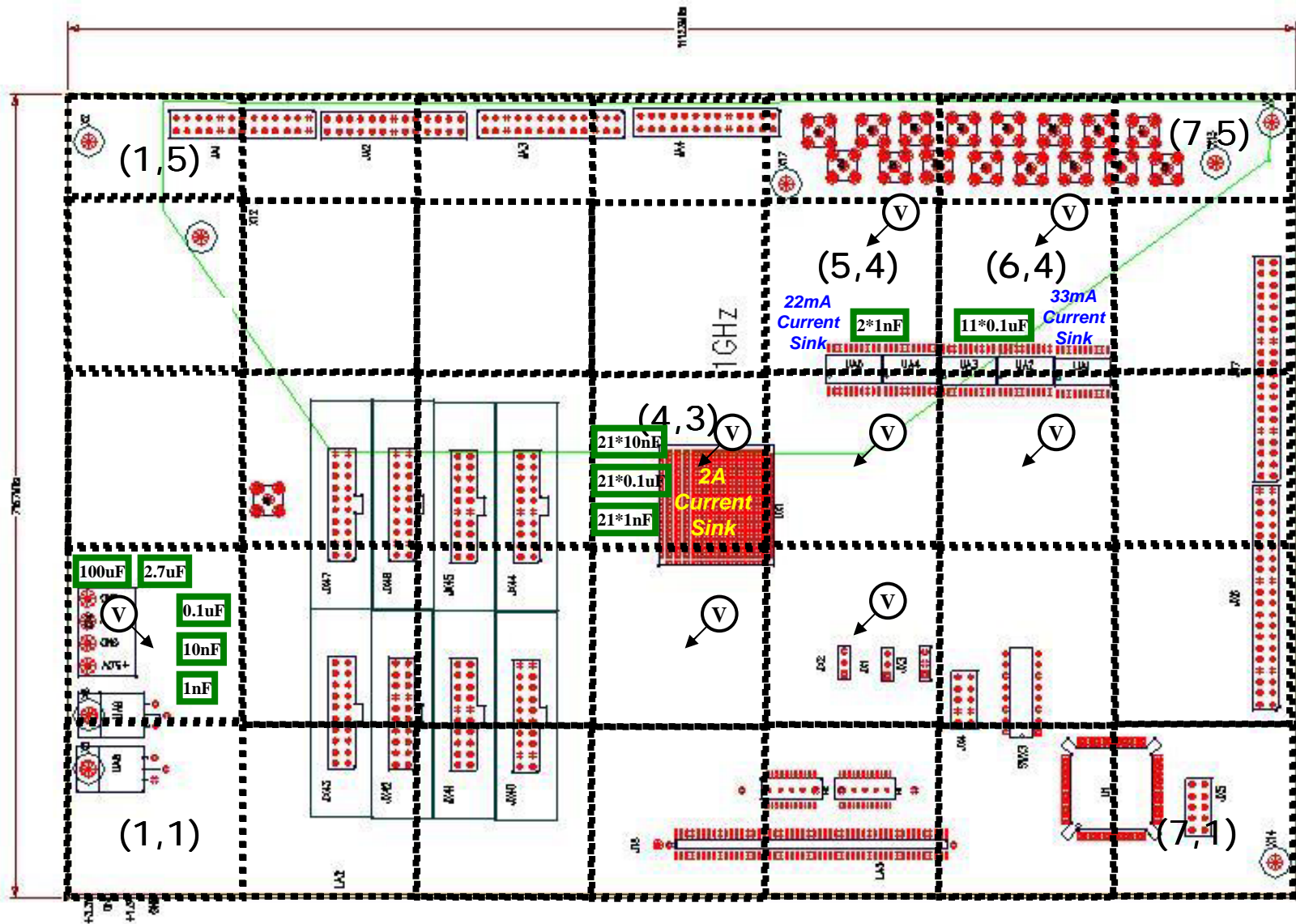
**3D Distributed  
PEEC**

**FULL WAVE  
HFSS+Full Wave Spice  
SI\_wave**

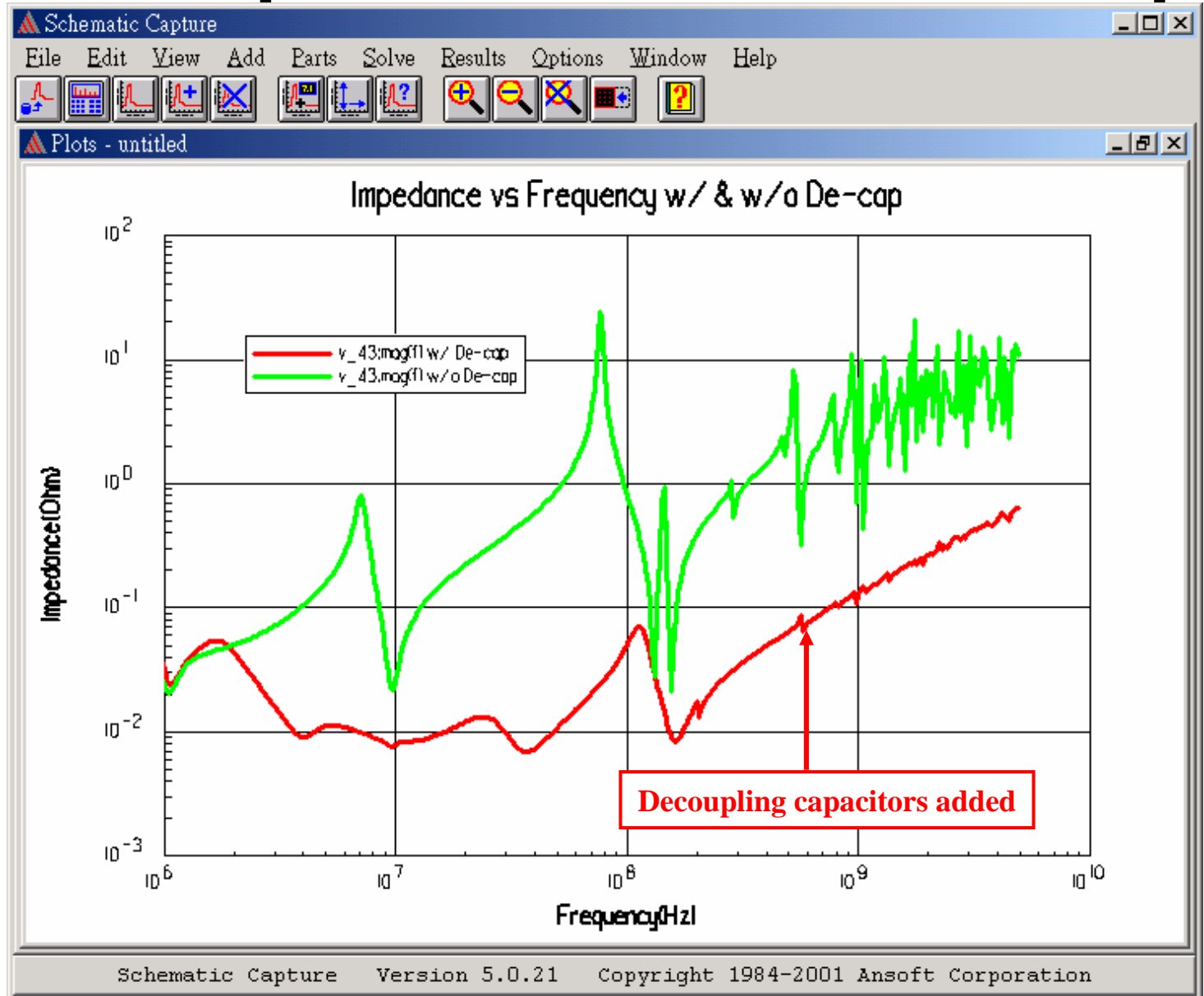


**Physical Design  
Using  
Full Wave Spice  
Model from HFSS**

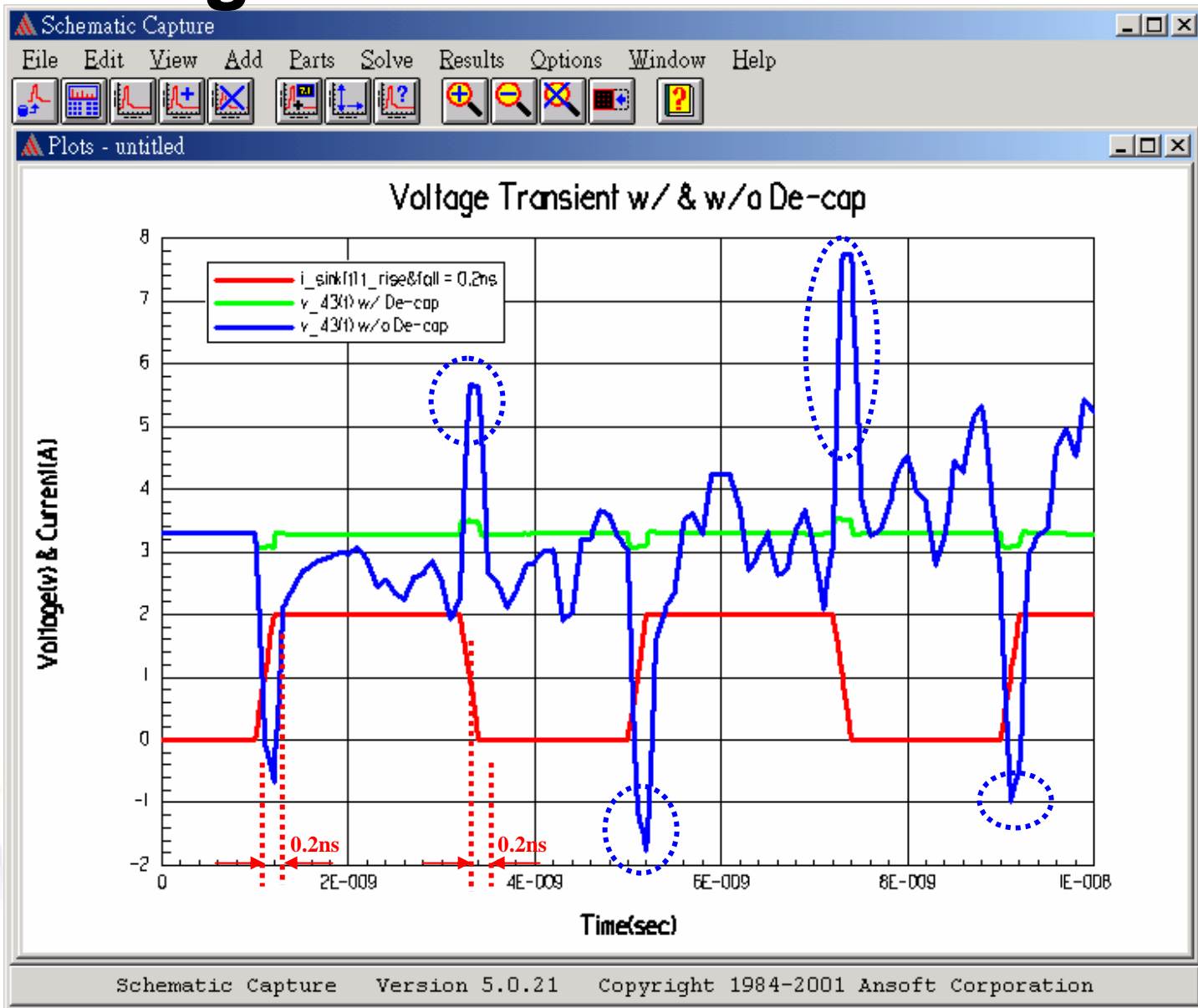
# 12 Layers PCB



# Plane Impedance w/ & w/o De-cap

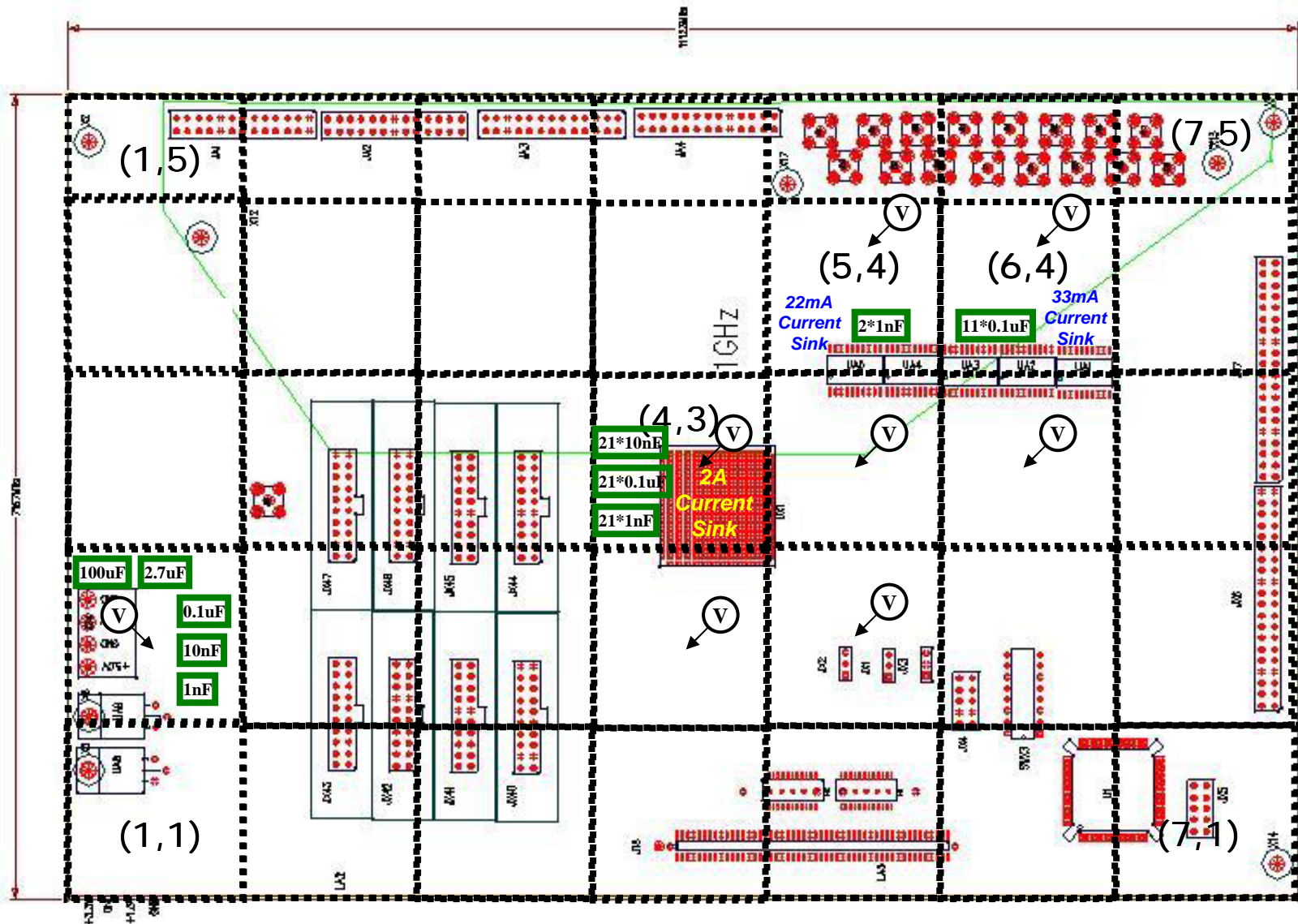


# Voltage Transient w/ & w/o De-cap

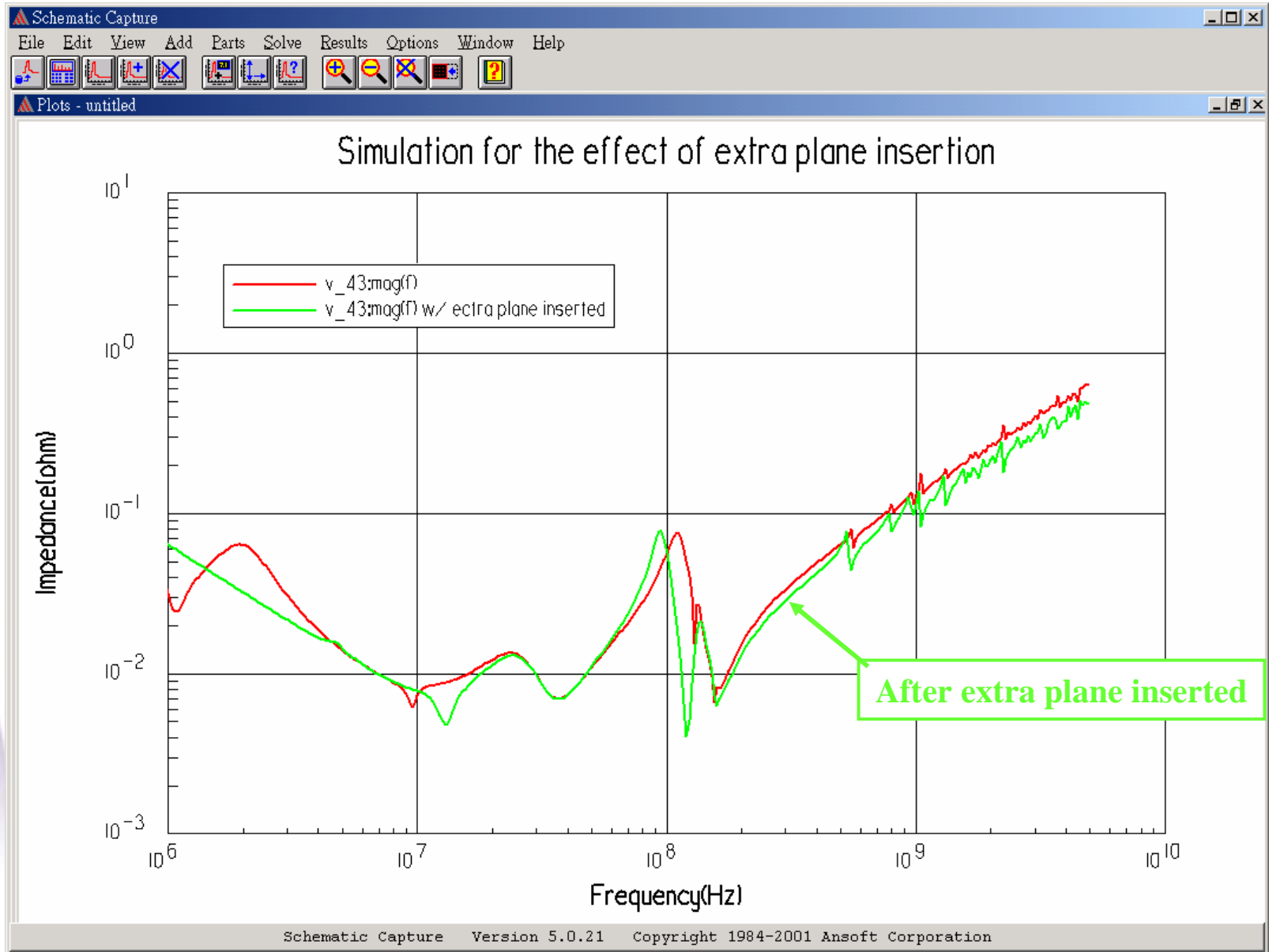


# Simulation for Extra AGND Plane Inserted

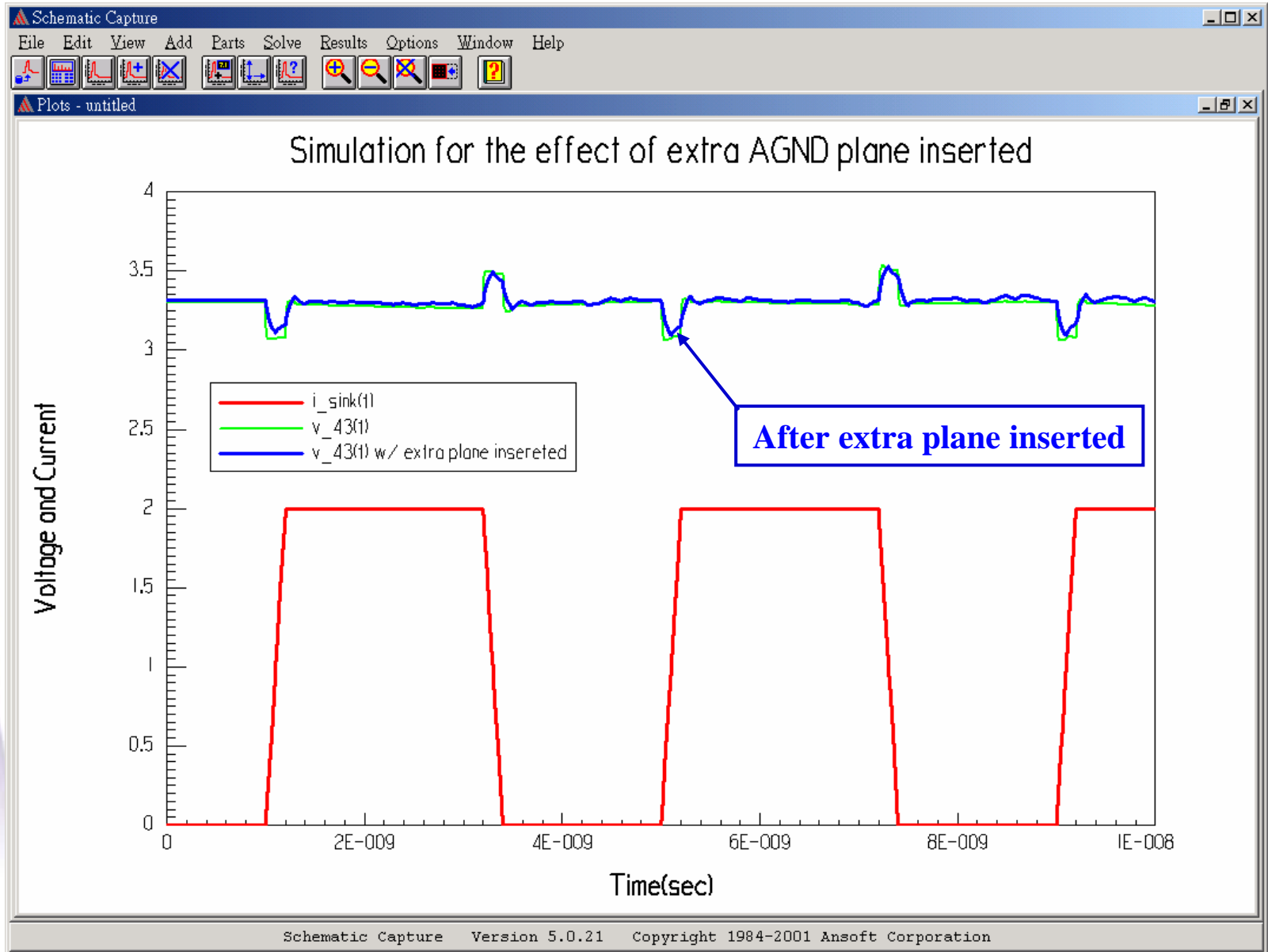
S1
AGND
S2
S3
AGND
AVCC 3.3v
S4
S5
DVCC 3.3v
S6
S7
DGND
S8



# Plane Impedance with Extra AGND Plane Inserted

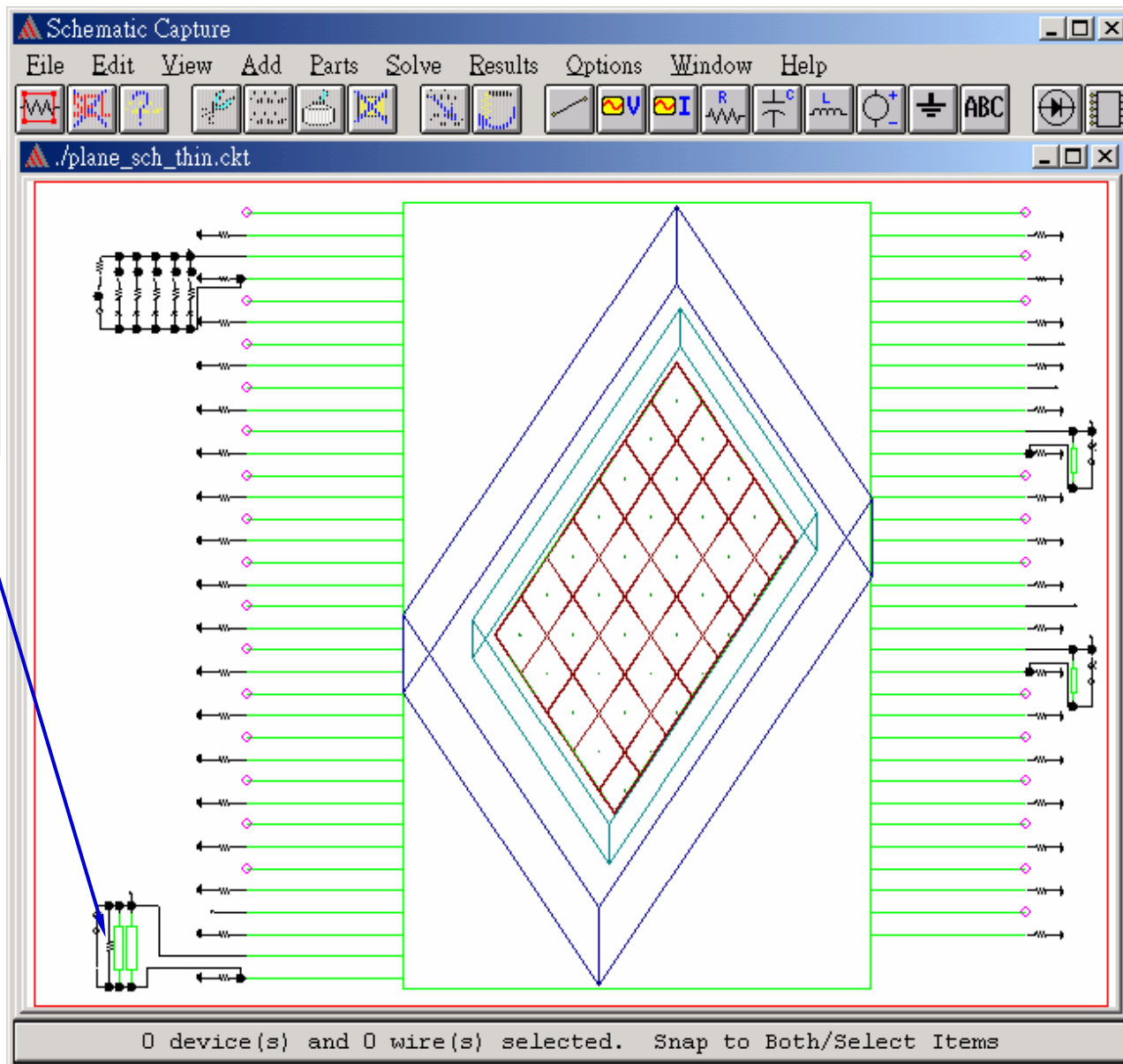


# Voltage w/ & w/o Extra AGND Plane Inserted

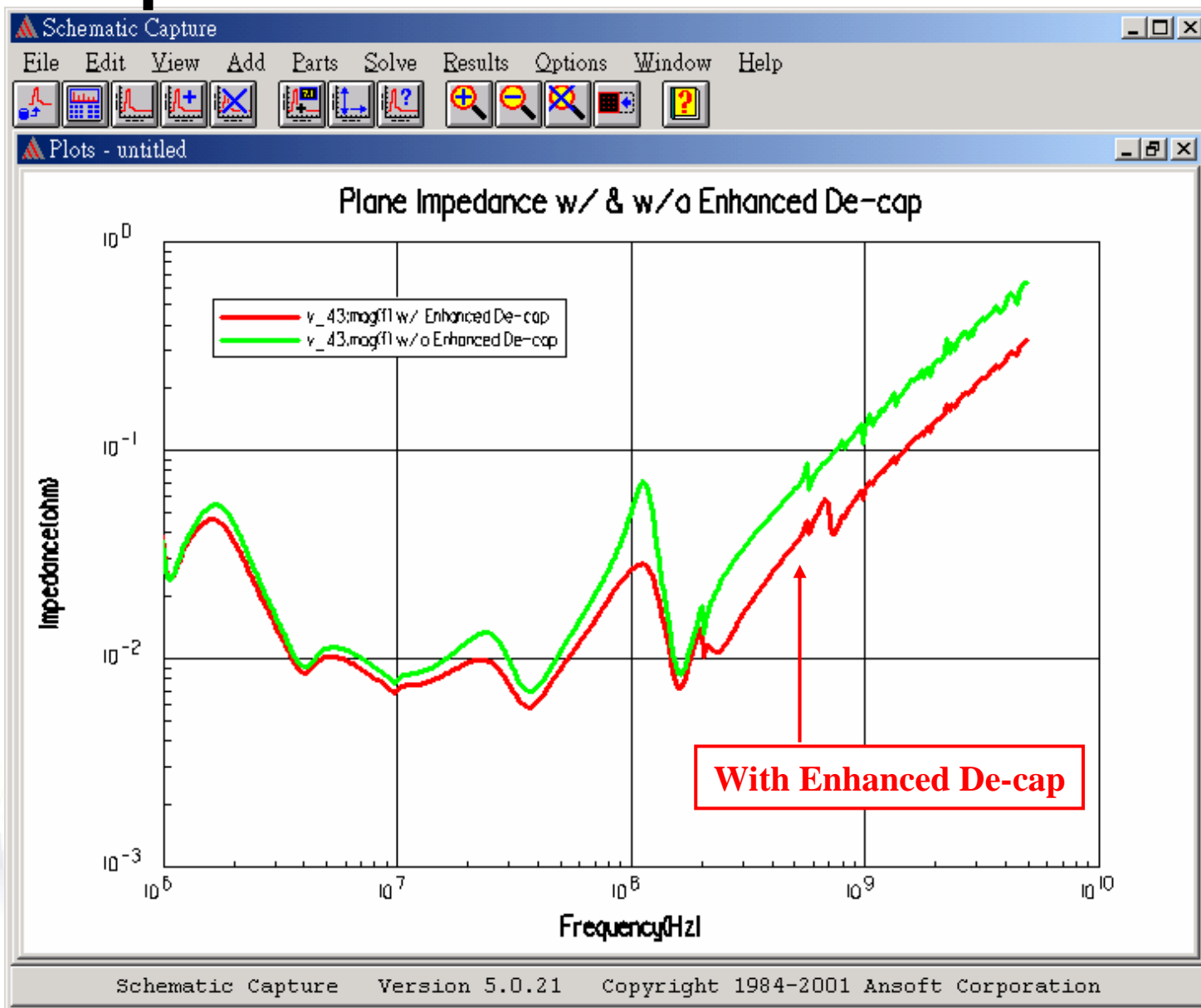


# De-cap Enhancement for HF Range

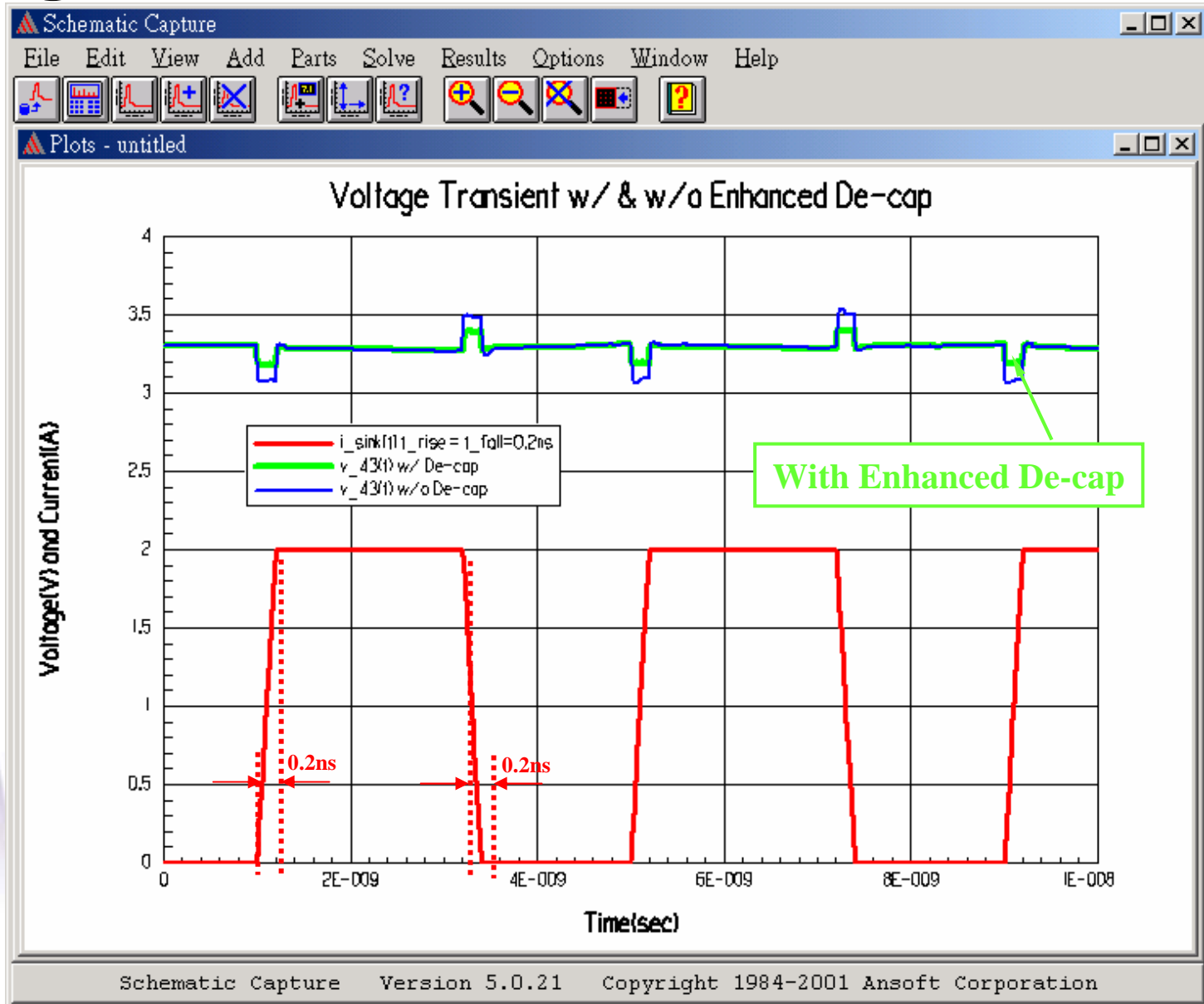
Enhanced de-cap:  
100nF\*2, 50nF\*2  
25nF\*2, 10nF\*2  
2.5nF\*2, 1nF\*10  
100pF\*2 are in parallel!!



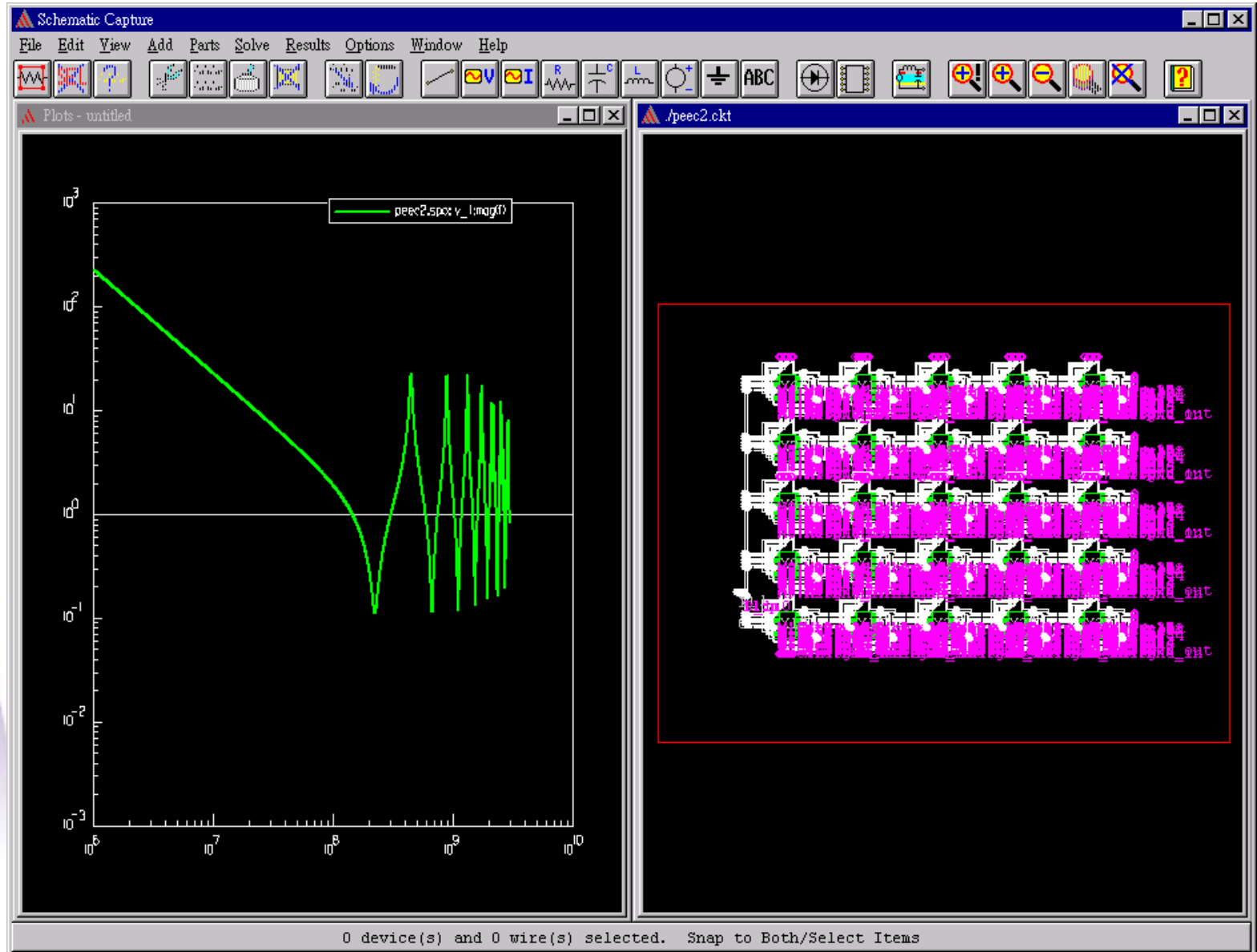
# Plane Impedance w/ & w/o Enhanced De-cap



# Voltage Transient w/ & w/o Enhanced De-cap



# Impedance Simulation using PEEC



# Summary

- ◆ Impedance control from DC to GHz:
  - ◆ Voltage Regulator Module (VRM)
  - ◆ Bulk Capacitor
  - ◆ High Frequency Ceramic Capacitor
  - ◆ PCB Planes
- ◆ Tools used for simulation:
  - ◆ Schematic Capture
  - ◆ Serenade
  - ◆ HFSS
  - ◆ PCB/MCM