

THE MISSING LINK IN TELECOM MEMS, TODAY.™

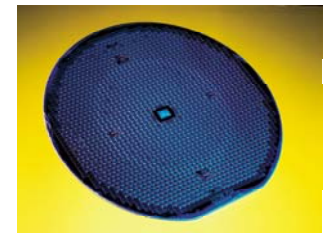
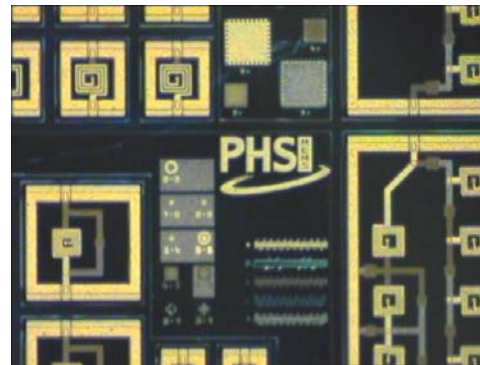
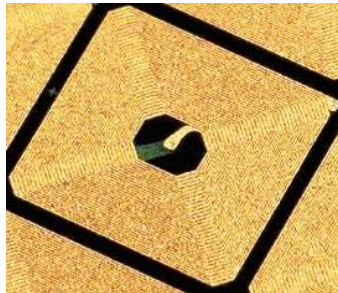


www.phsmems.com

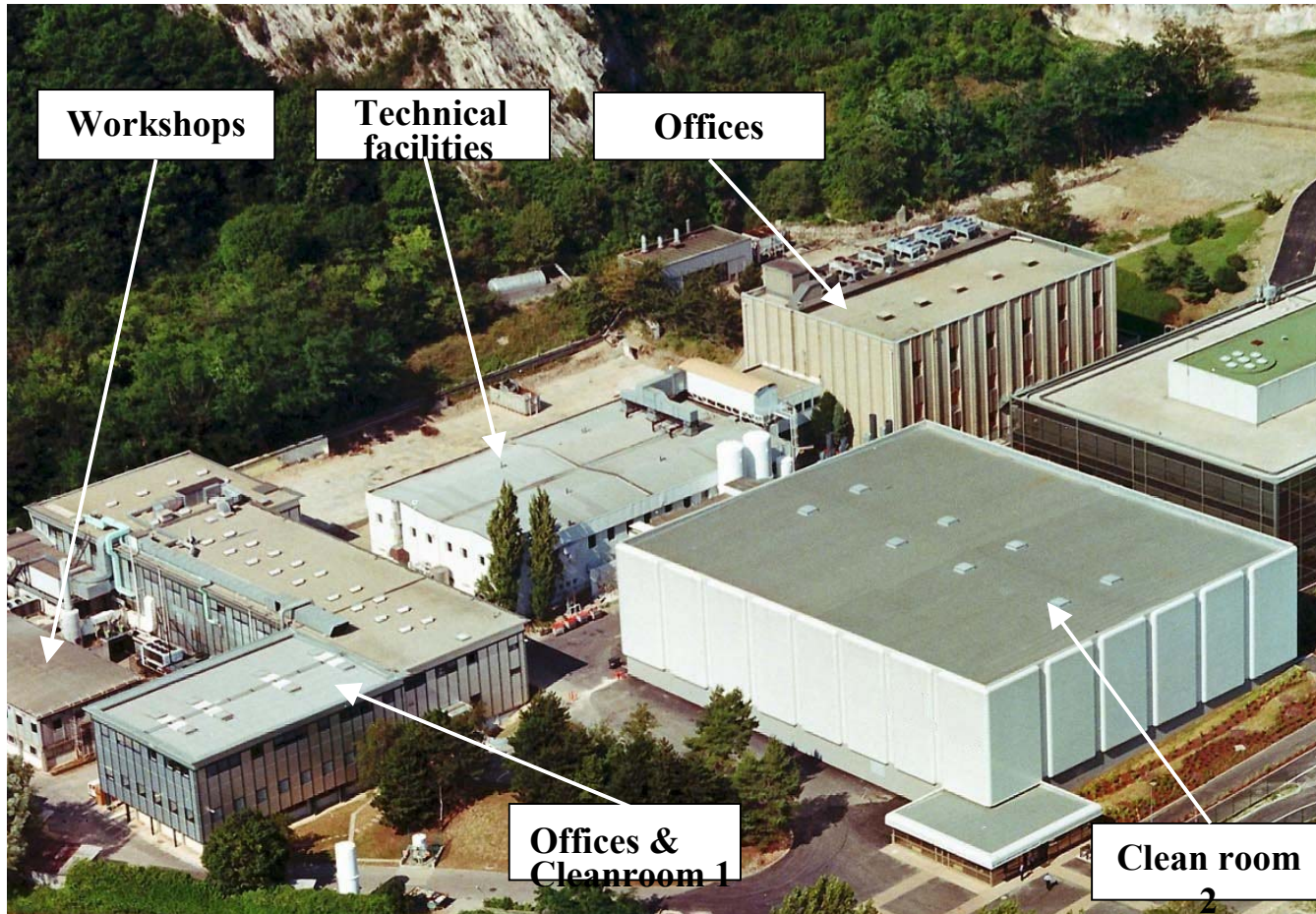
PHS MEMS

PHS MEMS: The company

- **Founded in August 1998 –Based in Grenoble, France**
- **82 employees -**
- **Production capacity ~12 000 wafers/month in 100mm**
 - 2 800 m² class 100 and 2 700 m² class 10 clean rooms
 - 280 MEMS manufacturing equipments
 - 100mm and 150mm wafers.
- **Design center : RF & Optical MEMS; MEMS packaging**
- **Process workshops :**
 - **Lithography, Etching, Chemistry, Deposition, Back- End, Test.**



PHS MEMS Facilities



Clean room 1

Wafer Fab 2800 m²
Class 100 Facility

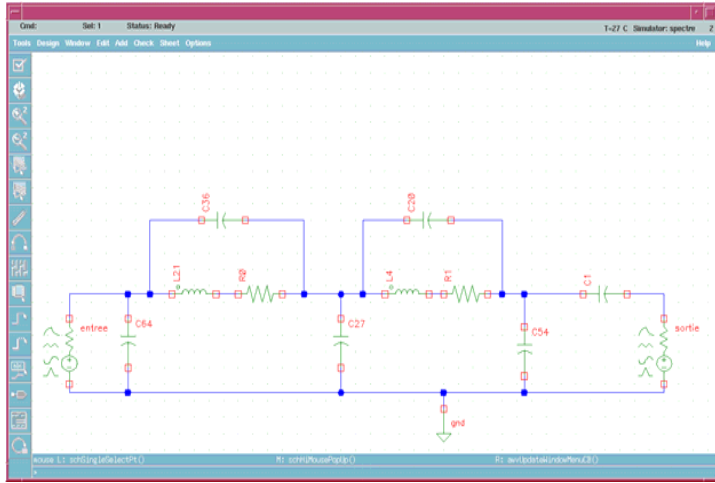
Clean room 2

Wafer Fab 2700 m²
Class 10 Facility

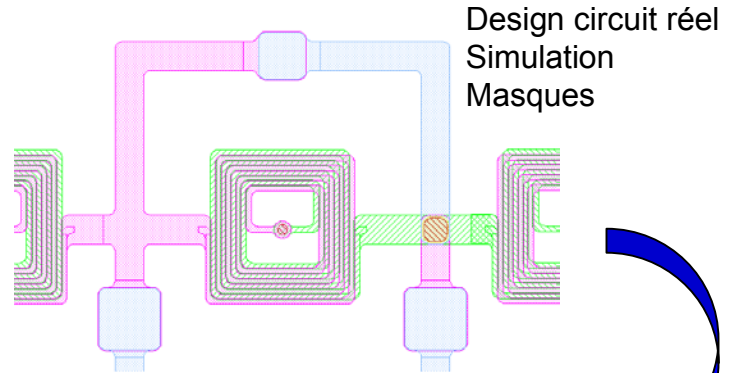
Manufacturing



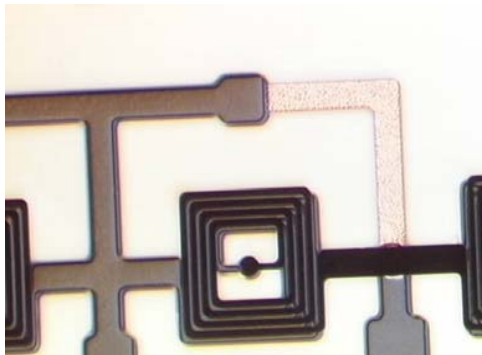
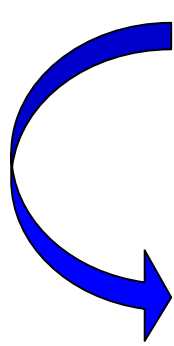
Integration de passifs.



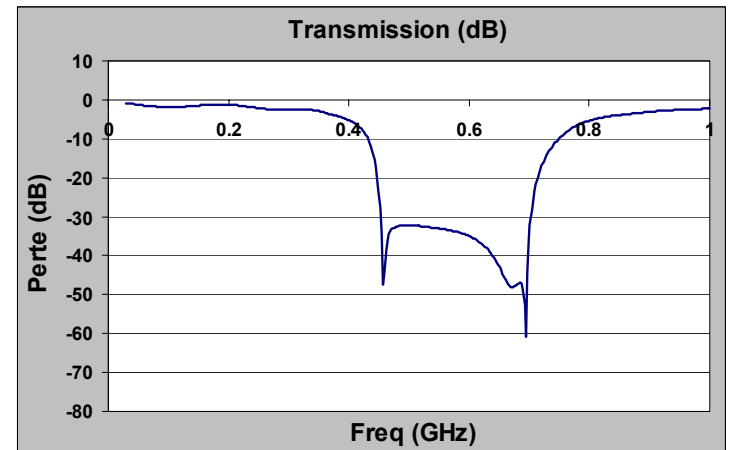
Cahier des charges
Schéma circuit idéal
Choix composants



Design circuit réel
Simulation
Masques



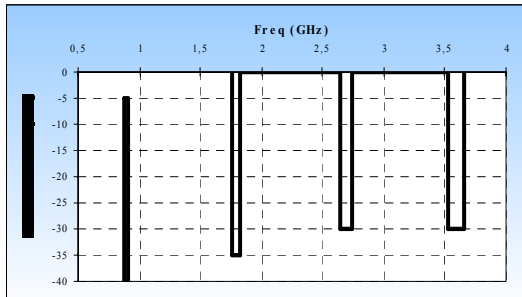
Protos
Test paramétrique



Test composants
Test circuit
Validation



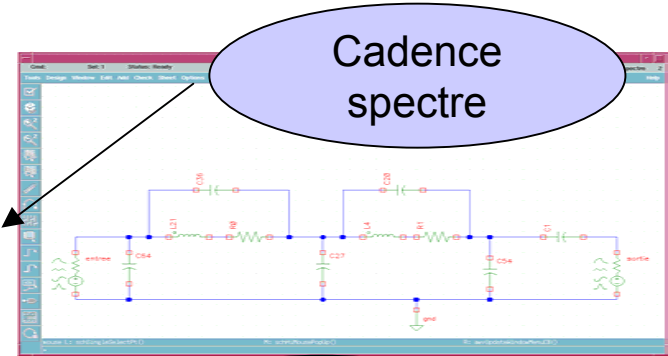
Conception-Phase 1 définition



Cahier des charges



Schéma circuit idéal



Cadence spectre

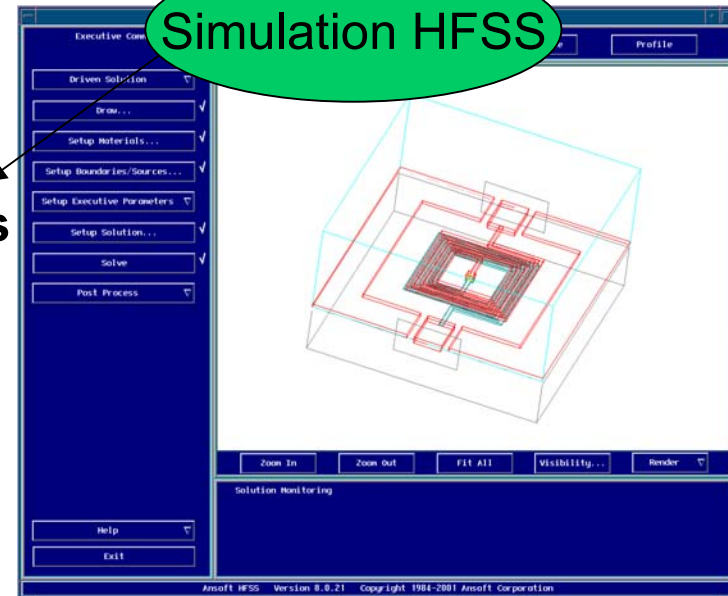


Choix composants

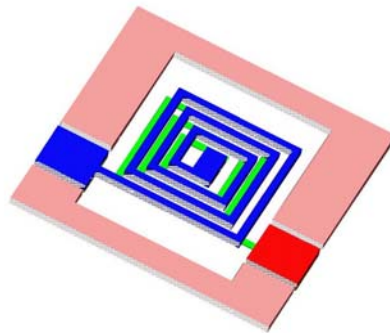
Simulation HFSS

Cadence

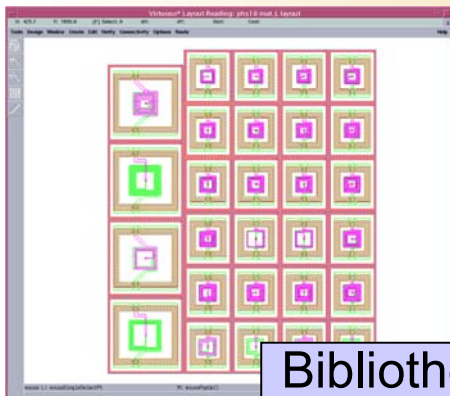
Bibliothèque L,C



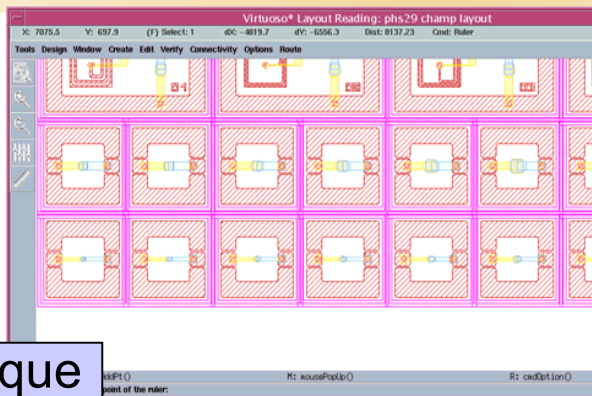
Simulation HFSS



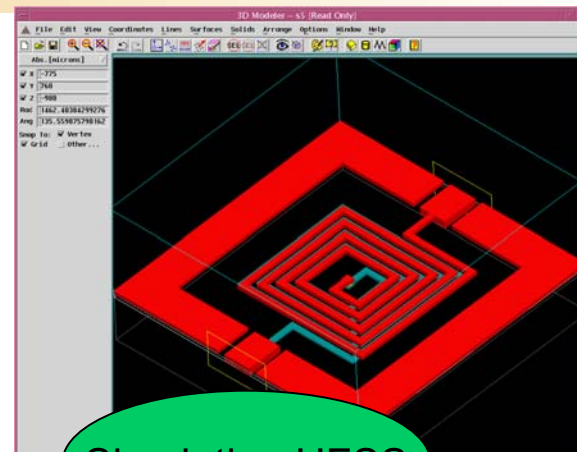
Conception-Phase 2 composants.



Bibliothèque
L,C



Choix composants



Simulation HFSS

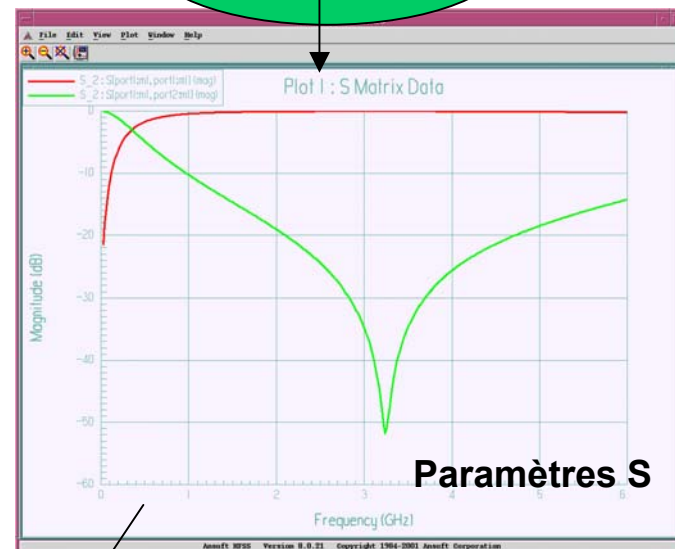
! Touchstone file from Maxwell project L1C6
 # GHZ S MA R 50.000000
 ! Row1=Port1 Row2=Port2()

Frequency	S[1,1]_Mag	S[1,1]_Phs	S[1,2]_Mag
3.000000E+0	8.385713E-02	8.167738E+0	9.922901E-01
4.492500E+0	1.249201E-01	8.044522E+0	9.881259E-01
5.985000E+0	1.653934E-01	7.866077E+0	9.823823E-01

Fichiers paramètres S

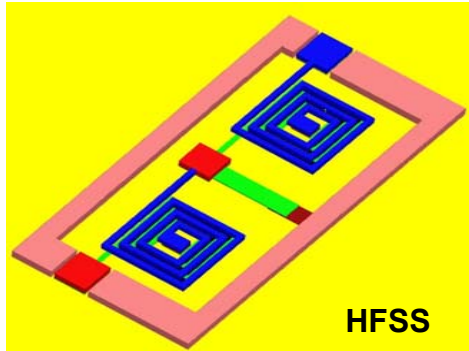
Cadence
spectre

Design circuit réel

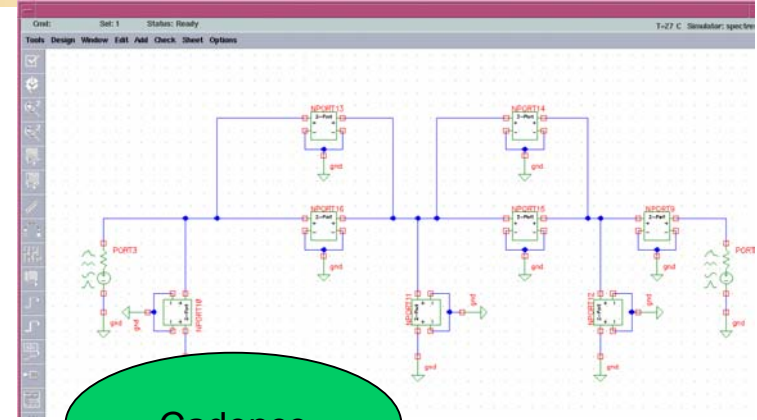


Conception-Phase 3 circuit

Design circuit réel

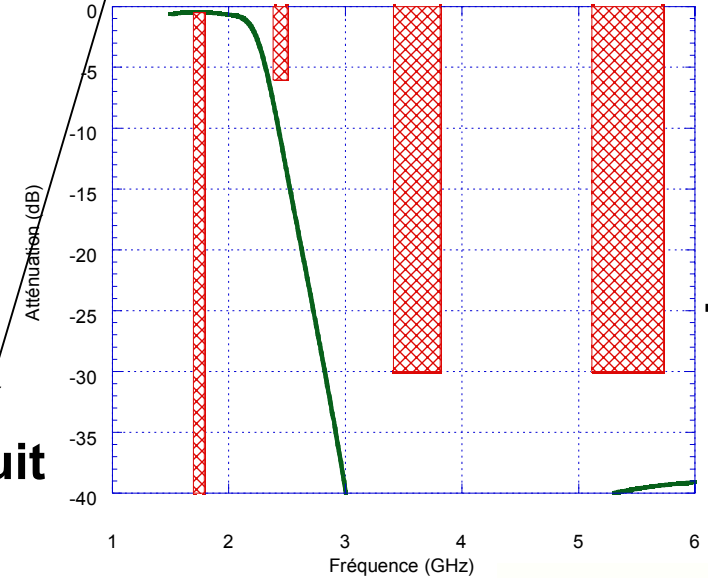


HFSS

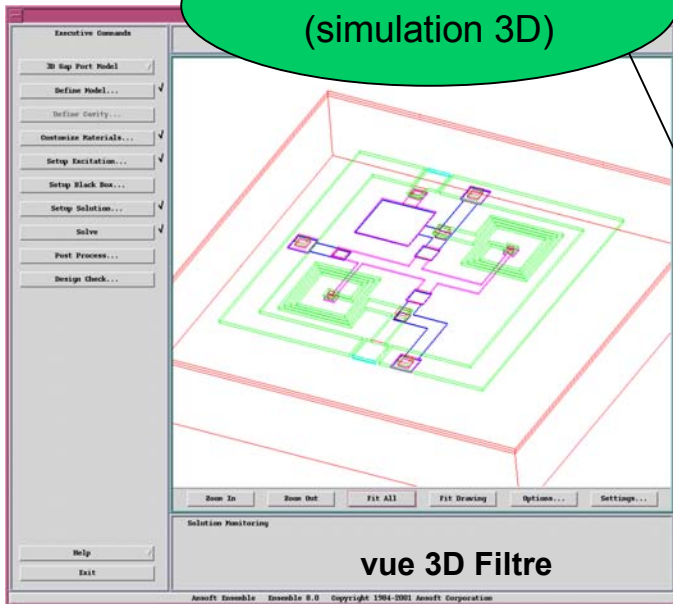


Cadence

mag S21



Evaluation « Ensemble »
(simulation 3D)



vue 3D Filtre

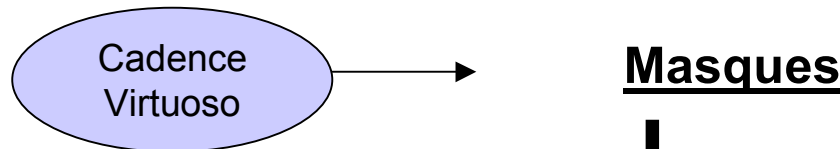
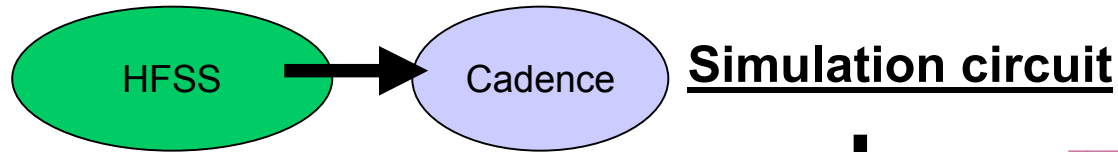
Simulation circuit



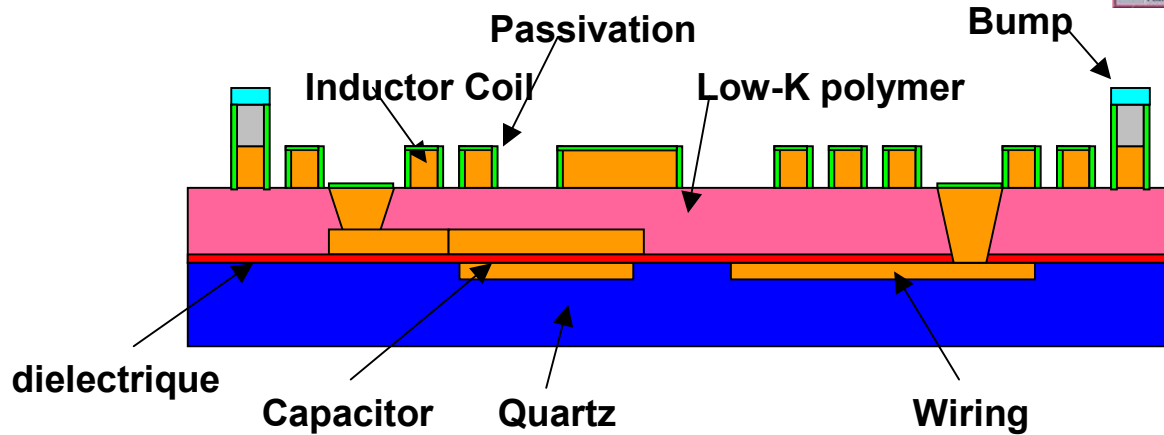
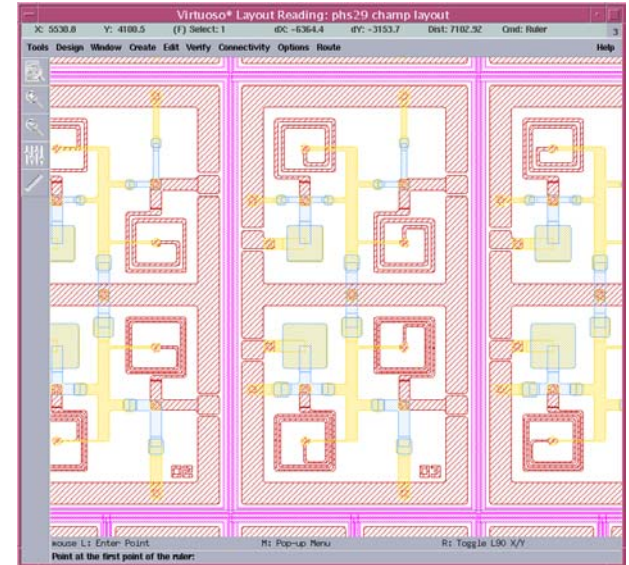
PHS MEMS Confidential



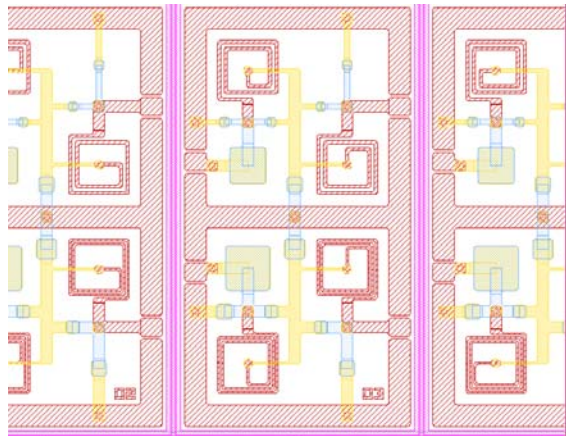
Conception-Phase 4 masques



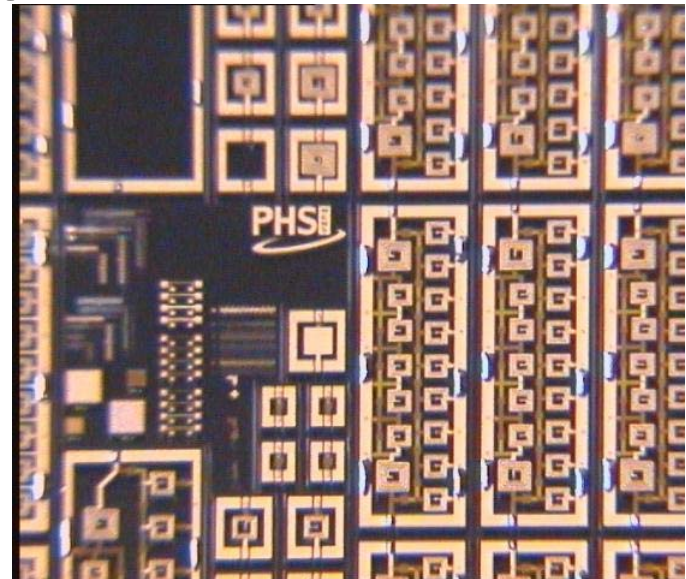
Protos



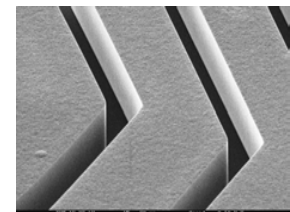
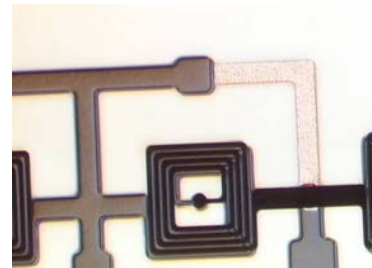
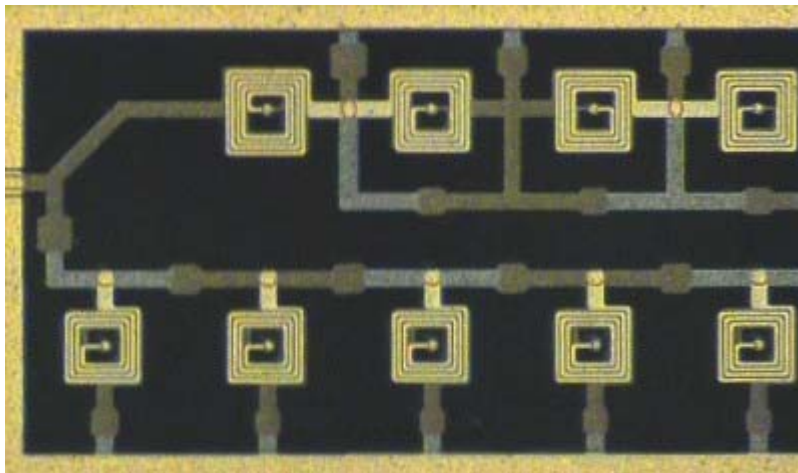
Conception-Phase 5 protos



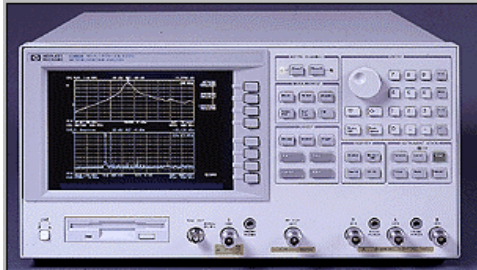
Masques



Protos



Conception-Phase 6 Test

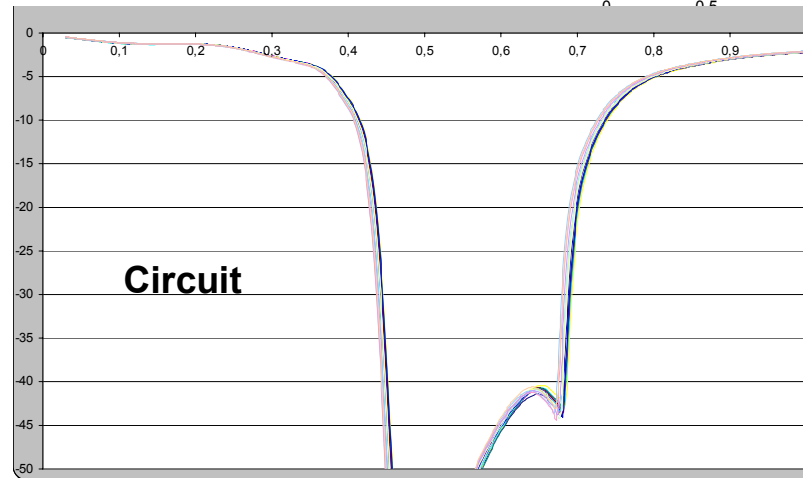
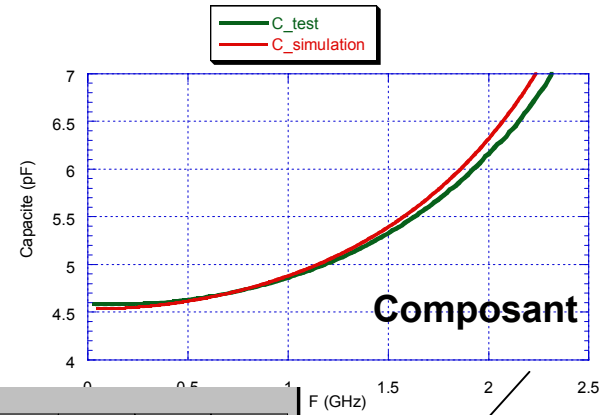
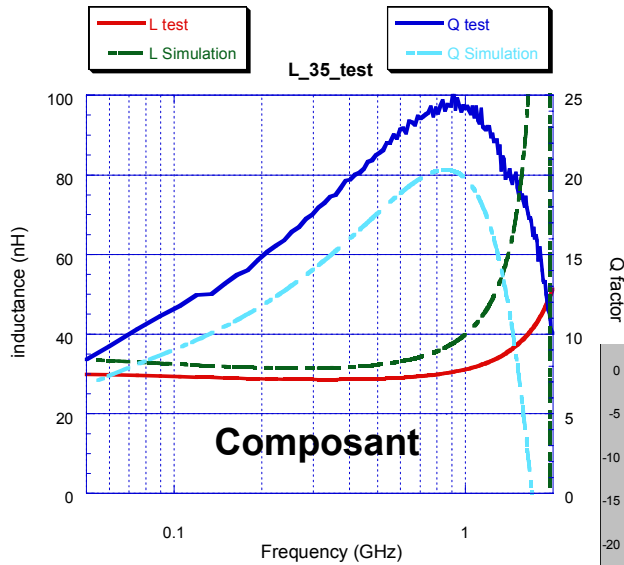


Analyseur de Réseau HP 8753ES

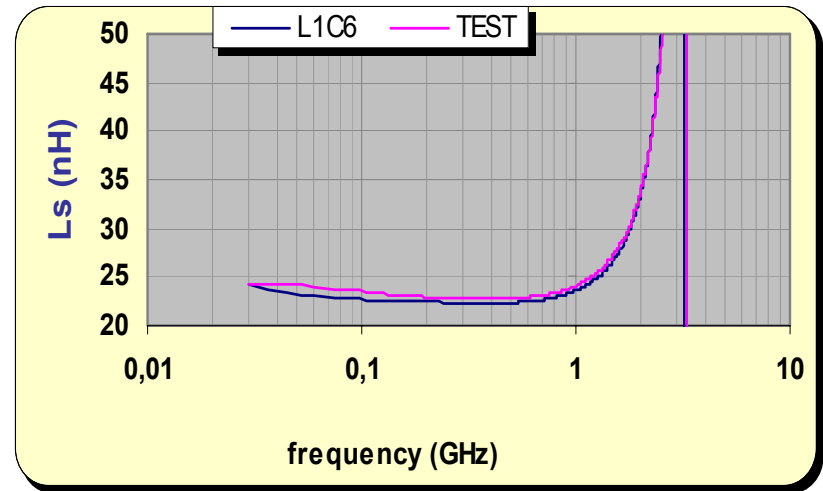
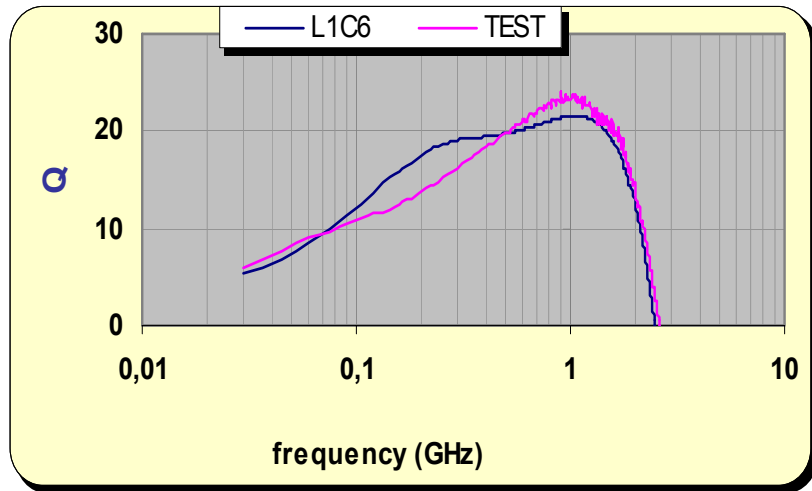
Test



Validation

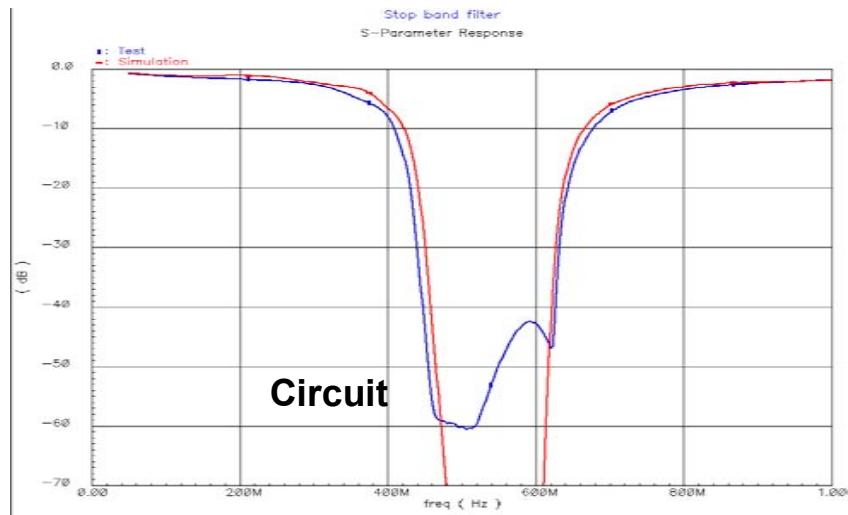


Conception-Phase 7 validation

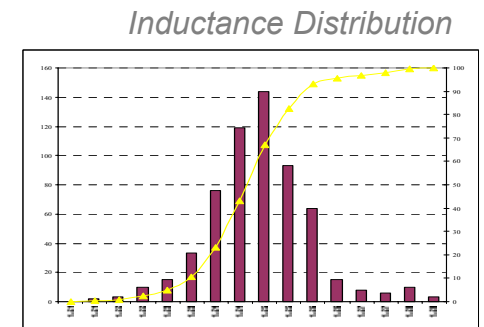


Composant

Composant

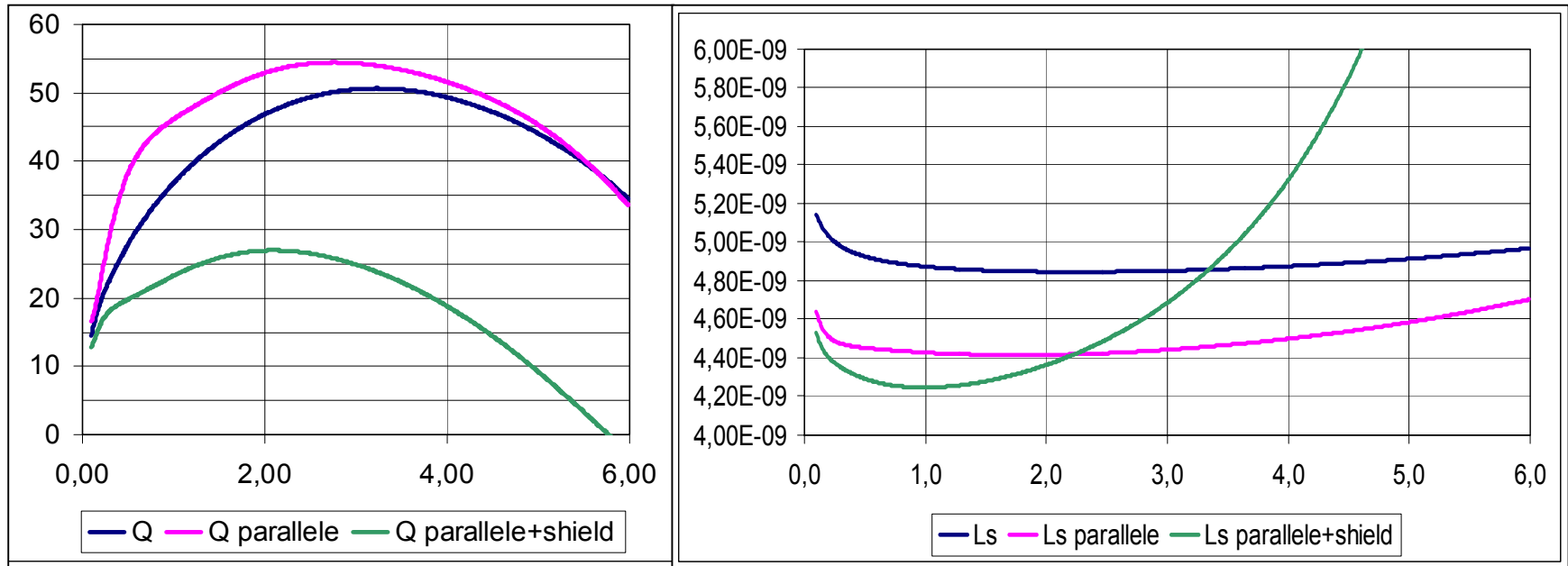


Circuit



Analyse statistique
 →capabilité(cpk,...)

Simulation-Analyse structures



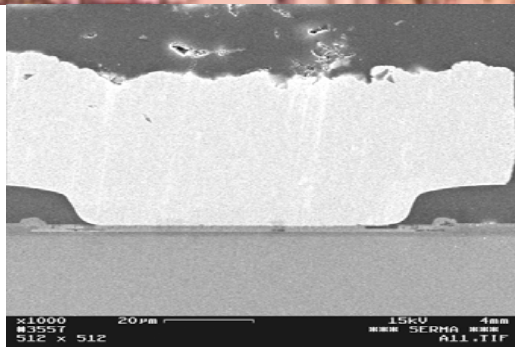
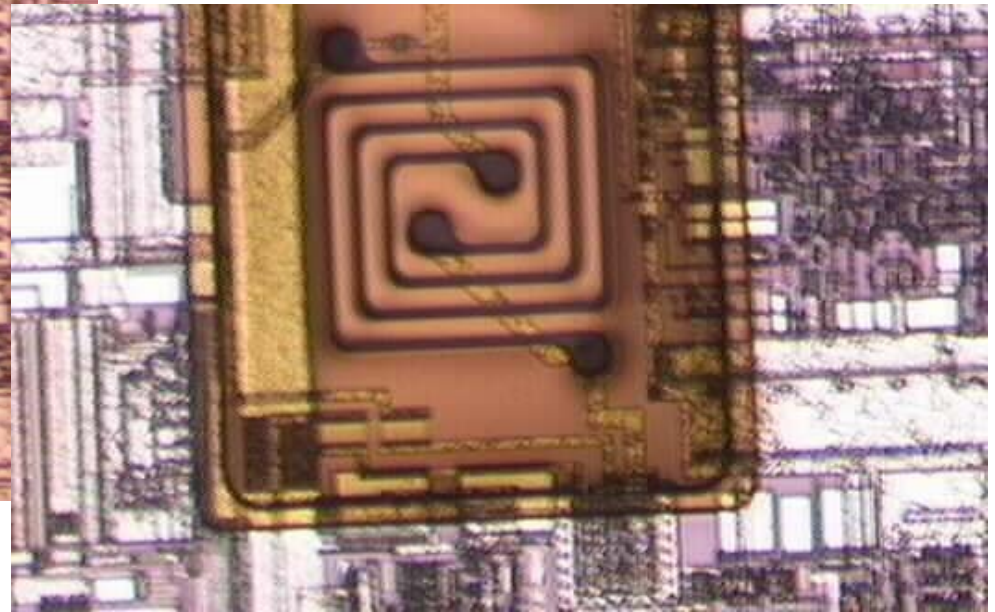
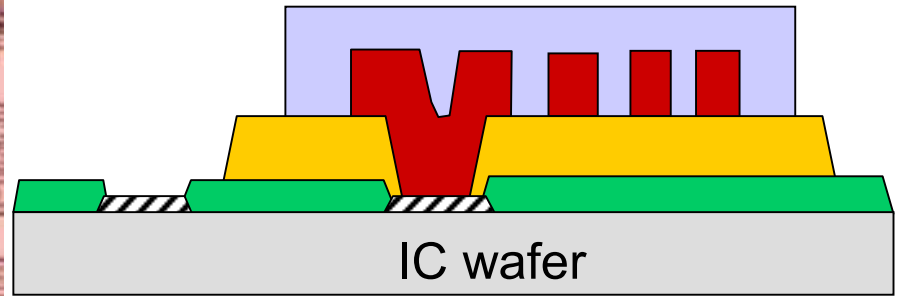
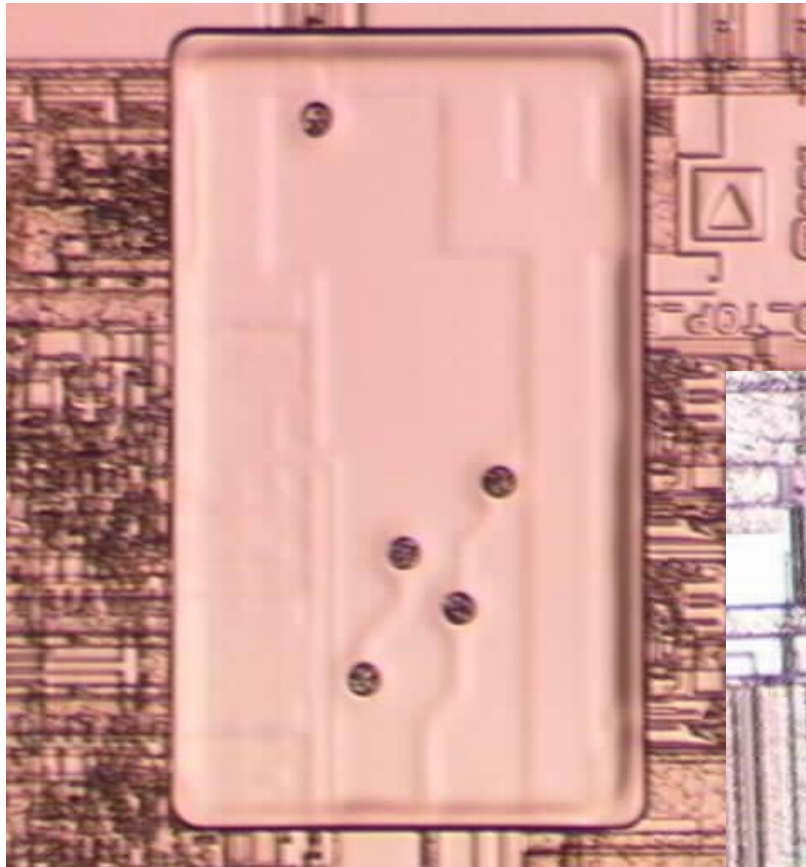
- **Comparaison différents process d'inductances.**

- Inductance 1 niveau standard

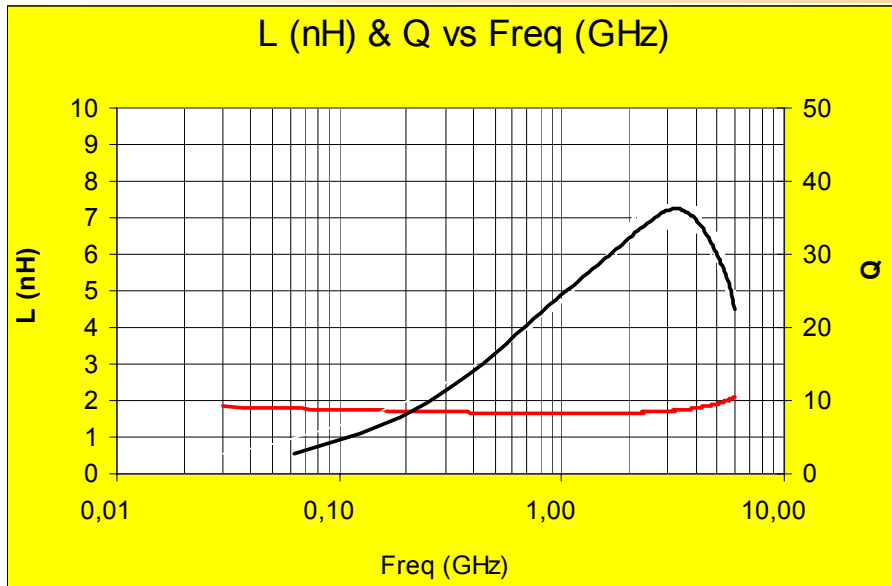
- Inductance 2 niveaux parallèles

- Inductance 2 niveaux parallèles avec écran

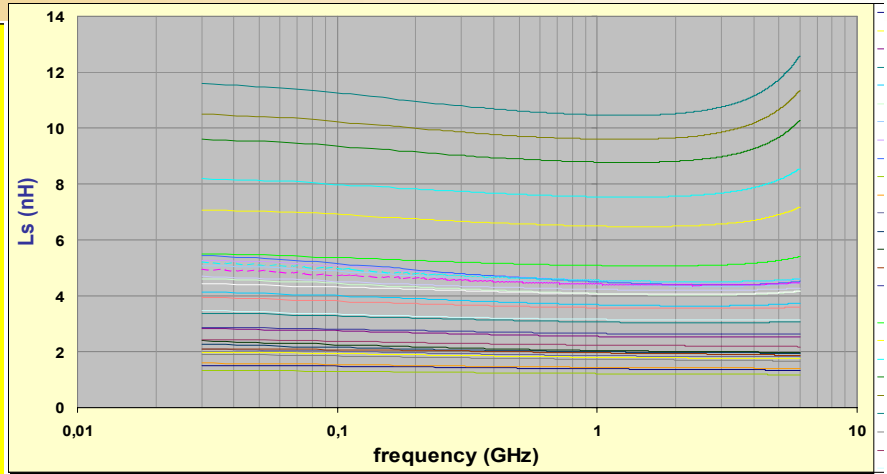
Above IC (Design-Process)



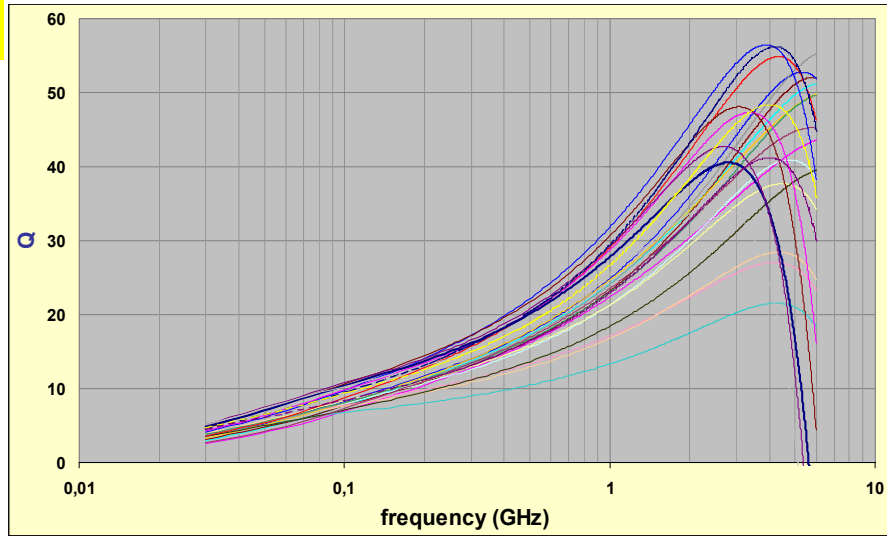
Above IC (Simulation & test)



Résultat test inductance



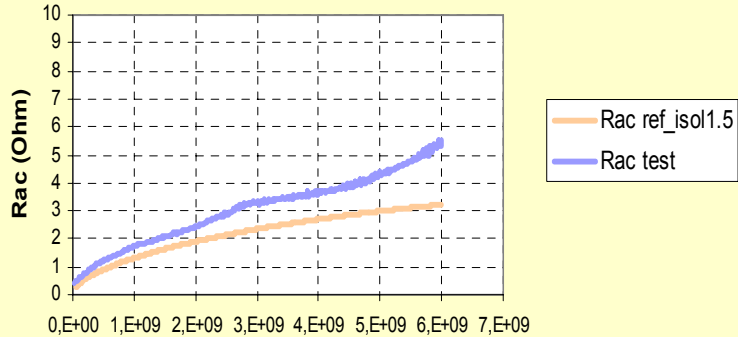
Bibliothèque L-Simulation HFSS (L)



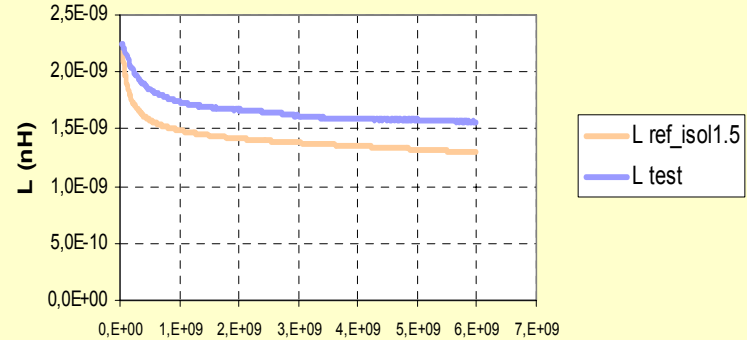
Bibliothèque L-Simulation HFSS (Q)

Solénoïde (test-HFSS)

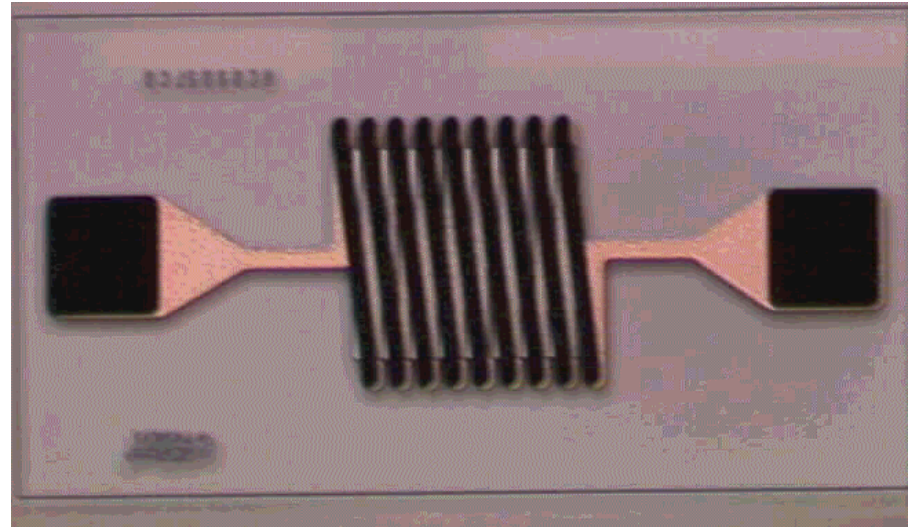
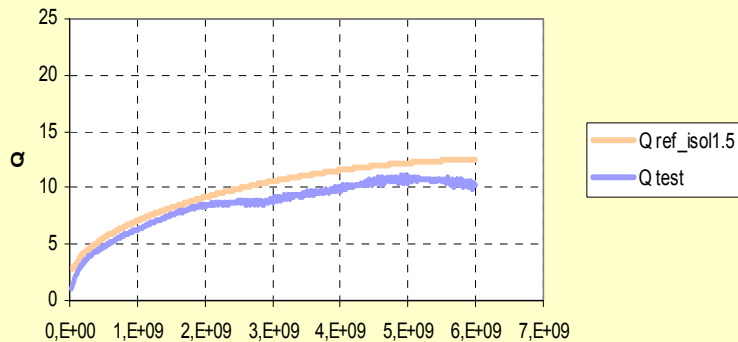
Solenoïde 9 tours à vide
hauteur cœur 4 μm



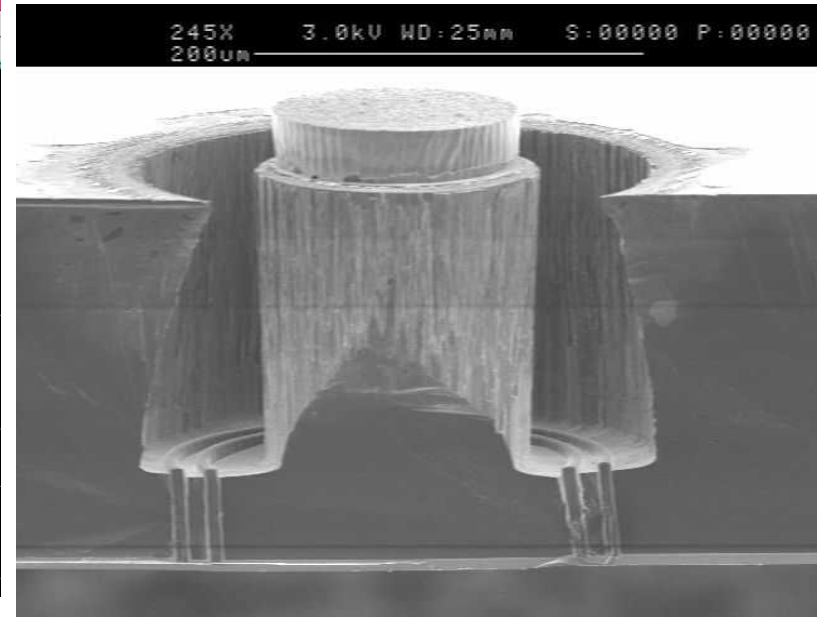
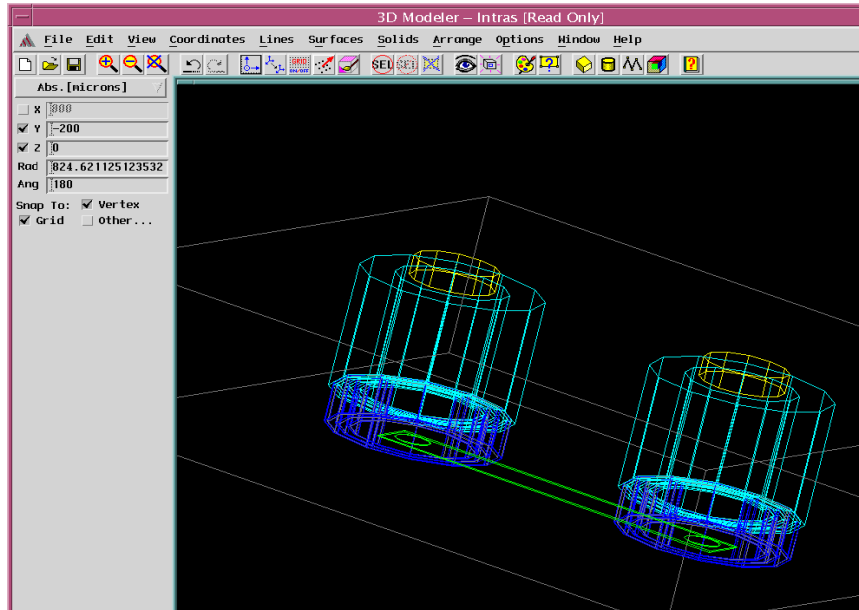
Solenoïde 9 tours à vide
hauteur cœur 4 μm



Solenoïde 9 tours à vide
hauteur cœur 4 μm

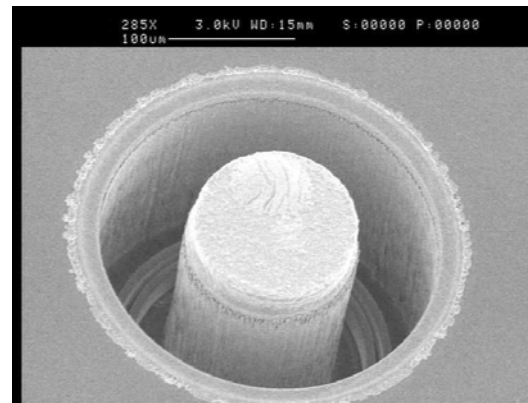
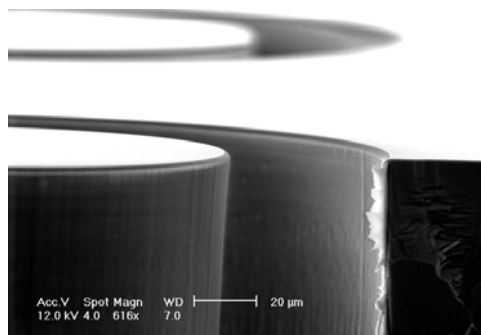


Front-to-Back Contacts (Process-HFSS)



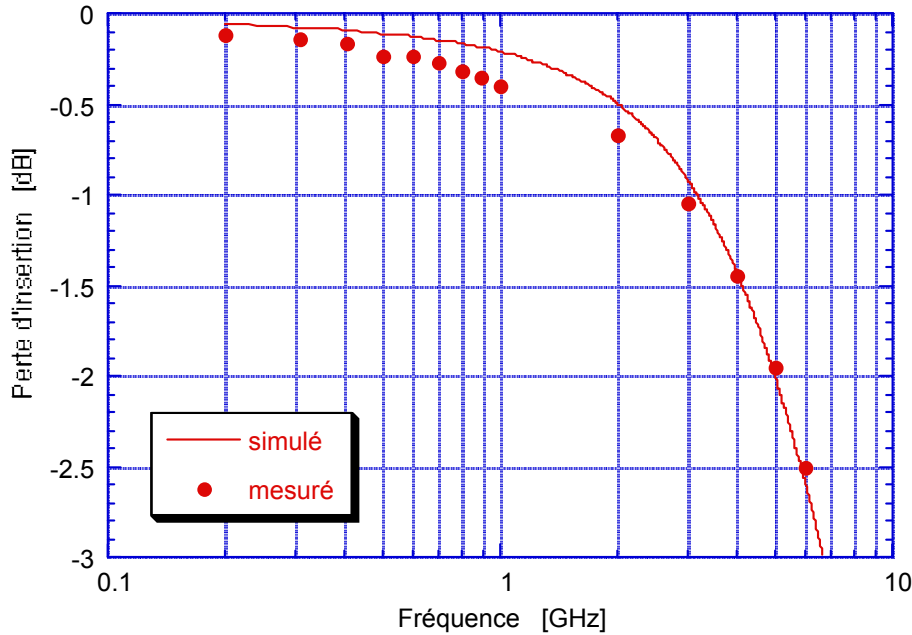
• Characteristics

- 2-in-series resistance $< 1\Omega$
- DC Insulation Res $> 100\text{ M}\Omega$
- Breakdown voltage $> 500\text{ V}$
- Capacitance : $< \text{few pF}$

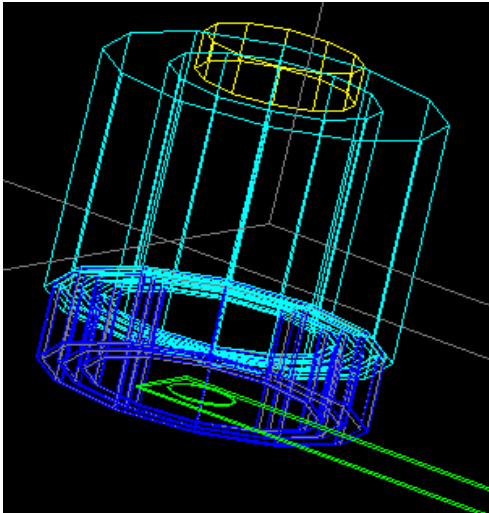
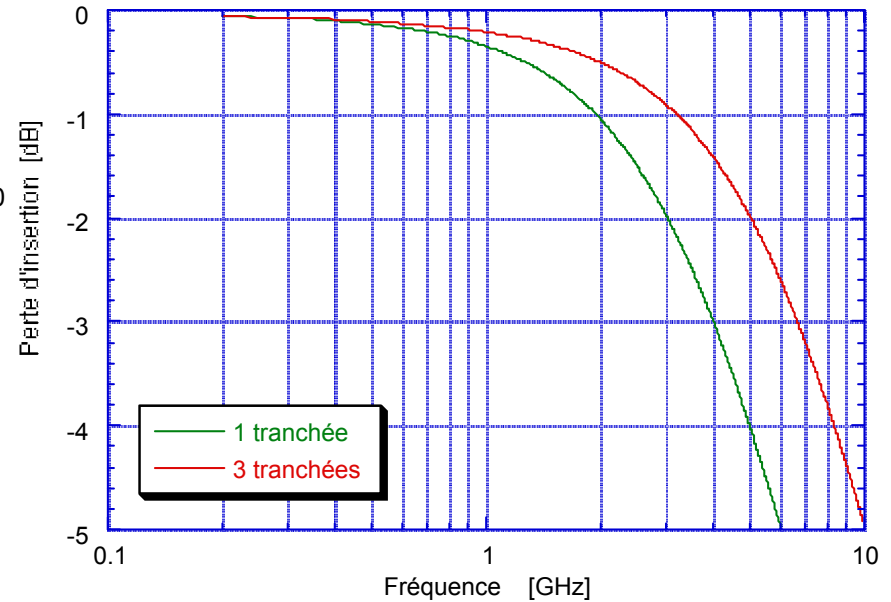


Front-to-Back Contacts (Test-HFSS)

Comparaison simulation et mesure intras 3 tranchées



Simulation intras avec 1 et 3 tranchées





Vous remercie de votre attention.

