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# Switching Noise: Characterization and Analysis Techniques

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*Copies of this presentation are available for download from [www.GigaTest.com](http://www.GigaTest.com)*



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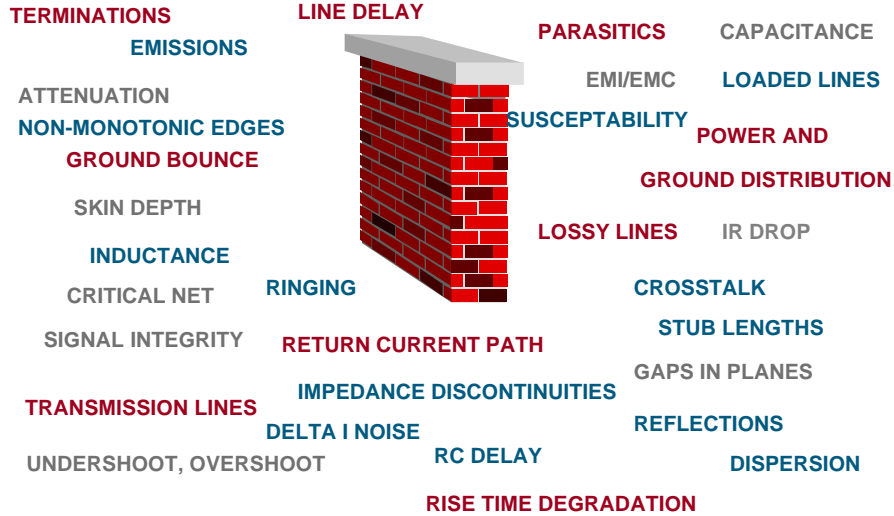
## Overview

***“There are two kinds of design engineers, those that have signal integrity problems, and those that will”***

- The four signal integrity problems
- Origin of Switching Noise
- Building models from measurement: terminating resistors
- Partial Inductance and connector models
- Common and separate return pins



# Signal Integrity Issues

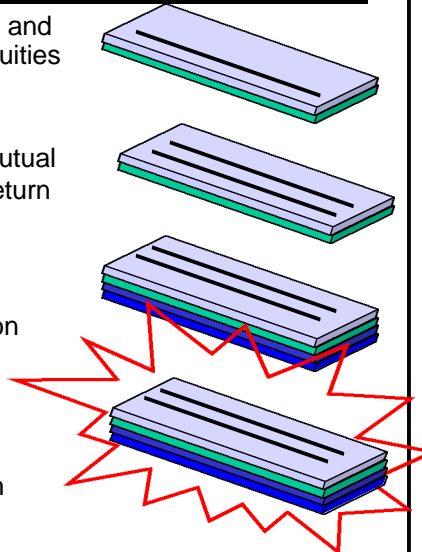


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# The Four High Speed Problems

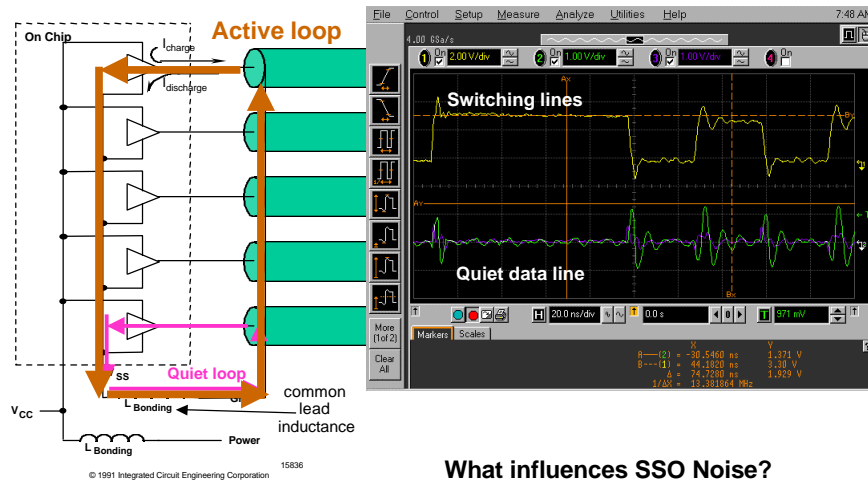
1. **Signal quality** of one net: reflections and distortions from impedance discontinuities in the signal or return path
2. **Cross talk** between multiple nets: mutual C and mutual L coupling with ideal return paths and without (SSO)
3. **Rail collapse** in the power distribution system (PDS): voltage drops across impedance in the pwr/gnd network
4. **EMI** from a component or the system



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## Conceptual Origin of SSO Noise



What influences SSO Noise?

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## What Influences SSO?

$$V_{a(\text{switching noise})} = L_{ab} \frac{dI_b}{dt}$$

- Mutual inductance between the loops
- Number of SSO's (total  $I_b$ )
- $dt$ , i.e., rise time

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## How Much Mutual Inductance is too Much?



$$V_{A(\text{noise})} = L_{AB} \frac{dI_B}{dt} \sim L_{AB} \frac{V_B}{Z_0 \tau} \quad I_B = \frac{V_B}{Z_0}$$

$Z_0 = 50 \text{ Ohms}$   
 $\tau = 1 \text{ nsec}$   
 $V_{A(\text{noise})} < 5\% V_B$

$L_{AB} < 5\% \times 50 \text{ Ohms} \times 1 \text{ nsec} = \mathbf{2.5 \text{ nH}}$



When  $L_{AB} > \sim 2.5 \text{ nH} \times \tau$ , be worried about SSO  
 When  $\tau < L_{AB} / 2.5 \text{ nH}$ , be worried about SSO

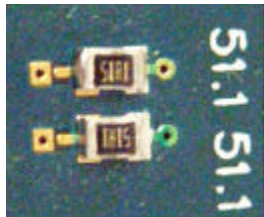
$L_{AB}$	$\tau$ to worry
2.5 nH	1 nsec
1.2 nH	0.5 nsec
0.5 nH	0.2 nsec
0.2 nH	0.1 nsec

How large is  $L_{AB}$  typically?  
 How to minimize  $L_{AB}$  ?

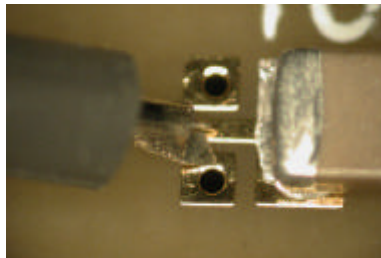


## Example: Coupling Between SMT Terminating Resistors

Two, 0805 resistors, ~ 120 mils centers, far end shorted to return plane ~ 15 mils below surface

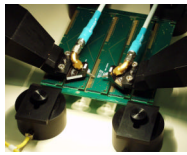


Close up of typical probing method



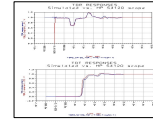


# A Complete Measurement and Analysis System



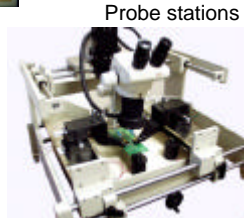
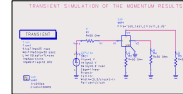
Probing and fixturing

Simulation and Model extraction software



Precision calibration

**GigaTest can provide complete turn key systems and the necessary training**



Probe stations



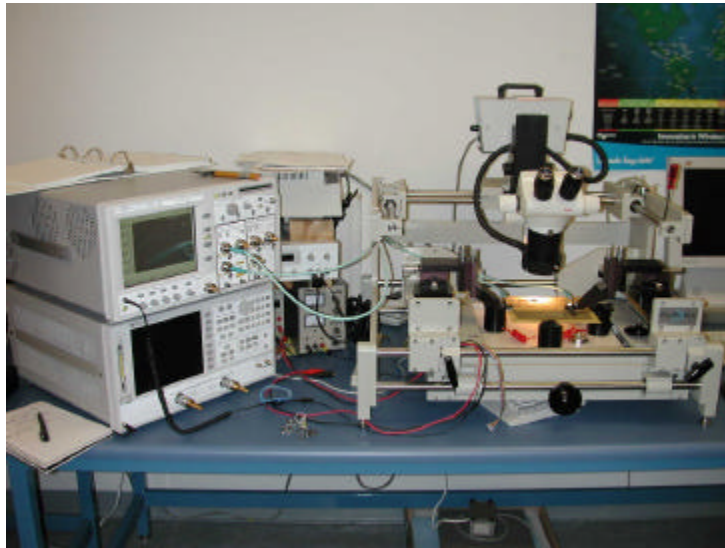
Measurement Instrument



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# Complete Measurement System for All Interconnect Structures

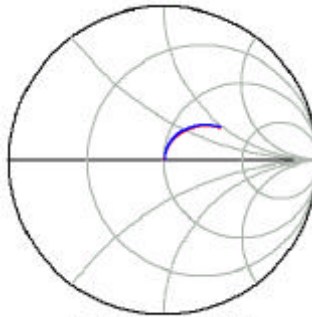


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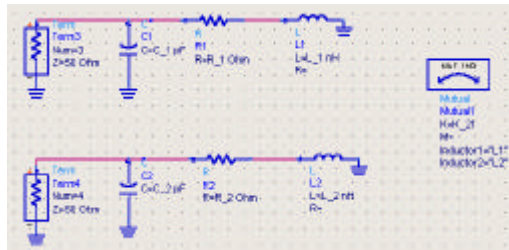
# Modeling Resistors

Modeled and measured  $S_{11}$



freq (12.50MHz to 5.013GHz)

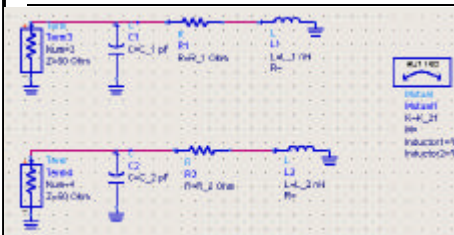
Topology for coupled resistors uses exactly the same circuit model for isolated resistors, with mutual inductance added



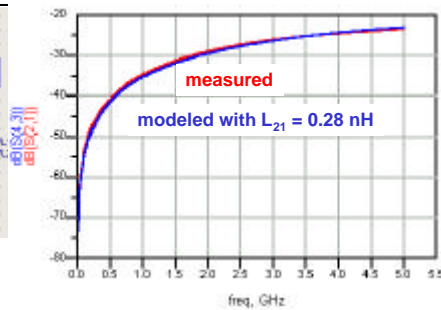
R = 51 Ohm  
L = 1.85 nH  
C = 0.162 pF



# Modeled Cross Talk



R = 51 Ohm  
L = 1.85 nH  
C = 0.162 pF  
 $L_{12} = 0.28$  nH



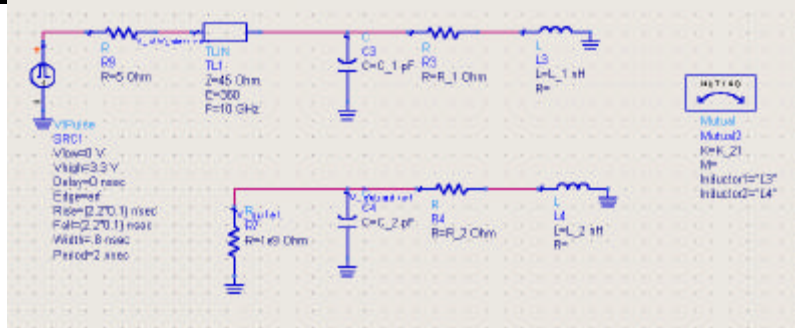
If -30 dB is the allocation in the noise budget, what is the max useable bandwidth for the resistors?

What does the switching noise look like in the time domain?

At what rise time should we start to worry?



## Simulating Switching Noise in the Time Domain



- ✓ Same model of the coupled resistors
- ✓ 5 Ohms source impedance of the driver
- ✓ Quiet line receiver in tri state
- ✓ Rise time of 100 psec, BW ~ 3.5 GHz, 500 MHz clock
- ✓ What is the expected coupling at 3.5 GHz? ~ -25 dB

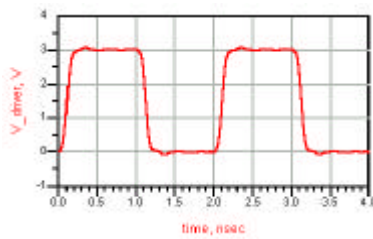
What switching noise might be expected? ~ 5%, of 3.3v ~ 150 mV

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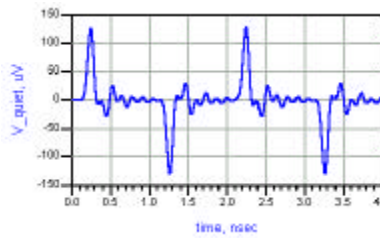


## Simulating Switching Noise

Driver



Quiet receiver



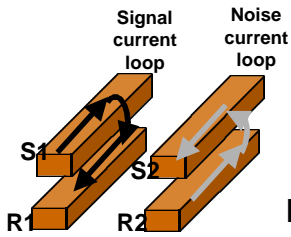
Does this look familiar?

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# Switching Noise, Loop Inductance, Partial Inductance

Describing the switching loops in a connector

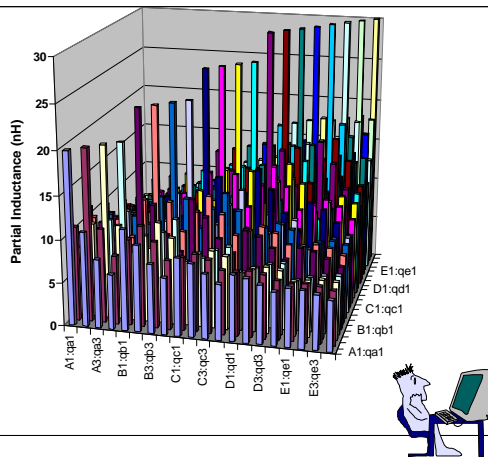
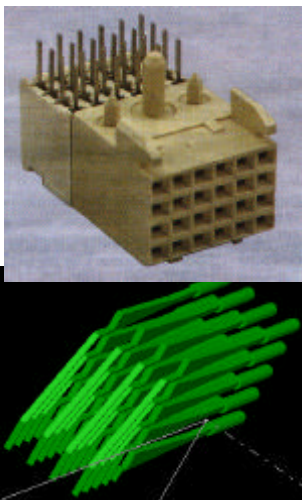


$$L_{loop} = L_{S1} + L_{R1} - 2L_{S1-R1}$$

Loop mutual inductance  
Partial mutual inductances



# Partial Inductance Matrix of a Connector



Using the Ansoft Maxwell Q3D Extractor



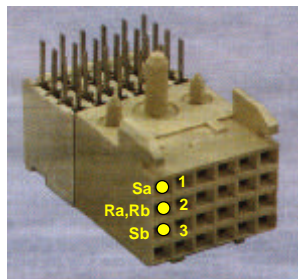
## Forget the Word "Ground"



*Think  
Return Path*



## Sharing a Return Path Pin

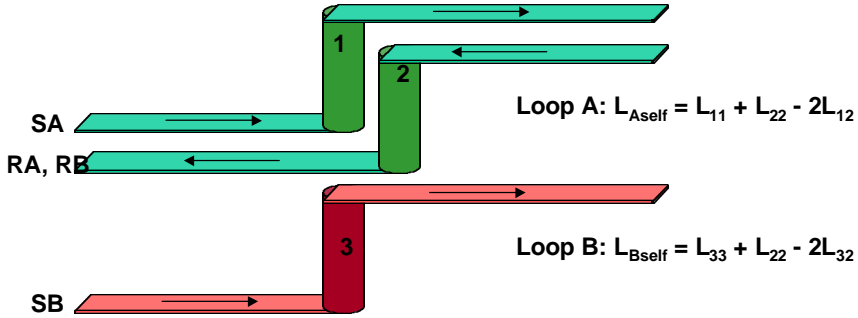


Amp connector

If a is active loop and b is quiet loop,  
What is the noise on b when a switches?



## Worse Case: common return paths



Mutual inductance between A and B Loops:

$$L_{AB} = (L_{31} - L_{32}) + (L_{22} - L_{21}) \sim L_{22}$$

**Mutual inductance between two loops with a common return path can be as large as the self inductance of the common lead inductance**



## Part of the Partial Inductance Matrix

	A1	A2	A3	A4	B1	B2	B3
A1:qa1	19.94	10.89	7.92	6.33	11.61	9.98	7.97
A2:ra2	10.89	19.92	10.87	7.92	9.98	11.61	9.97
A3:qa3	7.92	10.87	19.91	10.89	7.97	9.97	11.61
A4:ra4	6.33	7.92	10.89	19.91	6.55	7.97	9.98
B1:qb1	11.61	9.98	7.97	6.55	23.43	12.51	9.13
B2:rb2	9.98	11.61	9.97	7.97	12.51	23.44	12.50
B3:qb3	7.97	9.97	11.61	9.98	9.13	12.50	23.43
B4:rb4	6.55	7.96	9.98	11.61	7.31	9.13	12.50
C1:qc1	8.95	8.45	7.43	6.43	13.50	11.56	9.23
C2:rc2	8.45	8.95	8.44	7.43	11.56	13.49	11.55
C3:qc3	7.43	8.44	8.95	8.44	9.23	11.56	13.48
C4:rc4	6.44	7.43	8.45	8.95	7.60	9.23	11.56
D1:qd1	7.63	7.39	6.81	6.15	10.48	9.88	8.66
D2:rd2	7.40	7.60	7.37	6.82	9.87	10.48	9.86

Pin selection:

Pin	Path	#
A1	S <sub>A</sub>	1
A2	R <sub>B</sub>	2
A3	S <sub>B</sub>	3

$L_{31} = 7.9 \text{ nH}$   
 $L_{32} = 10.9 \text{ nH}$   
 $L_{21} = 10.9 \text{ nH}$   
 $L_{22} = 19.9 \text{ nH}$

$$L_{AB} = (L_{31} - L_{32}) + (L_{22} - L_{21}) \sim L_{22}$$

$$L_{AB} = (7.9 - 10.9) + (19.9 - 10.9) \sim L_{22}$$

$$L_{AB} = (-3) + (9) \sim 6 \text{ nH}$$

**At what rise time is this important?  
 What would increase the SSO for this connector?**

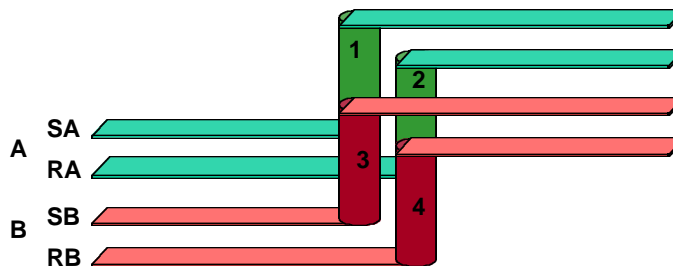


## What Would Increase SSO?

- More pins switching simultaneously, in proximity to each other
- More pins using the same common return path
- Higher mutual inductance between adjacent paths:
  - ✓ Longer pins
  - ✓ Pins farther apart
  - ✓ Narrower pins
- What would decrease SSO?



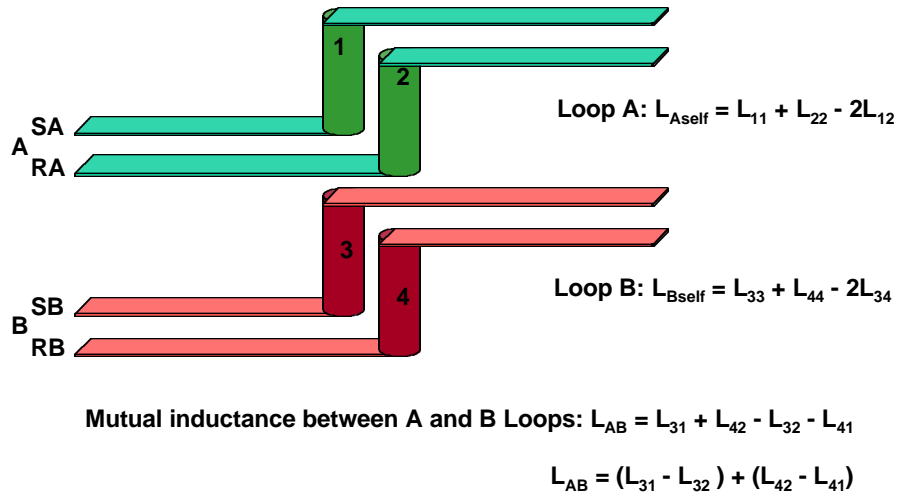
## Each Signal Path Has Its Own Return Path



1. What are the loops?
2. What is the mutual inductance between the loops,  $L_{AB}$ ?



# Mutual Inductance in Connectors



# With Separate Return Path Pins

	A1	A2	A3	A4	B1	B2	B3
A1:qa1	19.94	10.89	7.92	6.33	11.61	9.98	7.97
A2:ra2	10.89	19.92	10.87	7.92	9.98	11.61	9.97
A3:qa3	7.92	10.87	19.91	10.89	7.97	9.97	11.61
A4:ra4	6.33	7.92	10.89	19.91	6.55	7.97	9.98
B1:qb1	11.61	9.98	7.97	6.55	23.43	12.51	9.13
B2:rb2	9.98	11.61	9.97	7.97	12.51	23.44	12.50
B3:qb3	7.97	9.97	11.61	9.98	9.13	12.50	23.43
B4:rb4	6.55	7.96	9.98	11.61	7.31	9.13	12.50
C1:qc1	8.95	8.45	7.43	6.43	13.50	11.56	9.23
C2:rc2	8.45	8.95	8.44	7.43	11.56	13.49	11.55
C3:qc3	7.43	8.44	8.95	8.44	9.23	11.56	13.48
C4:rc4	6.44	7.43	8.45	8.95	7.60	9.23	11.56
D1:qd1	7.63	7.39	6.81	6.15	10.48	9.88	8.66
D2:rd2	7.40	7.60	7.37	6.82	9.87	10.48	9.86

Pin selection:

Pin	Path	#	
A1	SA	1	$L_{31} = 7.9 \text{ nH}$
A2	RB	2	$L_{32} = 10.9 \text{ nH}$
A3	SB	3	$L_{41} = 6.3 \text{ nH}$
A4	RB	4	$L_{42} = 7.9 \text{ nH}$

$$L_{AB} = (L_{31} - L_{32}) + (L_{42} - L_{41}) = 7.9 - 10.9 + 7.9 - 6.3 = 1.4 \text{ nH}$$

Conclusions:

- 1) 30% pins as return paths has M ~ 6 nH
- 2) 50% pins as return paths has M ~ 1.4 nH (a reduction of > 75% in SSO)
- 3) Max. usable rise time ~ 0.5 nsec: 4x higher usable bandwidth than for common return pins



## Conclusions

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- Switching noise will only get worse as rise times decrease
- If you have the physical part, measurements can offer a way of extracting a model to predict switching noise
- In the design phase, a quasi static 3D solver can offer a way of extracting a model to predict switching noise
- GigaTest Labs can assist you in:
  - ✓ providing a complete turn key measurement system
  - ✓ performing measurements and creating models for you
  - ✓ helping you move up the learning curve with signal integrity training

[www.GigaTest.com](http://www.GigaTest.com)



## Resources Posted on [www.GigaTest.com](http://www.GigaTest.com)

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- ✓ Recommended bibliography with links to [www.fatbrain.com](http://www.fatbrain.com)
- ✓ List of:
  - relevant trade journals
  - professional societies and other web sites
  - Application Notes and presentations for download (> 50)
- ✓ Complete list of signal integrity engineering courses from GigaTest
- ✓ Products for optimizing high bandwidth measurements

[www.GigaTest.com](http://www.GigaTest.com)



## GigaTest Labs Courses in Signal Integrity Engineering that cover switching noise

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- GTL01 Survey of signal integrity problems and solutions
- GTL122 a Fundamental principles of SI  
b Fundamental principles of Transmission lines
- GTL130 a Transmission line characterization with TDR  
b Transmission line stack up design
- GTL250 a High speed board design: signals  
b High speed board design: switching noise, ground bounce and EMI
- GTL260 a Creating high bandwidth models from measurement: 1<sup>st</sup> order models  
b Creating high bandwidth models from measurement: high bandwidth
- GTL262 a Creating high bandwidth models from calculations : 1<sup>st</sup> order models  
b Creating high bandwidth models from calculations : numerical simulation